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# Analysis of VCO based Noise Shaping ADCs Linearized by PWM Modulation

Luis Hernandez, Enrique Prefasi, Susana Paton Electronics Technology Dept. Carlos III University Madrid, Spain luish@ing.uc3m.es

Abstract- Nonlinearity is one of the main problems associated with VCO based noise shaping ADCs. Their open loop architecture does not permit correction of the nonlinear voltage to frequency response of the VCO by feedback. Recently, linearization of a VCO ADC by Pulse Width Modulation (PWM) precoding has been proposed. Here, the input signal is encoded by a PWM modulator to drive the VCO with a 2-level signal, thus eliminating the nonlinearity of the VCO. This paper analyzes the remaining inherent distortion in such modulators which originates from subsampling the PWM sidebands.

#### INTRODUCTION I.

New data converter and signal processing techniques are being developed to cope with low performance of nanometer CMOS analog circuits. Several of these techniques are based on time encoding mechanisms. One of such ADC architectures is based on the phase accumulation effect of a modulated VCO [1]. These converters are efficiently constructed with ring oscillators but exhibit poor linearity. Recently, a new linearization technique has been proposed [2],[3], that seizes the precise signal encoding of an analog Pulse Width Modulator (PWM) into a two-level signal to modulate a VCO. This way, the need for the voltage to frequency characteristic of the VCO to be linear, is eliminated as only two frequencies have to be generated. Such a VCO modulated at two operating points only, will be designated as a Gated Ring Oscillator (GRO) [3] when implemented with inverters.

#### MODEL OF VCO BASED NOISE-SHAPING ADC II.

Figure 1.a displays the building block of a VCO noise shaping ADC. In this figure, a VCO is modulated by input signal s(t) defined between  $0 \le s(t) \le 1$ . The oscillator output is applied to an asynchronous counter that increases its count by one each time the oscillator phase wraps around  $2\pi$ . The counter is sampled at a sampling frequency fs and the sampled value is differentiated generating the output  $y_s[n]$ . Such a VCO-based ADC is equivalent to a conventional firstorder sigma modulator with M=f<sub>max</sub>/f<sub>s</sub> quantization levels,

Pieter Rombouts ELIS Ghent University Ghent, Belgium

being f<sub>max</sub> the maximum oscillation frequency of the VCO when s(t)=1. This system can be found to be equivalent to the system described in [1], except for the gain of the VCO and the quantizer step size, as ring oscillators have multiple output phases instead of only one.



Figure 1. Block diagram of a VCO-based noise shaping ADC.

Figure 1.b shows an equivalent system to fig. 1.a that permits to describe the system equations. Input s(t) modulates the frequency of the VCO, hence, its phase  $\varphi(t)$  represents the integral of s(t) with an integration gain  $k=2\pi f_{max}$ . The effect of the counter of fig. 1.a is represented by a uniform quantizer that adds quantization noise q(t). The differentiating filter after the sampler in fig. 1.a can be moved to the other side of the sampler in fig. 1.b, by replacing  $(1-z^{-1})$  by  $(1-e^{-sTs})$ , where  $Ts=1/f_s$  represents the sampling period.

The system in fig. 1.b is in continuous time up to signal y(t), which permits to calculate its Noise (NTF) and Signal (STF) Transfer Functions directly in the Laplace domain:

$$\varphi(t) = k \int_{0}^{t} x(\tau) d\tau \rightarrow \Phi(s) = \frac{k}{s} S(s)$$

$$Y(s) = NTF(s) \cdot Q(s) + STF(s) \cdot S(s) \qquad (1)$$

$$NTF(s) = (1 - e^{-sT_s}) \quad STF(s) = k \cdot \frac{(1 - e^{-sT_s})}{s}$$

One of the practical problems of the circuit of fig. 1.a is the nonlinearity associated with the voltage to frequency

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translation of the VCO. To overcome this problem, we may use the system of Figure 2.a where the input signal s(t) is first PWM encoded. The equations in the previous section allow defining the equivalent system in Figure 2.b



Figure 2. ADC built with a PWM and a Gated Ring Oscillator.

This noise shaping ADC will exhibit a first order noise transfer function and a sinc shaped STF with zeros at multiples of the sampling frequency  $f_s$ . We must also encode the band limited input analog signal s(t) as a two level signal  $x_p(t)$  to connect it to the VCO-based ADC. PWM modulators encode a signal using a periodic or quasi periodic carrier signal of frequency  $f_c$ . We will define the Carrier Over Sampling Ratio (COSR) as the ratio between the carrier frequency of the PWM modulator and the sampling frequency of the noise shaping modulator:

$$COSR = \frac{f_c}{f_s} \tag{2}$$

A PWM signal contains the input signal s(t) in its low pass components (baseband), and hence, s(t) will be encoded by the VCO-based ADC. However, modulation sidebands centered at the harmonics of the PWM carrier will be present as well. These sidebands can pass through the STF and be subsampled by the sampler of fig. 2.b, falling within the baseband. This problem imposes a fundamental limit of the system of fig 2.a, and will be the subject of the next section.

#### III. SYSTEM LEVEL DESIGN OF A PWM – VCO ADC

Two essentially different kinds of PWM modulators can be considered: synchronous or asynchronous, each one generating different spectra. The spectra of asynchronous modulators is strongly dependent on the input signal. For this reason we will focus on synchronous modulators only [3]. Synchronous PWM modulators are in practice directly driven by the band limited, continuous time input signal s(t). However we will consider an additional reference case where the PWM modulator is driven by a sampled and held version of the input signal s(t). In this section we will explain how the combination of pulse width modulation and sampling by the VCO quantizer produces baseband distortion and show how a suitable choice of the COSR affects this. Since we want to study these effects separately from the inherent quantization noise of the VCO quantizer (q(t) in fig. 1), we will base our discussion on the output signals x(t) (and its sampled version  $x_s[n]$ ), as defined in fig. 2.b.



Figure 3. PWM with (a) uniform (b) natural sampling.

#### A. Synchronous PWM with uniform sampling

Synchronous PWM modulators employ a sawtooth waveform as carrier to create a pulsed signal of fixed frequency and variable pulse widths. Figure 3.a shows a conceptual block diagram of such a modulator with a uniformly sampled input. The spectral content of synchronous PWM signals is well controlled because the carrier may be derived from a digital clock, and then, sidebands at the harmonics of the carrier are located at fixed frequencies. To apply a uniformly sampled (and held) signal to the PWM modulator, we may use the sampler shown in figure 3.a operated at  $f_s$ . An analysis of the PWM spectra [4] would show that the PWM signal  $x_p(t)$  contains distortion in the baseband. This is illustrated in Figure 4.a, which shows the spectra of  $x_p(t)$  in a simulation for the case of an oversampling ratio OSR=16, COSR=1 and a -6dBfs dithered input tone at 1/4 of the signal bandwidth (distortion tones into dotted square). However, when passing this signal trough the VCO quantizer (fig. 2.b) the combined action of the STF sinc filter and the sampling, produces a remarkable phenomenon when COSR is an integer number. In this case, the sampled signal x<sub>s</sub>[n] will be equal to the area of an integer number of PWM pulses, whose duty cycle corresponds to  $s(nT_s)$ . Hence:

$$x_{s}[n] = k \int_{(n-1)T_{s}}^{nT_{s}} x_{p}(t) \cdot dt = k \cdot s(nT_{s})$$
<sup>(3)</sup>



Figure 4. Spectrum of  $x_p(t)$  when uniform (a) and natural (b) sampling are used.

Equation (3) implies that the overall output signal is an exact representation of the input signal s(t), scaled by

constant k. This is illustrated in Figure 5.a, which shows the FFT of  $x_s[n]$  as Fig. 4.a but without spurs.

This way, PWM precoding does not affect the accuracy of the ADC. We will see that this is not the case for other types of PWM that will introduce distortion. The situation where the PWM modulator operates on a sampled signal using an integer value for COSR, corresponds to the ideal case for the converter of fig. 2.b.



Figure 5. FFT of xs[n] obtained with uniform sampling PWM (a) and a natural sampling PWM (b).

#### B. Synchronous PWM with natural sampling

Unfortunately, if we want the PWM modulator to be easily implementable and low power, it would be desirable that the sampler is removed (see fig. 4.b) and COSR<1 to have a slowly switching signal at the comparator. Removing the sampler produces a naturally sampled PWM signal. In this case, the PWM baseband spectra would be equal to that of s(t) [4], and would not have distortion. This is illustrated in fig. 4.b where the same simulation as for fig. 4.a was carried out but now, without the sample and hold.

However, when this signal is applied to our VCO quantizer, the high frequency modulation side bands will alias to the baseband and produce spurs. This is illustrated in fig. 5.b., where the SNDR equals 74 dB only. This problem has to be taken into account in the design of the PWM-VCO ADC as a system level limiting factor.

## IV. SELECTION OF COSR

In the previous section we have assumed COSR=1. However, this is not the best practical choice. To evaluate the optimum value of COSR, some understanding of the aliasing effect of the carrier sidebands in fig. 2.b is required. This aliasing effect is explained in Figure 6. We will assume that an input tone of frequency  $f_{in}$  is encoded with a PWM modulator using COSR<1. The spectra of a PWM signal has been analyzed mathematically [4] and in essence, is composed of groups of multiple tones (sidebands) located at each harmonic of the carrier, spaced by integer multiplies of  $f_{in}$ . Fig. 6 shows a simplified sketch of the spectrum  $X_p(\omega)$  of  $x_p(t)$  together with the STF( $\omega$ ) (dashed line). The sidebands A, B, C located at the carrier harmonics  $f_c$ ,  $2f_c$ ,  $3f_c$  etc, will be first attenuated by the STF. The discrete time Fourier transform of  $x_s[n]$  will exhibit aliased tones at frequencies  $\Omega_a$ , given by:

$$\Omega_a = 2\pi \cdot rem \left( \frac{Nf_{in} \pm Mf_c}{f_s} \right) \quad N = 0, 1, 2... \quad M = 1, 2... \quad (4)$$

Function rem() in (4) is the remainder after division. Only a few aliases A', B', C' are shown in fig. 6. The power of the aliased tones cannot be computed directly from the STF attenuation because several tones alias to the same locations its addition depends on their phase.



Figure 6. Sideband aliasing in the proposed system (fig. 2).

A mathematical analysis of the exact power of the aliased sidebands is out of the scope of this paper. However, fig. 6 permits to draw an interesting conclusion. All aliases are filtered by the side lobes of a sinc function whose nulls alias to DC. For a tone to be aliased close to DC it has to be close to an integer multiple of f<sub>s</sub> and hence, it will be highly attenuated. As a consequence, the distortion created by aliasing will have high pass spectra with a zero at DC, just as the quantization noise of the ADC itself. Now, we will investigate the effect of COSR in the SNDR by behavioral simulation of the ADC of fig. 2. We have plotted in Figure 7.a the SNDR obtained at  $x_s[n]$  using uniform sampling in fig. 2.b and sweeping COSR in the same modulator and conditions of fig. 5. The SNDR has been calculated in fig. 7 using four dithered tones spread along the input signal band for each value of COSR, showing the average for all tones and the maximum/minimum SNDR.

In fig. 7.a, the SNDR of the synchronous PWM is limited by dither to 92dB at integer multiplies of  $f_s$ , which can be observed at COSR=1. At this point, any input frequency has the maximum SNDR as explained by (3). As COSR decreases, the difference between maximum and minimum SNDR increases up to approximately 20dB with periodic maxima and minima at rational values of COSR. The choice of a low COSR ratio [3] permits to reduce the power of the analog circuitry that implements the PWM, as the switching speed is slower, but limits the maximum SNDR achievable. Figure 7.b shows the same data as fig. 7.a but using natural sampling, as it would correspond to a practical hardware implementation. In this case, the synchronous modulator shows SNDR local minima at integer multiplies of COSR, as opposed to fig. 7.a. Also, as an advantage, the difference between maximum and minimum SNDR at low COSR is 10dB smaller in average than in fig. 7.a.



#### V. SIMULATIONS

To investigate the consequences of the analysis of the previous section, we have simulated the complete system (now also including the quantization noise of the VCO-quantizer) of fig. 2 to evaluate the effect of all impairments in a naturally sampled synchronous PWM modulator. We have considered an OSR=32 and a noise shaping modulator with a 32 level quantizer, which could correspond to a Gated Ring Oscillator with 32 stages. An ideal sigma delta modulator with these parameters would produce a peak SNDR of approximately:



(5)

Figure 8. Dynamic range of PWM-VCO.

To ease implementation we will use COSR<1 but such that  $f_c$  is always sufficiently larger than the signal bandwidth defined by OSR to ensure proper operation of the PWM modulator. In the simulation, COSR has been swept between 4 times the signal bandwidth up to  $f_s/2$ . Figure 8 shows the dynamic range obtained for the COSR values that produce the maximum and minimum peak SNDR, corresponding to COSR=0.44 (70.8dB) and COSR=0.0625 respectively. These

results are consistent with fig. 7, where SNDR decreases as COSR is closer to the minimum value. Figure 9.a shows the FFT of  $x_s[n]$  for COSR=0.44 and Figure 9.b for COSR=0.0625 at Vin=-4dBFull-Scale. The SNDR at fig. 9.a and fig. 9.b are 76dB and 60dB respectively. If we add the quantization noise contribution, we would obtain at  $y_s[n]$  a SNDR=70dB for COSR=0.44 and a SNDR=59dB for COSR=0.0625, which correspond with the values displayed in Fig. 8. Fig. 9 shows in both cases high pass distortion spectra, as predicted in section III.B.

## VI. CONCLUSIONS

We have studied VCO-based quantizers that are linearized by PWM pre-coding. We have shown that the modulation sidebands of the PWM, when passing through the VCO quantizer may alias to the low pass band and affect the SNDR. We have demonstrated that this effect is significantly different for various types of PWM modulation schemes. Also, the choice of the PWM carrier frequency (COSR) has a severe impact. E.g. theoretically, an ideal performance is achieved by uniformly sampled synchronous PWM when COSR is an integer. However, with a suitable choice of COSR and OSR, also useful ADCs can be built with other PWM variants.



Figure 9. FFT of x[n] in PWM-VCO at a COSR of 0.44 (a) and a COSR of 0.0625, (b).

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