Efficient Optimization of the Integrity Behavior of Analog Nonlinear Devices Using Surrogate Models

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Abstract

A novel technique to analyze and optimize the integrity behavior of nonlinear analog devices in the presence of noise is proposed. The technique leverages surrogate models, as such reducing the simulation time, avoiding time-consuming and expensive measurements after tape-out and hiding the original netlist of the circuit, while maintaining high accuracy. Easy integration of the surrogates into a circuit simulator together with pertinent subcircuits representing, e.g., board and package, allows mimicking the integrity behavior of a complete setup while still being in the design phase. In this contribution, the method is applied to a case study, being a voltage regulator designed for automotive applications.

Introduction

In modern microelectronic design it is essential to quickly and accurately predict the behavior of the novel circuits in the early stage of the design cycle. This allows assessment of the circuit before tape-out, thus significantly reducing the total production costs and time-to-market. Such an approach is often based on the construction of fast and reliable models that can efficiently reproduce the behavior of the designed circuit. In [1,2] successful techniques were presented, based on surrogate modeling. However, the focus was on modeling digital circuits, more specifically on the input/output buffers of integrated circuits (IC).

We propose a novel method to obtain behavioral models of nonlinear *analog* circuits that are typically susceptible to radio frequency (RF) noise. This noise can cause integrity issues. As our models consist of surrogates, they hide the intellectual property of the circuit manufacturer (i.e. the netlist), while still providing high accuracy. Additionally, they can be easily integrated into a typical SPICE environment and, most importantly, they can be evaluated rapidly, making them ideally suited for optimization purposes. The full methodology was first explained in [3] and is based on the construction of artificial neural networks (ANNs) [4] starting from Harmonic Balance simulations. In this contribution, this technique is briefly repeated for the case study of the optimization of the integrity behavior of a voltage regulator.

Case study

A voltage regulator (VR) is an electronic circuit that is commonly used in automotive industry, as it is able to provide a stable DC voltage. The power supply coming from a typical car battery may fluctuate due to, e.g., temperature changes or battery lifetime, therefore it can destabilize and cause malfunctioning of the electronic circuits of the vehicle. To avoid this situation VRs are used to convert the unstable $V_{in,DC}$ battery voltage to a constant $V_{out,DC}$ (Fig. 1). However, it is well-known that VRs are susceptible to noise at their DC supply pin. The noise can cause changes or fluctuations of the output voltage again, corrupting the power integrity of the electronic circuits depending on the VR. This situation is schematically presented in Fig. 1, w RF noise.

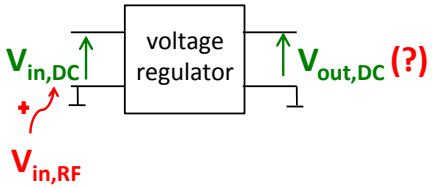

Figure 1: Principle schematic of the voltage regulator function.

It is thus very important to correctly predict the functioning of the VR, especially when subjected to RF noise, and to optimize the design if necessary. Therefore, for our case study we investigate a highly nonlinear automotive voltage regulator designed by Melexis Technologies N.V., Belgium. This novel IC, which has not even been taped-out yet, is called MLXTC883 and its netlist consists of integrated active and nonlinear components, i.e. 21 transistors and 123 passive components (resistors and capacitors). The VR MLXTC883 is designed to receive a 5 V DC supply, which it converts into a stable 3.3 V DC voltage at the output. A deviation of ± 100 mV from this 3.3 V is allowed for its intended automotive application.

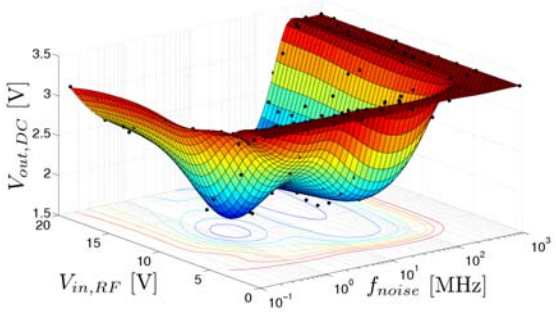

Figure 2: Output voltage drop for the voltage regulator subjected to RF noise: $V_{out,DC}(f_{noise}, V_{in,RF})$

To investigate the reliability of the VR, its original netlist was imported into Agilent's Advanced Design System (ADS) and Harmonic Balance (HB) simulations were performed. The behavior of the VR, in terms of its DC output voltage $V_{out,DC}$, was observed whilst being subjected to RF noise with frequency f_{noise} and amplitude $V_{in,RF}$. From Fig. 2 it is seen that the VR is indeed susceptible to noise, as the desired 3.3 V output voltage drops to a much lower value for a large range of the noise frequencies when the noise amplitude is sufficiently high. This

behavior can cause power integrity problems. It is also interesting to notice that at high frequencies ($f_{noise} > 300$ MHz), the VR is not much affected. This is thanks to the low-pass behavior of the input stages of the VR.

Surrogate Modeling

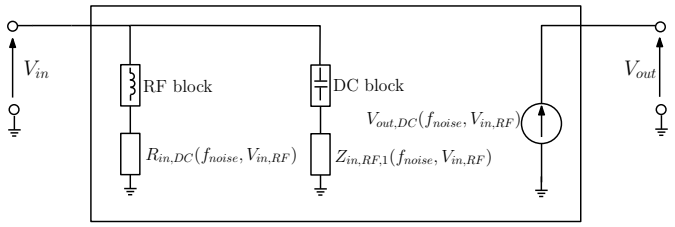

Figure 3: Architecture of the voltage regulator's behavioral model, illustrating the pertinent components (building blocks).

To model the behavior of the investigated VR, we propose the model architecture as depicted in Fig. 3. The signal V_{in} at the input consists of a DC component, being the DC supply $V_{in,DC}$, and an RF component, i.e. RF noise at frequency f_{noise} and amplitude $V_{in,RF}$. The model contains three crucial building blocks that describe the functioning of the VR in the presence of this RF noise. The two components $R_{in,DC}$ and $Z_{in,RF,1}$ depict the input impedances for the DC and noise, respectively. A third block $V_{out,DC}$ describes the DC output voltage. It is safe to only consider the DC behavior at the output, as the VR behaves as a low-pass filter, suppressing the presence of RF signals at the output. Also, an output impedance is not included in the model, as the output pin is considered to be open, due to a typically highly-impedant load connected to it in its intended automotive application. These three building blocks $R_{in,DC}$, $Z_{in,RF,1}$ and $V_{out,DC}$, fully capture the behavior of the VR, and all three depend on two parameters, i.e., the frequency and amplitude of the noise (for the block $V_{out,DC}$ this was already demonstrated in Fig. 2). The validity of this architecture will be clearly demonstrated *a posteriori* in the next part of this paper.

To reduce the simulation time and to conceal the intellectual property of the VR manufacturer, the three aforementioned building blocks $R_{in,DC}$, $Z_{in,RF,1}$ and $V_{out,DC}$ of the proposed model architecture are substituted with surrogates, allowing us to efficiently mimic the behavior of the circuit while still maintaining good accuracy. The construction of these three surrogates requires a careful choice of many modeling parameters, such as surrogate type, sampling scheme and number of selected samples, type of measure and applied error function, etc. [5]. These choices will now be discussed in detail.

For the considered case study, ANNs are selected as a surrogate type, as they are more suitable to model highly nonlinear functions than, for example, Kriging based models [4]. These latter would fail to accurately model the transition region where $V_{out,DC}$ starts to drop to a value lower than 3.3 V (see Fig. 2). Additionally, the construction of ANNs requires far less samples compared to classic interpolation methods. A five-fold cross-validation measure is used to assess the accuracy of the surrogates. Cross-validation temporarily re-trains a surrogate several times using different subsets of data (called folds) and assigns an error to each fold using an error criterion. The final accuracy is then obtained by calculating the mean error over all folds. Here, the desired final accuracy error is set to $3 \cdot 10^{-3}$ for the surrogates of all three components, which is sufficiently low for our needs. The error criterion, used to estimate the error of each fold, is calculated as follows:

$$error_{fold} = \sum_{i=1}^{N_{fold}} w_i (s_i - s_{model,i})^2. \tag{1}$$

In this equation, N_{fold} is the number of samples in a particular fold. Variable s_i is the i-th sample value of either $V_{out,DC}$, $R_{in,DC}$ or $Z_{in,RF,1}$ (depending on the surrogate that is being modeled), obtained by a HB simulation that was performed using the original netlist of the voltage regulator for a carefully chosen tuple $(f_{noise}, V_{in,RF})$. Below we give a detailed explanation of the adaptive sampling algorithm used to select the sample tuples. Variable $s_{model,i}$ represents the value of either $V_{out,DC}$, $R_{in,DC}$ or $Z_{in,RF,1}$ returned by the constructed surrogate for the same sample tuple $(f_{noise}, V_{in,RF})$. The weighting factor w_i is assigned to the samples according to the rule:

$$w_i = \begin{cases} 10\,, & |3.3\text{ V} - s_i| \leq 0.15\text{ V} \\ 2\,, & 0.15\text{ V} < |3.3\text{ V} - s_i| \leq 0.5\text{ V} \\ 1\,, & 0.5\text{ V} < |3.3\text{ V} - s_i| \leq 1\text{ V} \\ 0.1\,, & 1\text{ V} < |3.3\text{ V} - s_i| \end{cases} \tag{2}$$

where 3.3 V is the intended value of $V_{out,DC}$, i.e., when the VR works properly in the absence of RF noise. By applying this kind of weighting (2), the modeling process focusses mainly on the acceptable margin of ± 100 mV around 3.3 V, where the circuit is still considered as functioning correctly. Less attention is paid to regions where $V_{out,DC}$ really differs from 3.3 V, i.e. where the circuit fails badly anyway. In this way, the total construction time of all surrogates is kept low, while still providing enough accuracy where it is most necessary. To obtain the initial surrogates, data samples are collected using a Latin Hypercube Design (LHD). Thereto, the design space is partitioned into an equal number of columns and rows and the samples are selected in such way that in each column and each row only one sample resides. Consequently, the samples that are used to construct the initial surrogates efficiently cover the complete design space. However, to provide high accuracy of the modeled surrogates, more dense sampling is needed. To achieve that, a highly adaptive Lola-Voronoi algorithm [6] is employed to select extra samples, which are used to update the surrogates. The Lola (Local Linear Approximation) component of this sample selector investigates the linearity of the modeled function. If a nonlinear region of the design space is detected, Lola selects a higher number of samples in this region, ensuring high accuracy of the model. Furthermore, in order not to leave large areas of the design space undersampled, Voronoi tessellation is applied to provide sufficiently dense sampling in the complete design space.

Results

To validate the model, we will now study the influence of RF noise on the circuit using both the original netlist of the VR and the constructed behavioral model presented in Fig. 3. To

perform this validation under standardized condition, we follow the instructions of the International Electrotechnical Commission concerning the 62132-4 direct power injection (DPI) test [7]. Here, of course, we will mimic this test via simulations. First, we briefly describe how the DPI test for ICs is performed (Fig. 4). The IC, here being the VR, should be placed on a dedicated printed circuit board (PCB), together with all the components necessary for its proper functioning. Via a bias tee, sinusoidal RF noise is injected into the DC supply pin. The performance of the VR is observed, here by monitoring the output voltage delivered to a decoupling network with a very high impedance, represented by R. The power of the RF noise is varied between 0 dBm and 30 dBm and its frequency is swept from 150 kHz to 1 GHz. The maximal power levels at which the VR still operates correctly, i.e. when $V_{out,DC}$ varies within ± 100 mV from the desired 3.3 V value, are recorded. Only if the VR can withstand 30 dBm of RF noise over the complete frequency range, it passes the test. Otherwise, additional precautions, such as for example decoupling capacitors C_d or ferrite beads, must be added to improve the behavior of the VR.

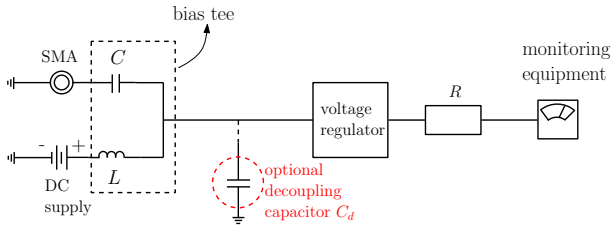

Figure 4: Schematic configuration of the DPI test set-up

VR subjected to the DPI test

In our first validation we integrate the model architecture (Fig. 3) into Agilent's ADS circuit simulator and replace the components $R_{in,DC}$, $Z_{in,RF,1}$ and $V_{out,DC}$ by their surrogates. This is a straightforward operation, as these three surrogates, i.e. the ANNs, are merely mathematical expressions. Next, following the instructions given in [7], we construct a simulation set-up that allows us to predict the results of the DPI test. The schematic of the DPI test is presented in Fig. 5. The VR (its original netlist or the behavioral model) is connected to 1 nH inductors, which represent here a simplified model of the package. The effect of the PCB is included by adopting the EM/circuit co-simulation technique given in [8]. Following this method, the pertinent scattering parameters of the unpopulated PCB are analyzed, using full-wave simulation of ADS-Momentum, and these are later on imported into the circuit solver, where they are combined with the model of the packaged VR and the required lumped elements. The bias tee comprises a DC blocking capacitor AVX Z5U 08055E223MAT2A with a nominal value $C = 22$ nF and a DC feeding inductor (Ferroperm Type 1583 RF choke) with a nominal value $L = 47$ μH. The choice of these real lumped components, which include also parasitic effects, is carefully made, as advised in [8], so that the requirements concerning the proper RF injection path given in [7] are fulfilled. The VR receives the 5V DC supply from a DC voltage source with a DC supply ca-

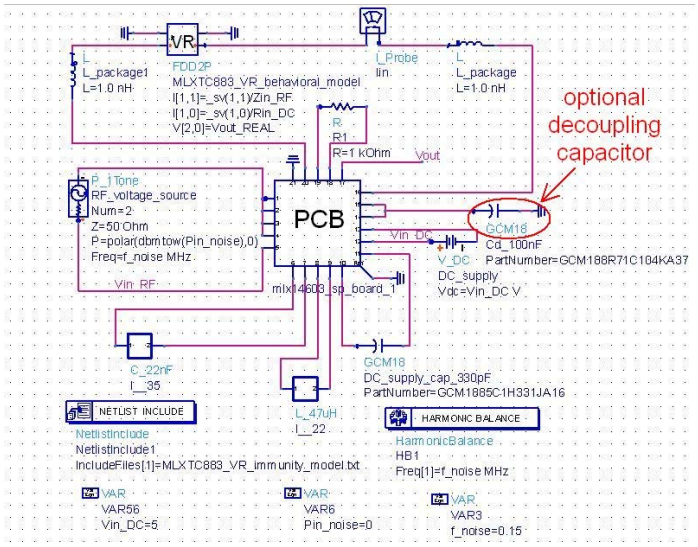

Figure 5: Implementation of the DPI test set-up into ADS

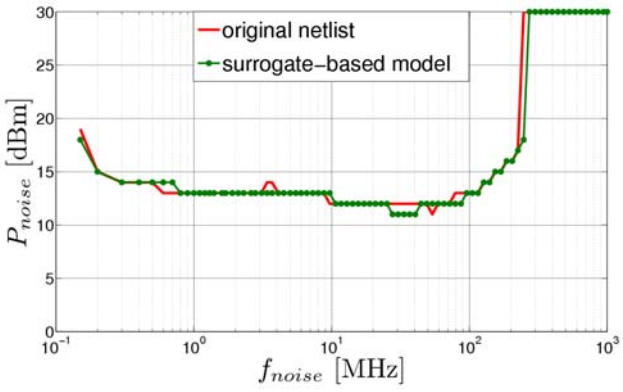

Figure 6: Comparison of the DPI test results of the original circuit and the surrogate-based behavioral model.

pacitor GCM1885C1H331JA16 of 330pF, and the RF noise is generated by an RF voltage source. A resistor of $1k\Omega$, mimicking the required decoupling network R, is used to monitor the behavior of the IC, more specifically its DC output voltage.

Fig. 6 depicts the results of a simulated DPI test using both the original netlist (red line) and the surrogate-based model (green line with circles). The plotted curves represent the maximum value of the RF noise power P_{noise} (in dBm) that the investigated VR can withstand while $V_{out,DC}$ still remains within acceptable ± 100 mV margin, i.e. $V_{out,DC} \in [3.2\text{V}, 3.4\text{V}]$. The obtained results show excellent agreement over the complete frequency range of the simulated DPI test. According to the original netlist, at 150 kHz the IC withstands 19 dBm and still functions correctly, while 18 dBm is returned by the behavioral model as a maximal value of the RF noise that does not cause malfunctioning of the VR. For the large frequency range from 500 kHz till 100 MHz, according to both set-ups, this value decreases to less than 14 dBm. For frequencies higher than 300 MHz, the IC fully passes the DPI test, as it is capable to withstand 30 dBm of RF noise. The simulation time of this test, using the original netlist, equals 2913.8 s, whereas the time

needed to run this test when using the surrogate-based model is 32.6 s. Therefore, by applying the proposed behavioral model, a significant speed-up factor of 90 is obtained.

Optimization of integrity behavior

It was confirmed in the previous section that the behavioral model can be used to accurately predict the integrity issues caused by the VR when it is subjected to RF noise. Now we use our surrogate-based model to demonstrate how to improve this behavior of the VR. Initially, an extra, often used, decoupling capacitor GCM188R71E682KA37 of 6.8 nF is added at the input pin (Figs. 4 and 5) to protect the VR by leading the unwanted RF signal to ground, and the DPI test simulations are repeated, using again the original netlist and the behavioral model. Fig. 7 depicts a very good agreement between both results, which together show that this decoupling capacitor C_d leads to an improvement of the integrity behavior but it is not sufficient to cover the entire frequency range. Therefore, an optimal value of the decoupling capacitor needs to be found. Via optimization and using the behavioral model, it is assessed that a capacitor of 84 nF is sufficient to satisfy our goal. A similar optimization, using the original netlist indicates an optimal value of 79 nF. Taking the typical manufacturing tolerances of a real capacitor ($\pm 10\%$) into account, we finally decide to use the 100 nF capacitor GCM188R71C104KA37. Repeated simulations of the DPI test prove that now, in both cases, the DPI test is fully passed (Fig. 7). It is important to mention that the total time needed to find the optimal capacitor using the original VR netlist is 7427 s while the optimization using the behavioral model only took 65 s, resulting in an impressive speed-up factor of 114. This result clearly demonstrates the usefulness of the proposed behavioral model in the optimization process.

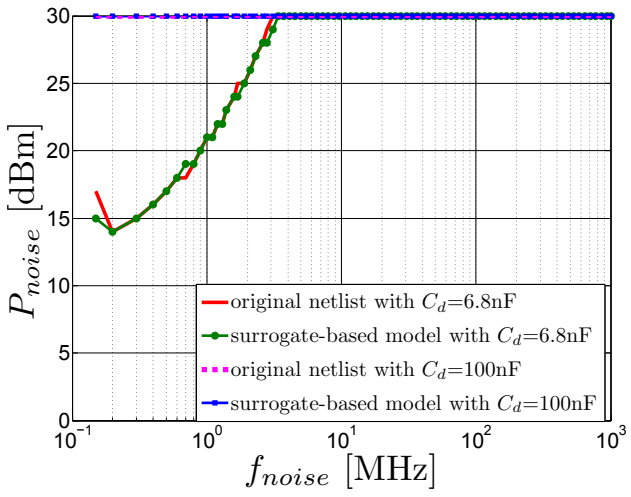

Figure 7: Comparison of the DPI test results of the original circuit and the surrogate-based behavioral model with additional decoupling capacitors.

Conclusion

A novel modeling approach has been proposed that enables the analysis and optimization of the integrity behavior of a nonlinear analog device subjected to RF noise. Compact size ANN surrogates employed in this method conceal the intellectual property of the manufacturer and considerably expedite the simulation process while keeping the modeling accuracy high, thus making this technique suitable for optimization purposes.

An industrial case study of a nonlinear analog VR confirmed that the obtained behavioral model can be quickly integrated into a circuit solver and used to predict, in the early design stage, the behavior of the circuit, e.g. during a standardized DPI test. The technique was validated by means of comparison with the original netlist, showing excellent accuracy and far shorter simulation time. Thanks to this speed-up factor of about 100, an optimal solution to improve the integrity behavior of the IC was efficiently found.

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