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PERFORMANCE OF ELECTRONIC DISPERSION COMPENSATOR FOR 10-GB/S MULTIMODE FIBER LINKS

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ABSTRACT

In high-speed optical links, electronic compensation circuits can be utilized to greatly improve the data transmission performance limited by fiber dispersion. In this paper, we develop a full link model, including multimode fibers, optical/electronics/optical components, clock-and-data recovery and electronic compensation circuits. The performance of various electronic compensation techniques, such as feed-forward equalizer and decision feedback equalizer for optical multimode fiber is investigated and numerically evaluated. Finally, a comparison of the performance of each compensation techniques and a proposal of optimal equalizer circuit implementation, achieving a 10-Gb/s transmission over 1-km standard multimode fiber are presented.

INTRODUCTION

Multimode fiber (MMF) has become more promising and competitive alternative for high throughput short distance communications due to a burgeoning increase in the number and size of local area networks and data centers. Whereas the inter-symbol interference (ISI) introduced by signal pulse broadening due to fiber dispersion limits the transmission speed and distance of optical fiber links. In such links, the ISI dominates the power penalty in the link power budget as it increases exponentially with the fiber reach [1].

Electronic dispersion compensation (EDC) has been successfully deployed in wireline and wireless channels to mitigate the effects of ISI for decades, which has the advantages of lower cost, more adaptability and higher robustness over optical compensation. Two widely adopted EDC schemes are linear equalizer (LE) and decision feedback equalizer (DFE). The performances and comparisons of electronic equalization techniques in long-haul single mode fiber systems have been well documented in [2, 3]. However, few documents have contributed to a thorough performance demonstration of various equalizers in multimode fiber links.

In this paper, we presented 10-Gb/s simulations, exploited the feasible diversity showing performances of LE and DFE in MMF links. In order to maximize the achievable serial multimode fiber transmission distance, efficient equalizer configuration was investigated in terms of performance against implementation complexity. The system link model proposed can be extended to higher data rate systems as 25-Gb/s and 40-Gb/s.

SYSTEM LINK MODEL

Fig. 1 shows the considered MMF communication system model. A 10-Gb/s nonreturn-to-zero (NRZ) pseudorandom binary sequence (PRBS) of length $2^9 - 1$ is used as transmitted signal, driving a vertical cavity surface

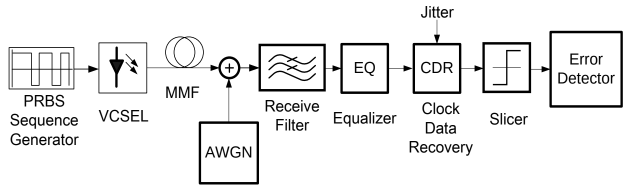


Figure 1: MMF fiber link simulation block diagram

emitting laser (VCSEL) using direct modulation. The exhaustive set of electrical and optical data of a commercial GaAs VCSEL for fitting the model was presented in [4]. We use the equivalent electrical parasitic model shown in Fig. 2 to represent the VCSEL. A diode junction model of R_j and C_j , along with parasitic capacitance C_p for the bond pad and parasitic resistance R_p, R_s associated with the package and the distributed Bragg reflector (DBR) mirrors are necessary to provide a complete description of the laser. The receiver-end filter is modeled by a fourth order Bessel low pass filter with bandwidth of 0.75 times the bit rate. The shaped NRZ signal propagates through the linear dispersive optical fiber characterized by the following Gaussian impulse response as in [5]:

$$h(t) = \frac{1}{\sqrt{2\pi}\,aT} exp[-t^2/(2(aT)^2] \qquad (1)$$

The corresponding frequency response is:

$$H(f) = exp[-(2\pi aTf)^2/2] \qquad (2)$$

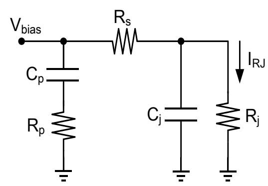


Figure 2: VCSEL electrical equivalent circuit

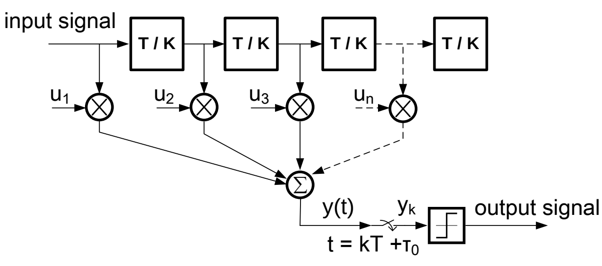
The described MMF fiber channel has a 3-dB bandwidth of $f_{3\,dB} = \frac{0.1329}{aT}$. Various channel bandwidth can be achieved through changing a for the given baud time T = 100 ps. Therefore, we can give rough estimation of the fiber reach in conjunction with the modal bandwidth. Equalization is performed on the incoming signal corrupted by additive Gaussian noise (AWGN) from the channel and timing jitter from the clock recovery circuit (CDR). The bit error rate (BER) is calculated by an error detector at the output of the link.

EQUALIZER ARCHITECTURES

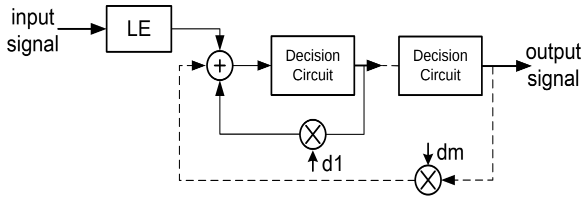
The architecture of the DFE is shown in Fig. 2(b) which generally consists of a feed-forward filter or LE that can remove the pre-cursor ISI and a feedback filter to cancel post-cursor ISI. The tapped delay line structure of LE is depicted in Fig. 2(a) while the DFE works by subtracting a proportion of previous decisions from the output signal of LE. The output of the DFE can be expressed as:

$$\hat{s}(t) = \sum_{i=1}^{n} u_i \cdot x(t - [i \cdot \Delta t1]) - \sum_{i=1}^{m} d_m \cdot \hat{s}(t - [i \cdot \Delta t2]) \qquad (3)$$

where the first item on the right of equal sign is related to the expression of LE, u_i is the variable tap weight, n is the number of feed-forward taps and x(t) is the input signal. The second item is corresponding to the feedback taps with variables have similar physical meanings to the first item except for $\hat{s}(t)$ represents the decision of past symbol. Δt is the time delay between two adjacent equalizer taps. Typically, the time delay for LE is a fraction of bit period with ratio $K = \Delta t / T$ referred as oversampling rate, such equalizer is known as fractional spaced equalizer (FSE) and K = 1 as the feed-forward equalizer (FFE) or baud spaced equalizer while for the feedback taps the time delay is always baud time. The least mean square (LMS) algorithm is adopted to optimize the tap weights of the equalizer. The optimal decision instant t can be distorted by the timing jitter τ_0 of the CDR circuit, thus affecting the equalization performance.



(a)



(b)

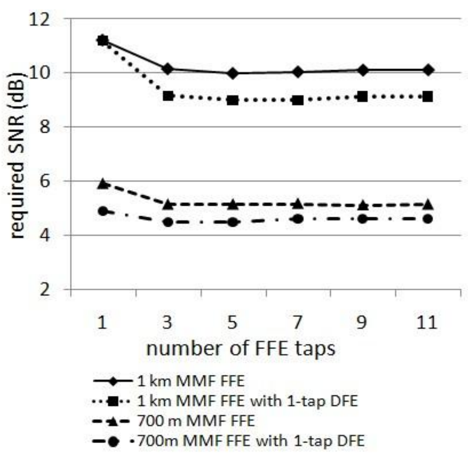
Figure 3: equalizer architectures:(a)LE (b)DFE

The feedback filter utilizes the past decision signal to ameliorate the effect of current symbol on the following symbols therefore enabling post-cursor ISI compensation without the noise enhancement associated with LEs [6]. But the DFE has an impairment of error propagation caused by incorrect decision feedback to the feedback filter. Though adding the feedback tap will dramatically improve the link performance compared to increase the number of feed-forward ones, usually one feedback tap is chosen due to the tight timing budget and high power consumption in circuit implementation.

In spite of the disadvantage of larger chip area, continuous-time analog implementation of equalizer outperforms its digital counterparts in eliminating the complex and power-hungry high speed ADC front end for MMF links. Low-complexity, power-efficient analog electronic equalizer configurations are investigated to extend the fiber reach.

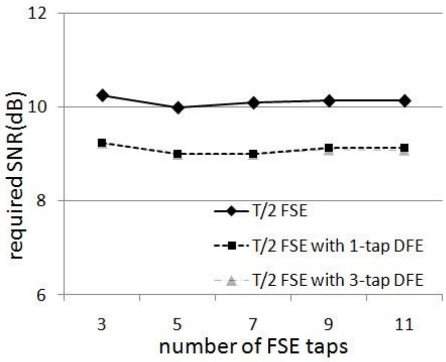
PERFORMANCE AND DISCUSSION

Simulations of various equalizer configurations have been carried out to optimize the future circuit design. To give numerical and visual analysis of the foregoing fiber link quality, we assumed odd-tap LE for the symmetric dispersed signal and focused on the BER and eye diagram simulations. Due to the time-consuming Monte Carlo simulations, we chose 10^{-6} BER sensitivity as performance reference for the modeled links. Fig. 4 (a) shows the effect of changing the number of FFE taps for 700-m and 1-km



(a)

MMF channel. No significant enhancement can be achieved increasing the number of FFE taps from 3 to 11. Whereas, there are approximately 1-dB and 0.6-dB sensitivity improvement for 1-km and 700-m channel separately combining the FFE with 1-tap DFE . As you can see in Fig. 4(b), when the number of taps was added, the T/2 FSE performed at least as good as FFE, not necessarily with the same total time span, in other words, no need doubling the number of taps. The simulation results also showed that equalizer with more taps did not always outperform a shorter one because the gradient noise is proportional to the length of equalizer.



(b)

Figure 4: simulated SNR sensitivity (10^{-6} BER) for various LE and DFE configurations

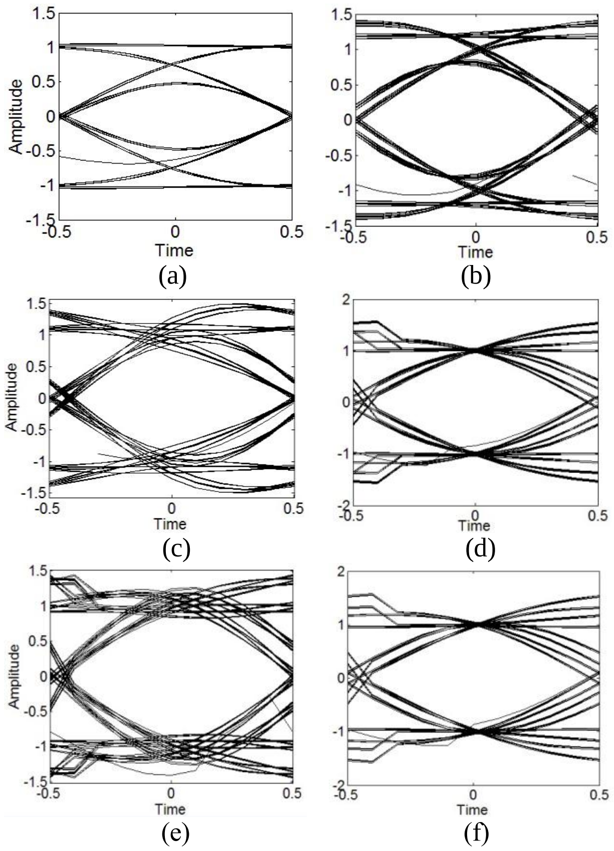


Figure 5: eye diagrams for 700-m MMF link under various equalization schemes:
(a) uncompensated (b) 3-tap FFE (c) 5-tap FSE (d) 3-tap FFE + 1-tap DFE (e) 5-tap FSE + 1-tap DFE (f) 3-tap FFE + 3-tap DFE

Fig. 5 shows the eye diagrams after 700-m MMF link under different equalization schemes. It was obvious that the FSE provided more independence from phase distorted channels [5].In all these simulations, using more than one tap DFE did not improve the performance apparently. A five tap T/2 spaced FSE connected with one tap DFE is superior to a three tap FFE combined with one tap DFE taking link performance and implementation complexity into account.

CONCLUSION

The transmission distance feasibilities of 10-Gb/s multimode fiber under different equalization schemes are reported. Simulations predict that five tap FSE combined with one tap DFE is the optimum configuration against ISI, additive noise and timing jitter under given system settings. The simulation result is of great significance for cost-effective equalizer design in high speed optical links.

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