# A Digitally Controlled Threshold Adjustment Circuit in a 0.13$\mu$m SiGe BiCMOS Technology for Receiving Multilevel Signals up to 80Gbps

Timothy De Keulenaer
Ghent University,
INTEC/IMEC
Ghent, Belgium
Email: timothy.dekeulenaer@intec.ugent.be

Guy Torfs
Ghent University,
INTEC/IMEC
Ghent, Belgium

Ramses Pierco,
Johan Bauwelinck
Ghent University,
INTEC/IMEC
Ghent, Belgium

***Abstract*—In this paper, a high bandwidth digitally controlled threshold adjustment circuit is proposed which can be used for demodulating high-speed multi-level signals. Simulations of the bandwidth are presented together with measurements of the control currents to indicate the threshold adjustment capability. A bandwidth above 80GHz in a 0.13$\mu$m SiGe BiCMOS technology and a threshold tunable between $\pm$160mV in steps of 0.6mV is achieved, allowing very precise control of the threshold level. This allows the circuit to accurately position the threshold on the eye-crossing of a high speed multi-level signals. By applying this circuit to demodulate a duobinary signal over a 40GHz channel, a data rate of up to 80Gbps can be achieved.**

## I. Introduction

Advances in the data rate of modern communication systems has lead to the need for an increase in speed of inter-chip communication. Typically, a non-return-to-zero (NRZ) signal is transmitted over a PCB transmission line (microstrip, grounded coplanar waveguide), but, with rising speed, the limited bandwidth of the channel (the transmission line) and the maximum bandwidth that can be achieved by the chip technology (indicated by the maximum transition frequency $f_t$) impose a limitation on the maximum data rate. To counter this limitation, multi-level signalling such as PAM-4 or duobinary have been used in recent papers [1]–[3] to demonstrate data-rates up to 25Gbps across electrical backplanes.
However, although more advanced modulation schemes require less bandwidth, the processing needed on both the transmitting and the receiving chip significantly increases. Among others, a threshold adjustment circuit (TAC) operating at high speed is needed at the receiving end to seperate different symbol levels. This paper presents a 80GHz TAC designed in a 0.13$\mu$m SiGe BiCMOS technology using a current DAC for threshold adjustment. The large bandwidth and the fine threshold control of the presented circuit allows duobinary transmission up to 80Gbps when signalling over a 40GHz channel.
The structure of this paper is the following: in Section II the topology of a standard non-clocked duobinary receiver is discussed, Section III presents the circuit that is used to achieve a high speed threshold adjustment, the DACs used in the control of the threshold level are shown in Section IV, Section V discusses the fabrication of the chip and further work that has to be done and Section VI summarizes the results and concludes this paper.

978-1-4799-4994-6/14/$31.00 ©2014 IEEE

## II. Non-clocked duobinary receiver

One of the more promising modulation schemes to reduce the required channel bandwidth without adding too much chip complexity is the duobinary scheme discussed in [4]. A receiver structure as well as the typical 3-level eyediagram of this modulation scheme is shown in Fig.1. Due to the high speeds, a fully differential channel is needed, although, for simplicity, only the single-ended signaling is drawn. The wideband input amplifier needs a bandwidth comparable to the channel bandwidth, for a 80Gbps duobinary transmission this corresponds to approximately 40GHz. An input buffer achieving this performance is shown in [5]. After the input buffer, the signal is split and compared with both a lower and an upper threshold voltages. To do this comparison, the differential signal is first shifted using a TAC. This will position the zero level of the signal in the middle of the lower and upper eye respectively. This signal is then applied to a limitting amplifier stage which regenerates a signal with digital levels, i.e. logic high and logic low above and below the threshold respectively, necessary for the XNOR gate, which will demodulate the duobinary signal.

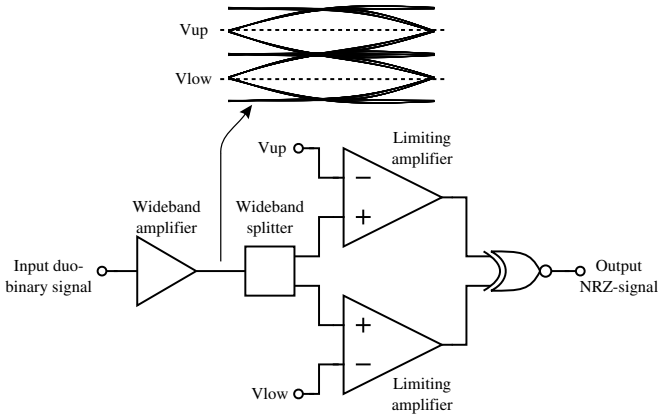


Fig. 1. Standard non-clocked duobinary receiver as described in [4].

## III. Emitter follower threshold adjustment circuit

The TAC, as shown in Fig.2 consists of two distinct parts: an emitter follower with threshold adjustment, and a cascoded output driver. Both circuits will be discussed in greater detail in the following sections.

### A. Emitter follower threshold adjustment

The input of the TAC uses emitter followers (EF), shown as transistors $Q_0$ and $Q_1$ in Fig.2. The transistors are biased with a constant current of 3.2mA, which is optimized for maximal bandwith (max $f_t$ biasing). The use of EFs has two main benefits: Firstly, they provide a low output impedance, and as a result allow for a higher bandwidth when driving the capacitive input of the cascoded output stage. Secondly, the voltage relationship between base (fixed at 2.4V DC by the wideband input amplifier) and emitter (given the constant emitter current) is fixed. This results in an equal DC voltage at the emitters of transistors $Q_0$ and $Q_1$. To introduce a shift in DC voltage, and hence in threshold, a series resistor ($R_0$ and $R_1$) is added between the output of the EFs and the input of the cascoded output stage. The biasing current of the EF is split into two parts, one directly connected to the emitter, one connected through this series resistor. By changing the ratio of these two current sources (varying $\alpha$ between 0mA - 1.3mA), the amount of current flowing through the resistor and hence the DC level at the input of the next stage can be controlled. By varying the DC voltage of the positive and negative input in the opposite direction, the threshold can be adjusted.

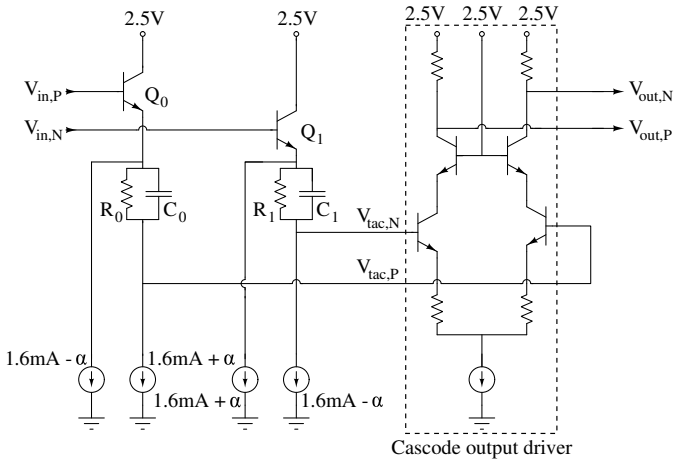


Fig. 2. Threshold adjustment circuit consisting of emitter followers biased with a constant current and the cascade output driver. The threshold level is adjusted by means of $\alpha$ ranging from 0mA - 1.3mA.

Furthermore, capacitors $C_0$, $C_1$ are added in parallel with resistors $R_0$,$R_1$ in Fig.2. This provides a low impedance path at higher frequencies between the output of the emitter followers and the input of the cascode, and hence, increase the bandwith. The capacitors used in this circuit are metal-insulator-metal (MIM) capacitors with their bottom plate connected to the emitter of the EFs and their top plate connected to the input of the cascode output driver. This reduces the parasitic capacitance at the input of the cascoded amplifier and increases the bandwidth. The use of this topology leads to shifting of signals with a bandwidth of more than 80GHz as shown in the post layout simulation results of Fig.3. The variation on the bandwidth is less than 5% across the whole shifting range. The shifting resistors $R_0$ and $R_1$ have a value of 80Ω in this design. The following trade-off exists: larger values give a larger maximum threshold adjustment but a smaller resolution and the need for a higher bypass capacitance while smaller values mainly deteriorate the maximum threshold varation. Parallel with these 80Ω resistors a 1pF MIM capacitor was implemented.

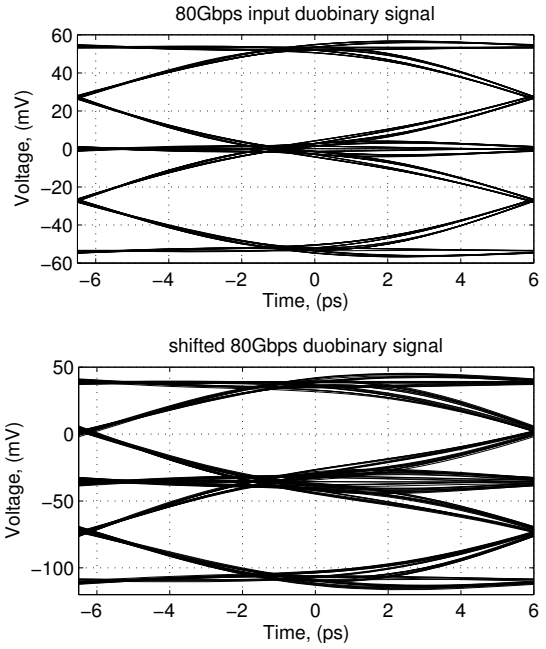


Fig. 3. Input eye-diagram of a 80Gbps duobinary input signal together with the eye-diagram of the shifted version at the output of the threshold adjustment circuit.

The current mirrors providing the current to the EFs are implemented as cascoded current mirrors to reduce the effect of the varying collector voltages of the mirror transistor. This allows us to have a current resolution of less than 5$\mu$A resulting in a voltage shifting resolution of less than 1mV.

### B. Cascoded output driver

The switching output driver of which the threshold is adjusted, consists of a degenerated differential cascode as shown in Fig.2. By using a cascode, the miller capacitance at the input can be diminished [6] and the maximally allowed voltage swing at the output is higher since the peak voltage at the collector of a common base stage can go up to $BV_{CBO}$ [7], [8]. Feedback by means of resistive degeneration is applied to increase the bandwidth of the circuit by trading in gain. Furthermore, it makes the cascode less sensitive to differences in DC-voltage at the input which limits the accuracy that is needed for the TAC. The biasing of the cascode is such that the transistors achieve their maximum $f_t$. The load resistor is a 80Ω poly resistor chosen to allow enough bandwidth when loaded with the input capacitance of the next stage. The tail current is 5mA.

In Fig.3 the output eye-diagram shows a zero-volt level that corresponds to the eye-crossing of the upper duobinary eye.

By adding a limiting amplifier to this output the wanted NRZ-signal for the upper half of the duobinary signal is obtained.

### C. Bandwidth and linearity

In Fig.4 the gain and the input referred 1dB compression point are simulated in function of the frequency. The -3dB bandwidth of the circuit is above 80GHz, to ensure that the level shifting stage will not limit the bandwidth in a 80Gbps data system. The simulated input referred 1dB compression point is around -4dBm.

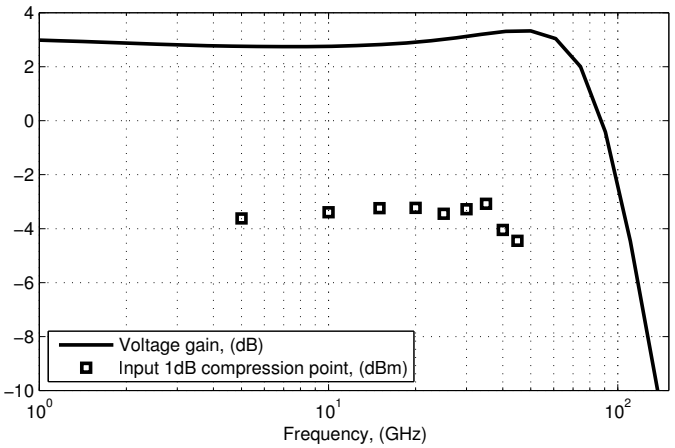


Fig. 4. Post layout simulation results for the voltage gain and input referred 1dB compression point of the TAC in function of the frequency.

The 1dB compression point was simulated by driving the power in a 50Ω input buffer connected in front of the TAC and measuring the input power of the TAC and the output power of the TAC. Since the linearity of the input buffer is greater than the linarity of the TAC this is a valid measure for the linearity. At higher frequencies it is no longer possible to include a sufficient number of harmonics in the simulation, which leads to a lower simulated 1dB compression point, as can be noticed from the two rightmost 1dB compression points in Fig.4. Verification of the linearity at high frequencies was subsequentially done by checking the in- and output diagram at different input power levels.

## IV. Digitally Controlled Current DACs

The circuit used to generate the currents for the EFs is shown in Fig.5, both currents are derived from one variable current source $I_{var}$. This source is implemented as a traditional binary weighted current mirror with switchable gates to control the total current. The variable current is mirrored and amplified five times. This amplification allows to reduce the current in the DAC as well as the area consumed by the DAC. However, care has to be taken to meet the matching requirements for the 7 bit DAC resolution used in this design.
In a second stage the amplified variable current is added and substracted from a constant current source $I_0$. Using this technique the current through the EFs will always be two times $I_0$. The last stage of the current generator is the implementation of a switch which allows to change the shifting direction.
Measurements on the fabricated die showed that the current

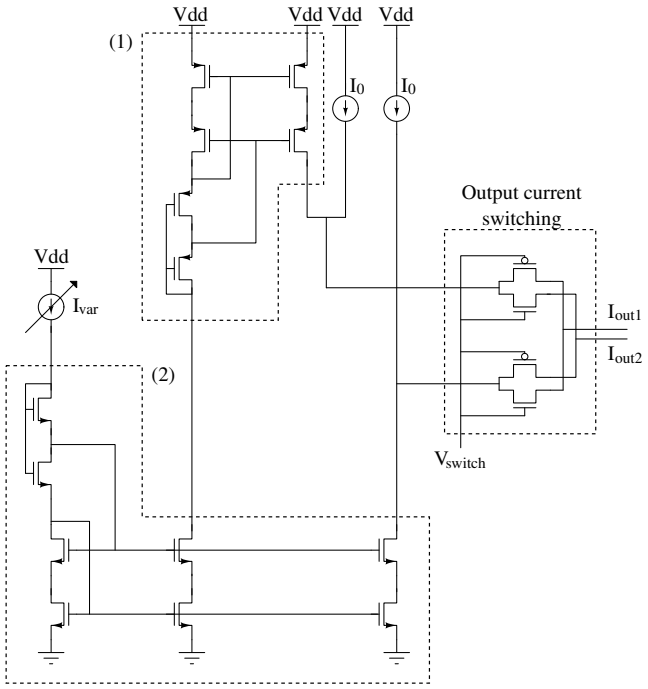


Fig. 5. Circuit used to generate complementary output currents $I_{out1}$ and $I_{out2}$ from the DAC current $I_{var}$. Sooch cascode current mirrors, subcircuits (1) and (2), are used to get accurate copies of the DAC current. The digital signal $V_{switch}$ interchanges the output currents.

switching circuit has a minimum of 263$\mu$A and a maximum of 1.26mA, variable in steps of 4$\mu$A. Taking into account the 80Ω resistor that converts this current into the level shifting voltage and the times two multiplication in the EF current mirrors, we can shift the level 160mV up or down in steps of 0.64mV. The current running through the EFs is constant around 3mA.

## V. Fabrication and Further Work

A chip implementing the discussed threshold adjustment circuit has been fabricated in a 0.13$\mu$m SiGe BiCMOS technology with an $f_t$ beyond 200GHz. The part of the chip with the discussed circuit is shown in the micrograph of Fig.6. Although the proposed circuit can not be tested on its own, preliminary measurements show that an eye at the input can be shifted over the complete input range.

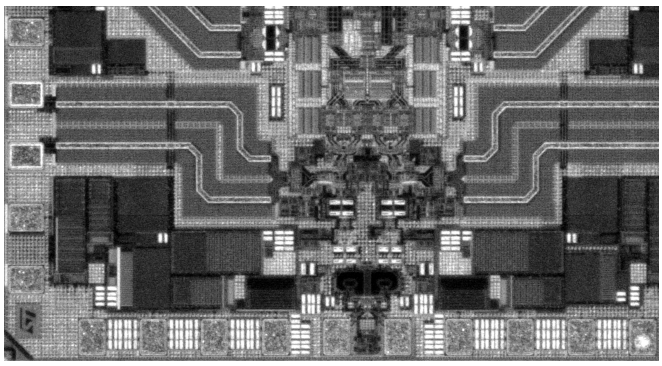

Fig. 6. Die micrograph of the TAC circuit.

Further testing of the chip implementing the discussed circuit, will include the reception and demodulation of a 80Gbps signal over a 40GHz channel. With improvement of the channel bandwidth even higher data rates should be attainable since the bandwidth of the TAC is as high as 80GHz. This means that with a sufficient bandwidth for the input buffer and the channel, a data rate up to 160Gbps becomes possible.

## VI. Conclusion and Results

In this paper a broadband threshold adjustment circuit capable of level shifting a duobinary data stream with a bandwidth up to 80GHz is presented. The threshold adjustment circuit can shift a differential input signal up or down by 160mV with a resolution of 0.64mV. It operates from a single 2.5V power supply, consumes only 35mW in a 130$\mu$m SiGe BiCMOS technology and still has an input referred 1dB compression point of approximately -4dBm. Using this circuit it is possible to demodulate a multitude of modulation schemes (e.g. duobinary, PAM-4) at high bandwidths allowing to achieve higher data rates over channels with limited bandwidth while keeping the added circuit complexity low.

## Acknowledgments

The authors would like to thank the Agency for Innovation by Science and Technology in Flanders (IWT) for supporting this work.

## References

[1] D. Correia, V. Shah, C. Chua, and P. Amleshi, "Performance comparison of different encoding schemes in backplane channel at 25gbps+," in *Electromagnetic Compatibility (EMC), 2013 IEEE International Symposium on*. IEEE, 2013, pp. 306–311.

[2] J. Lee, M.-S. Chen, and H.-D. Wang, "Design and comparison of three 20-gb/s backplane transceivers for duobinary, pam4, and nrz data," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 9, pp. 2120–2133, 2008.

[3] A. Adamiecki, M. Duelk, and J. Sinsky, "25 gbit/s electrical duobinary transmission over fr-4 backplanes," *Electronics Letters*, vol. 41, no. 14, pp. 826–827, 2005.

[4] J. H. Sinsky, M. Duelk, and A. Adamiecki, "High-speed electrical backplane transmission using duobinary signaling," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, no. 1, pp. 152–160, 2005.

[5] T. De Keulenaer, Y. Ban, Z. Li, and J. Bauwelinck, "Design of a 80 gbit/s sige bicmos fully differential input buffer for serial electrical communication," in *International Conference on Electronics, Circuits and Systems (ICECS-2012)*, 2012, pp. 237–239.

[6] E. Säckinger, *Broadband Circuits for Optical Fiber Communications*. New York, NY: John Wiley & Sons, 2005.

[7] H. Li, H.-M. Rein, T. Suttorp, and J. Böck, "Fully integrated SiGe VCOs with powerful output buffer for 77-GHz automotive radar systems and applications around 100 GHz," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1650–1658, Oct. 2004.

[8] M. Rickelt and H.-M. Rein, "Influence of impact-ionization induced instabilities on the maximum usable output voltage of Si bipolar transistors," *IEEE Trans. Electron Devices*, vol. 48, pp. 774–783, Apr. 2001.