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A 40 GBaud Integrated Silicon Coherent Receiver

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Abstract - *We present an ultra-compact and low-power silicon coherent receiver operating at 40 GBaud QPSK (80 Gb/s) and 16-QAM (160 Gb/s). The receiver consumes only 310 mW of power and realizes a factor 4 size reduction of the photonic integrated circuit compared to previously reported single-polarization silicon coherent receivers. This is the highest reported symbol rate for a silicon coherent receiver.*

Introduction

The growth of internet traffic has warranted a substantial amount of research towards high-speed transceivers for long-haul networks. Coherent communication provides multiple advantages over the classic OOK transmission schemes, including compensation of linear and non-linear fiber distortions and increased spectral efficiency thanks to phase-diversity and multilevel constellations (e.g. QPSK and 16-QAM) [1]. In the near future integrated coherent transceivers are expected to become key components in the metropolitan area networks, and in long-term even in access networks [2,3]. This will require a substantially reduction in size, cost and power consumption with respect to the current coherent transceivers. Silicon photonics emerges as an ideal platform to realize such devices. The high index contrast between Si and SiO_2 allows for devices with very small footprint and the circuits can be realized on large 200mm / 300mm wafers using existing commercial CMOS foundries allowing for low-cost chips. In this paper we present new results on the silicon integrated coherent receiver (ICR) presented in [4], operating at 40 GBaud for QPSK and 16-QAM.

Design and Setup

The ICR was fabricated in imec's iSiPP25G platform and hybridly integrated with a co-designed 2-channel transimpedance amplifier (TIA) array as shown in Fig.1(a). The photonic integrated circuit (PIC) is depicted in Fig. 1(b) and consists of a 2 grating couplers for the signal and local oscillator (LO), a 2x4 multi-mode-interferometer (2x4 MMI) acting as a 90° hybrid, and 2 pairs of balanced germanium photodetectors (Ge PDs) with an individual bandwidth of >50GHz. The TIAs were realized in a 0.13µm SiGe BiCMOS technology and optimized, aside from speed and power consumption, for linearity necessary for multilevel constellations as 16-QAM. The system performance was evaluated with the setup as shown in Fig 1(c). The in-fibre power was -8.5 dBm for the signal (QPSK/16-QAM) and +10.2 dBm for the LO. The fiber-to-chip grating couplers had an insertion loss of ~6.5 dB and a 1dB-bandwidth of 20nm.

Results

Fig. 1 (d) shows the BER performance of QPSK and 16-QAM at 28 GBaud and 40 GBaud. Operation below the hard-decision forward error coding (HD-FEC) threshold -

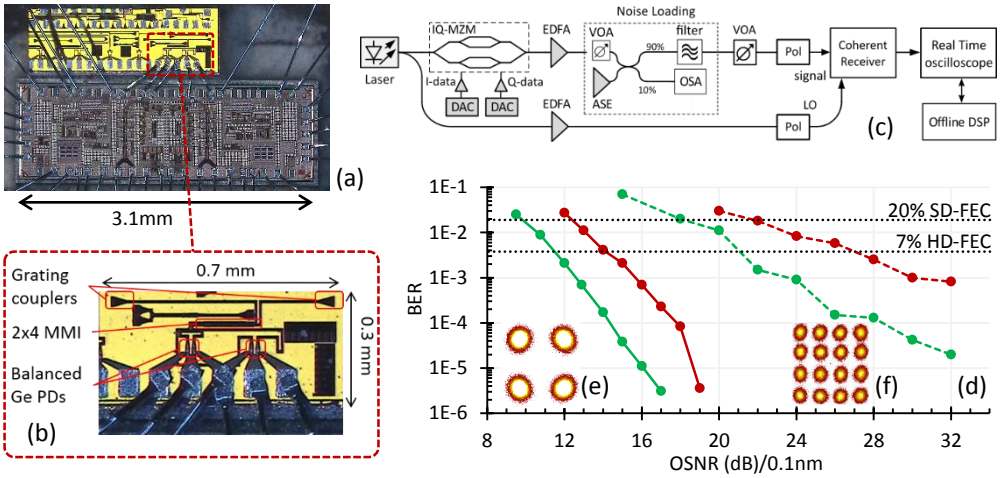

Fig. 1. (a) Micrograph of PIC + TIA-array chip; (b) PIC layout; (c) Test setup; (d) BER vs OSNR for 28 (green) and 40 GBaud (red); Example of a QPSK (e) and 16-QAM (f) constellation at 40 GBaud.

BER=3.8×10^{-3} at 7% overhead- requires an optical signal-to-noise ratio (OSNR) of ~14 dB for 40 GBaud QPSK, less than 3.5 dB from the theoretical minimum. At 28 GBaud 11.5 dB OSNR is needed for sub-FEC operation, corresponding to an even smaller penalty of <2.5 dB. For 28 Gbaud 16-QAM the HD-FEC threshold is passed at an OSNR of 21 dB. At 40 GBaud onset of an error-floor becomes noticeable, nonetheless stable operation well below HD-FEC is achieved. We even managed to successfully receive QPSK transmissions at 60 GBaud just below HD-FEC at a BER of 3.4×10^{-3}, but only for the highest OSNR that the setup could provide (i.e. ~33 dB). As the germanium photodiodes have a very high bandwidth and a slow roll-off [1], the TIAs probably form the bandwidth bottleneck of the ICR. The same PIC combined with a TIA-array with a bandwidth of ~35GHz would most likely suffice for a high-performance QPSK-ICR at 56 Gbaud.

In all experiments the receiver consumes 310 mW, an improvement of at least 40% compared to other reported Si-ICRs at 28 GBaud, while also realizing a PIC area reduction of a factor 4 [4]. A polarization division multiplexing version of this receiver could be realized by either using 2 dimensional grating couplers for fiber chip interfacing or by doing the polarization handling of chip, and combining two ICRs as presented in this paper on a single substrate.

Conclusion

We demonstrated the first silicon coherent receiver operating with high-performance at 40 GBaud QPSK and 16-QAM. Thanks to the ultra-compact design and the low power consumption of the co-designed TIAs, this receiver realizes an important building block for future compact pluggable transceivers modules (e.g. CFP4-ACO) at 300G and beyond.

References

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