H.264 on FPGA for cloud computing

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I. Introduction to cloud computing

Cloud computing is a technology that uses the internet and central remote servers to maintain data and server applications. It is a way to increase capacity or add capabilities on the fly without investing in new infrastructure, training new personnel or licensing new software.

Usually the cost of doing an operation in the cloud is lower due to several factors: device and location independence, multi-tenancy, scalability, utilization efficiency and maintenance. The H.264 encoder and decoder are suitable for a cloud implementation because of the large range of applications and multiple end-user platforms.

II. Introduction to H.264

Video compression is an essential technology for applications such as digital television, DVD-Video, mobile TV, videoconferencing and internet video streaming. H.264/AVC is one of the latest video coding standard which can save up to 45% of a stream's bit-rate compared with the previous standards. Some of the distinctive features are listed here : variable block-size motion compensation, motion vectors for each 8×8 can point to different references, six-tap filtering for half-pel luma sample predictions, quarter-pixel precision for motion compensation.[1] The H.264 decoder is about four times more complex than the MPEG-2 decoder and about two times more complex than the MPEG-4 Visual Simple Profile decoder[2]. In Figure 1 the main architectural blocks of a
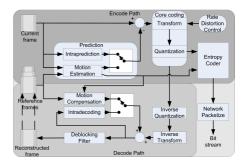

Figure 1. H.264 encoder and decoder top-level

standard Encoder and Decoder are shown.

III. Hardware-based H.264

A FPGA implementation of H.264 codec is suitable to serve many applications in parallel, because it can deliver fast operations, fast memory access and multiple streams. Also, FPGAs offer a lower power consumption and an increase in flexibility when compared to traditional approaches using digital signal processors and application-specific standard products.

In this article the principles of the challenging video coding standard H.264 are presented. H.264/AVC encoder and decoder building blocks are described and the advantages of implementing these blocks on an FPGA platform for applications in the cloud are shown.

References

[1] ITU-T Recommendation-International Standard of Joint Video Specification (ITU-T Rec. H.264/ ISO/ IEC14496-10 AVC), March 2003.
[2] R.G. Wang, "Motion compensation memory access optimization strategies for H.264/AVC decoder", IEEE ICASSP, vol. 5, pp.97-100, March 2005.

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