Room Temperature InGaAs/InP Distributed Feedback Laser Directly Grown on Silicon

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Abstract: We report an optically pumped room-temperature O-band DFB laser, based on the buffer-less epitaxial growth of high quality InGaAs/InP waveguides directly on silicon wafer.
OCIS codes: (140.5960); (160.6000); (230.0250)

1. Introduction

Since the early days of silicon photonics, the lack of on-chip laser sources has been a fundamental obstacle that inhibited its widespread adoption. Various solutions have been proposed, relying on engineered group IV materials and their alloys [1,2] or the integration of III-V materials through flip-chipping prefabricated laser diodes [3] or wafer bonding techniques [4, 5]. Although suitable for low-volume applications, the latter approaches do not fully benefit from the economies of scale offered by the well-established complementary metal-oxide semiconductor (CMOS) infrastructure, which is a main differentiator fueling the massive investments in silicon photonics.

Considerable efforts have been devoted to the direct epitaxial growth of III-V materials on silicon, mostly aiming at accommodating the large mismatch of lattice constant, thermal expansion and surface polarity [6]. Recently, a localized growth technique has been proposed that allows to grow almost defect-free InP and GaAs strips directly on silicon with very thin (~20 nm) buffer layer [7, 9]. By leveraging this technique, we have demonstrated an InP distributed feedback (DFB) laser array monolithically integrated on silicon [9]. In this paper, by growing InP/InGaAs heterostructures on an InP-on-Si virtual lattice matched structure, we demonstrate room temperature lasing in the near infrared.

2. Fabrication

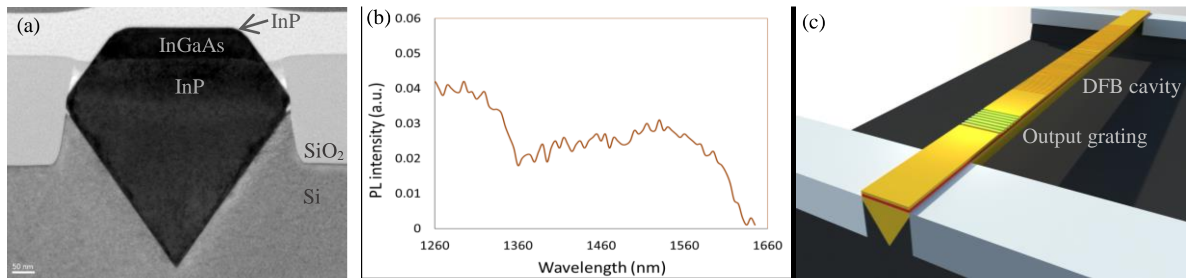

Figure 1 (a) Transmission electron microscope (TEM) image of the cross-section of an InP/InGaAs/InP waveguide grown directly on silicon. (b) Photoluminescence spectrum measured from an array of InGaAs/InP/Si waveguides. (c) A schematic plot of a fully processed InGaAs/InP DFB laser integrated on top of silicon.

The fabrication starts with a 300 mm (001) silicon wafer. Arrays of [110] aligned SiO_2 trenches were defined on top of the wafer by a standard shallow trench isolator (STI) patterning process, followed by a tetramethylammonium hydroxide (TMAH) solution based wet etch. The epitaxial growth of the InP waveguide was carried out in a 300 mm production metal organic vapor phase epitaxy (MOVPE) reactor. Details of the growth process can be found in ref. 9. After removing the overgrown InP by a chemical mechanical polishing (CMP) process, the wafer was loaded into the MOVPE reactor again to grow the InGaAs/InP heterostructures.

Fig. 1(a) presents a TEM image of the InP/InGaAs/InP heterostructures directly grown on the pre-patterned silicon substrate. Thanks to the well-optimized growth technique and the novel antiphase boundary (APD) elimination mechanism provided by the two <111> planes [9], no threading dislocations can be found outside of the very thin (~20 nm) defective layer at the InP/Si interface.. In addition, a sharp interface between the InGaAs and InP layers has been achieved. Fig. 1(c) gives a schematic plot of the full InGaAs/InP DFB laser structure. The detailed processing flow can be found in ref. 9. The DFB grating period is 362 nm with a 50% duty cycle. A λ/4 phase shift

is inserted in the middle of the cavity to ensure single mode laser operation. A second order grating was defined 40 µm away from the DFB cavity for vertical light extraction. To eliminate leakage loss to the substrate, we employed a soft dry etching process that undercuts the silicon substrate underneath the III-V waveguide. Very high yield is achieved, while the damage on the III-V material quality was found to be very limited.

3. Characterization

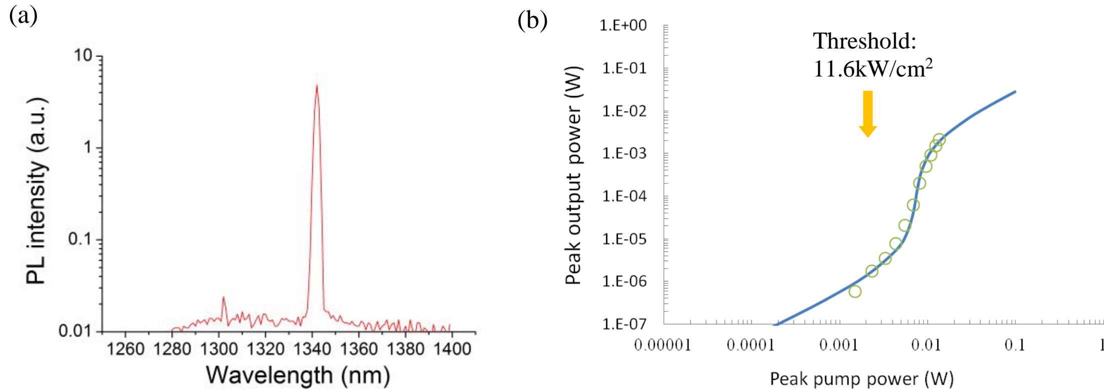

Figure 2 (a) Room-temperature laser emission spectrum measured above threshold. (b) Light in–light out (L–L) curve of the measured DFB laser. Open circles are measured data, and the solid line is the rate equation fit.

Fig. 1(b) presents the photoluminescence spectrum of the grown material under low intensity continuous wave pumping condition. While it is generally broad, the two major emission peaks located around 1300 nm and 1500 nm may be related to the non-uniform strain distribution in the layer stack, and splitting of the heavy hole and light hole valence bands. A micro-photoluminescence (µ-PL) set-up with a 7 ns pulsed laser (1064 nm) as the pump source was used for the further characterization [9]. A thermoelectric-cooled InGaAs detector was used to record the PL signal. Under low pumping intensity, the PL emission from a single IIIV waveguide is very low. By increasing the pump intensity, a sharp and intense peak shows up as shown in Fig. 2(a), and the side-mode-suppression-ratio (SMSR) can reach up to over 20 dB. The relatively wide full-width at half-maximum (FWHM) originates from the frequency chirp induced by carrier density variations under the pulsed pumping condition [9, 10]. Fig. 2(b) presents the measured LL curve of a laser working at 1355 nm on a double logarithmic scale. The obvious slope change as a function of pump intensity is a clear signature of lasing behavior. The peak pump intensity at lasing threshold is estimated to be 11.6 kW/cm^2, and the actual absorbed input power is 7 mW, which is a considerable improvement over the previously presented InP-on-Si laser [11]. This threshold reduction at least partly originates of the confinement of the photo-generated carriers in the InGaAs gain region.

It is worth to note that the recent demonstration of III–V based FinFET devices fully processed in a pilot CMOS line proves that it is indeed possible to avoid contamination from the III-V materials to other silicon devices processed in the foundry. Therefore, the proposed III-V laser on silicon can potentially be fully CMOS compatible.

4. Conclusion

In summary, we have presented an optically pumped near-infrared III-V laser that can be directly grown on (100) silicon, which may pave the path towards a fully integrated silicon photonic chip for large volume applications.

5. References

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