Balancing mechanisms for flying capacitor multilevel converters

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***Abstract*—To supply high-power medium-voltage AC machines, DC-AC converters working with a high bus voltage are required. By using multilevel converters, these high voltages can be supplied without the need for switches with a very high voltage rating. Moreover, the output voltage waveform can be improved considerably.**
The flying capacitor multilevel converter is a recently developed converter topology assuring a flexible control and modular design. However, the flying capacitor multilevel converter requires a balanced DC voltage distribution. This can be realized by using a special control leading to natural balancing or by measuring the voltages and selecting the appropriate switching state. The balancing is influenced by three factors, namely the harmonic content of the reference waveform, the switching frequency and the load impedance.
In addition to the voltage balancing of the flying capacitor multilevel converter, the output voltage must ensure the control of the load, e.g. a three phase AC machine.

***Index Terms*—Multilevel converter, flying capacitor, AC machines**

I. Introduction

Multilevel converters were developed as a result of a growing need for higher power converters. In order to achieve this higher power rating, the voltage and current capabilities of the devices used in the converter need to be increased. Current insulated gate bipolar transistor (IGBT) technology extends up to 6.5 kV 900 A per switching device. Converters that make use of a series connection of switches, allow for the use of switches with reduced voltage ratings. These lower voltage switches have lower conduction losses and can switch at a higher frequency. Higher switching frequencies and a smaller voltage step capability results in higher quality switching waveforms.
This paper focuses on the natural balancing property of the flying capacitor multilevel converter topology, also known as the capacitor clamped multilevel converter or the multicell converter topology.

II. Flying capacitor multilevel converter topology

In Fig. 1 a phase-leg of a flying capacitor multilevel converter is depicted, [1], [2]. In this circuit, independent capacitors clamp the device voltage to one capacitor voltage level. This converter topology has more flexibility than other multilevel converter topologies like the diode-clamped converter. Switches S_{1t}, S_{2t}, S_{3t} and S_{4t} are complementary with the corresponding switches S_{1b}, S_{2b}, S_{3b} and S_{4b}. The voltages of the capacitor banks are assumed to be at the nominal level at steady state. In Fig. 1, each capacitor symbol assigns for the same voltage value. So the first capacitor bank (C_1) has a voltage of $V_{dc}/4$, the second (2 times C_2) has a voltage of $V_{dc}/2$, the third (3 times C_3) has a voltage of $3V_{dc}/4$ and the fourth is the DC-bus and has a voltage V_{dc}. The voltage of the five-level phase-leg a output with respect to the neutral point n, V_{an}, can be synthesized by the following switch combinations. Here, the mentioned switches are on, the complementary are off.

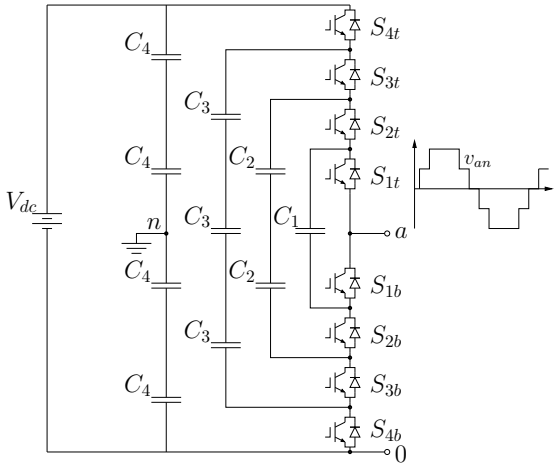

Fig. 1. Five-level flying capacitor multilevel converter circuit topology.

1) $V_{an} = V_{dc}/2$: turn on all upper switches, S_{1t}, S_{2t}, S_{3t} and S_{4t}.
2) $V_{an} = V_{dc}/4$: one of the upper switches is turned off and its complementary is turned on. When for example S_{2b} is turned on, $V_{an} = V_{dc}/4$ because of the following calculation: $V_{dc}/2$ (of upper C_4's) $-V_{dc}/2$ (of C_2's) $+V_{dc}/4$ (of C_1). This way a series connection of capacitors is made to create the desired output.
3) $V_{an} = 0$V: now two upper switches are turned off and their complementary switches are turned on. A similar calculation as above can be made.
4) $V_{an} = -V_{dc}/4$: in this case, there is only one of the upper switches on.
5) $V_{an} = -V_{dc}/2$: turn on all lower switches, S_{1b}, S_{2b},

S_{3b} and S_{4b}.

The voltage over the capacitors changes as current flows through the capacitors. By choosing an appropriate switch state for a desired output voltage according to the current direction, it is possible to control the voltage over the capacitors.

III. Control of capacitor voltages

The capacitor voltages can be controlled in two ways. Either the capacitor voltages and current direction are measured and an appropriate switch state is chosen to correct the capacitor voltage or a natural balancing scheme is used.

A. Measuring capacitor voltage and current and choosing switch state

This method requires measuring all the voltages of the capacitor busses and the direction of the phase current. When the sign of the error of the capacitor voltages and the direction of the current is known, an appropriate switch state for the desired output voltage can be assigned. This way the output voltage can be chosen at every instant, while always being sure the errors of the capacitor voltages are corrected.

Table 1 is a table with the switching states for a positive current, [3]. There is no choice when the desired output voltage V_{an} is $+/-V_{dc}/2$, so this is not in the table. For every possibility of deviation of the capacitor voltages ($+$ or $-$), a switch state can be determined. Here 1000 means S_{1t} is on and S_{2t}-S_{4t} are off. A similar table is available for a negative current.

unbalance			switch state (positive current)		
C1	C2	C3	$-V_{dc}/4$	0V	$+V_{dc}/4$
-	-	-	0001	0011	0111
-	-	+	0001, 1000	0011, 1001	1011
-	+	-	0001, 0100	0101, 1100	0111, 1101
-	+	+	0001, 1000	1001, 1100	1101
+	-	-	0010	0011, 0110	0111, 1110
+	-	+	0010, 1000	0011, 1010	1011, 1110
+	+	-	0100	0110, 1100	0111, 1110
+	+	+	1000	1100	1110

TABLE I
SWITCHING TABLE.

B. Natural balancing

Natural balancing of a flying capacitor multilevel converter is a technique which maintains the steady state stability of the capacitor voltages by using equal duty cycles for every pair of complementary switches. This can be done by using a special pulse width modulation (PWM) scheme. In this scheme, every pair of switches has a carrier signal which has a 90 degrees phase change, a so called phase shift carrier PWM (PSCPWM). When a reference signal, normally the desired output voltage, is compared with the carriers, the switch state of the corresponding switch pair is defined. When the reference signal is above the carrier, the upper switch is on and when below, the lower switch is on.

The control signals and output voltage of a PSCPWM for a five level converter are depicted in Fig. 2. The carrier signals with the reference signal are depicted in the upper part of the figure, with the thick carrier line the one of switch S_{1t}. Below this the switching signals of all the switches are depicted. The lower part gives the switched output voltage, which corresponds to the reference signal.

The static characteristics of the capacitor natural voltage balancing are well documented, but their dynamic response to DC bus variations vary significantly depending on parameters such as loading state, the modulation pulse ratio, filter design, etc, [4], [5], [6], [7].

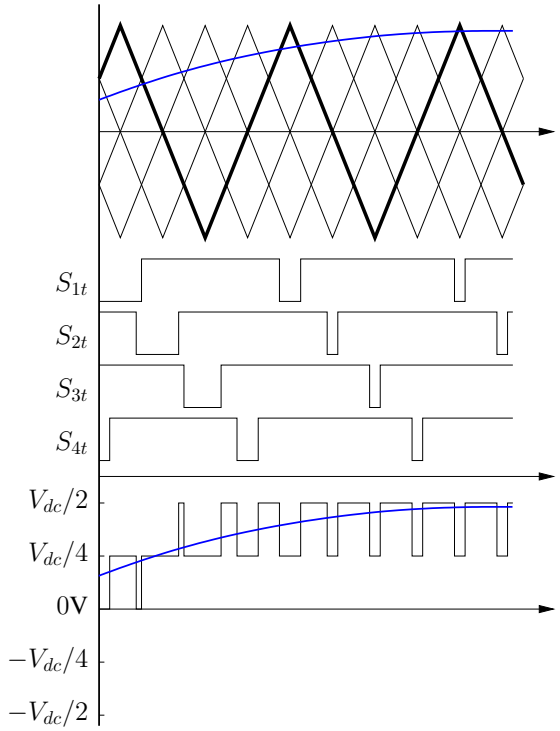

Fig. 2. Phase shift carrier PWM.

IV. Mathematical model

For simplicity, a 3-level flying capacitor multilevel converter will be used for this part, as depicted in Fig. 3. In the end the conclusions for the 3-level converters can be applied for higher level converters. The concept of a two-port switching circuit [8] will be applied. The basic two-port switching circuit is shown in Fig. 4. This switching circuit is controlled by a switching function $s(t)$ The arrow is pointed from port 1 to port 2. The relationship between the voltages $v_1(t)$ and $v_2(t)$ and the currents $i_1(t)$ and $i_2(t)$ are

$$v_2(t) = s(t)v_1(t), \tag{1}$$

$$i_1(t) = s(t)i_2(t). \tag{2}$$

The switching function $s(t)$ can assume any real value. In the case of a flying capacitor multilevel converter, $s(t)$ is the switching state of the switches connected to a capacitor and assumes the values -1 and 1.

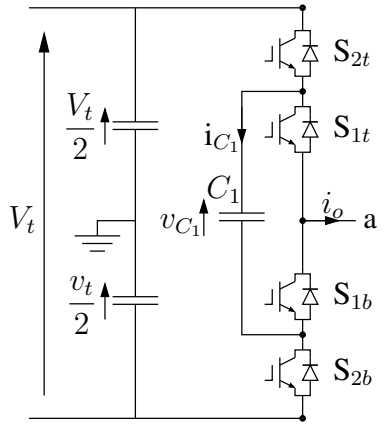

Fig. 3. 3-level flying capacitor converter.

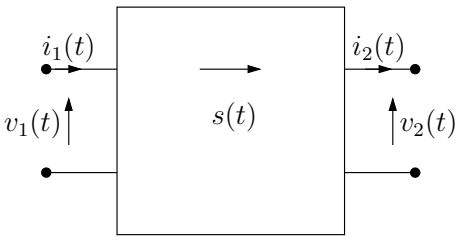

Fig. 4. Two-port switching circuit.

The relationship between the voltages and the currents of the two-port switching circuit can be obtained in the frequency domain as follows:

$$V_2(\omega) = S(\omega) * V_1(\omega) = \int_{-\infty}^{\infty} S(\xi)\, V_1(\omega - \xi)\, d\xi, \quad (3)$$

$$I_1(\omega) = S(\omega) * I_2(\omega) = \int_{-\infty}^{\infty} S(\xi)\, I_2(\omega - \xi)\, d\xi. \quad (4)$$

The $*$-symbol represents a convolution in the frequency domain.
This model of the two-port circuit can be used for a flying capacitor multilevel converter by defining the switching functions as follows:

$$s_i = \begin{cases} 1, & \text{if } S_{it} \text{ is closed,} \\ -1, & \text{if } S_{ib} \text{ is closed,} \end{cases} \quad \text{for } i = 1, 2. \quad (5)$$

V. Harmonic analysis

The phase shifted carrier PWM generates switching signals. These switching signals can be calculated, because the PSCPWM method makes use of comparing the reference value with a carrier signal for every pair of switches. Using Fourier methods developed by Bennet [9] and Black [10], it is possible to write Fourier series expansions for s_1 and s_2 using:

$$\begin{aligned} s_1 = \frac{1}{2}A_{00} &+ \sum_{n=1}^{\infty} \left[A_{0n}\cos(n\omega_r t) + B_{0n}\sin(n\omega_r t)\right] \\ &+ \sum_{m=1}^{\infty} \left[A_{m0}\cos(m\omega_s t) + B_{m0}\sin(m\omega_s t)\right] \\ &+ \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \left[A_{mn}\cos(m\omega_s t + n\omega_r t)\right. \\ &\left. + B_{mn}\sin(m\omega_s t + n\omega_r t)\right], \end{aligned} \quad (6)$$

$$\begin{aligned} s_2 = \frac{1}{2}A_{00} &+ \sum_{n=1}^{\infty} \left[A_{0n}\cos(n\omega_r t) + B_{0n}\sin(n\omega_r t)\right] \\ &+ \sum_{m=1}^{\infty} \left[A_{m0}\cos(m\omega_s t - 2m\pi)\right. \\ &\left. + B_{m0}\sin(m\omega_s t - 2m\pi)\right] \\ &+ \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \left[A_{mn}\cos(m\omega_s t + n\omega_r t - 2m\pi)\right. \\ &\left. + B_{mn}\sin(m\omega_s t + n\omega_r t - 2m\pi)\right]. \end{aligned} \quad (7)$$

In these equations for s_1 and s_2, the characteristics of the Fourier coefficients are important. For sinusoidal modulation with a modulation index of m_a, these Fourier coefficients are given by the following equations, [8]:

for $m \neq 0$:

$$A_{mn} + jB_{mn} = \frac{2}{jm\pi} J_n\left(\frac{m\pi m_a}{2}\right) e^{jn\pi}\left(1 - (-1)^n e^{jm\pi}\right) \quad (8)$$

for $m = 0$:

$$A_{mn} + jB_{mn} = \begin{cases} jm_a, & \text{if } n = 1 \\ 0, & \text{if } n \neq 1. \end{cases} \quad (9)$$

Here J_n denotes the Bessel function of the first kind [12], and m_a is the modulation index.
The Fourier coefficients can be summarized as follows:

- A_{00}: the dc-component of the reference signal.
- $A_{0n} + jB_{0n}$: Fourier series coefficients of the reference signal.
- $A_{m0} + jB_{m0}$: Fourier series coefficients at the switching frequency ω_s and integer multiples thereof.
- $A_{mn} + jB_{mn}$: Fourier series coefficients at harmonic side-bands around integer multiples of the switching frequency.

The harmonics of the switching functions occur in groups around integer multiples of the switching frequency. It is important to note that the values of the coefficients $A_{mn} + jB_{mn}$ are independent of the switching frequency. As the switching frequency is increased, the "distance" between the different groups of harmonics increases, but the amplitude and phase

remain unchanged.
In the general case, where the reference signal $f_r(t)$ is purely sinusoidal, it is difficult (if not impossible) to derive closed form solutions for $A_{mn}+jB_{mn}$. However, the following upper bound on the magitude of the harmonics can be determined, [13],

$$|A_{mn} + jB_{mn}| \leq \min\left(\frac{2}{m\pi}, \frac{1}{|n|\,\pi}\int_0^{\frac{2\pi}{\omega_r}}\left|\frac{df_r(t)}{dt}\right|dt\right). \tag{10}$$

This equation implies that the magnitudes of the harmonics decrease to zero as $|n| \rightarrow \infty$. By making use of this observation on the decay of the harmonics and the fact that the distance between the groups of harmonics increases as the switching frequency is increased, it is concluded that the overlap between the different groups can be made neglibible by choosing a high enough value of the switching frequency. In [6], it is shown that an overlap can result in cell capacitor voltage unbalance. Here, the theory has been explained for 3 level converters, but similar conclusions can be drawn for higher level converters.

VI. Practical verification of the natural balancing mechanism

The PSCPWM results in equal instantaneous duty cycles of the switching pairs. This results in an equal charge balance of the clamping capacitor, Fig. 5. Also the corresponding clamping capacitor current i_{C_1} and the load voltage of a half-bridge inverter v_{an} are depicted in Fig. 5. As can be seen in Fig. 5, the load current for a part of the time is delivered through the clamping capacitor. A part of the time the current flows in one direction and an other equal part of the time, the current flows in the other direction through the clamping capacitor. So in ideal conditions, the balancing is garanteed.

It is observed that as the clamping capacitor voltage v_{C_1} deviates from its nominal value $V_t/2$ ($v_{C_1} < V_t/2$ for the case shown), a switching frequency component Δv_{an} appears in the load voltage v_{an}. The voltage deviation results in a slight current variation which eliminates the voltage variation. We presume a positive output current i_o. For the case of a too low clamping capacitor voltage, as depicted in Fig. 5, the output voltage v_{an} is higher than usual while the clamping capacitor is discharged. When the clamping capacitor is charged, the voltage is to high because of the voltage deviation. This way the deviation of the clamping capacitor voltage will disappear with a certain time constant. This time constant increases with the capacitance of the clamping capacitor because then more current is needed for the same voltage change. The time constant also increases with the load impedance amplitude and the load impedance angle. The higher the load impedance amplitude, the less current flows, so the voltage balance takes more time. Also the angle of the impedance has an influence. With a pure reactive load, the clamped capacitor voltages would not balance. Also the modulation index has an influence. This is described theoretically in [5].
It is shown, [6], that the load impedance can be manipulated by adding a passive balance booster. This balance booster enhances the effect of the natural balancing mechanism. The balance booster has a low impedance for the switching frequency.

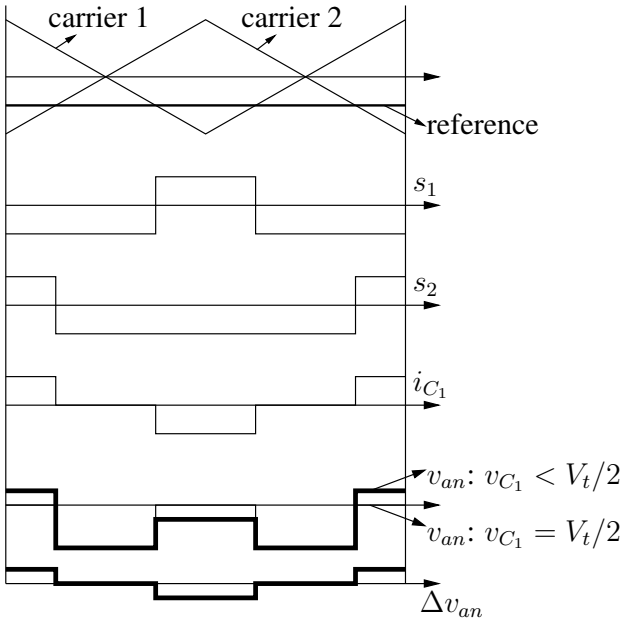

Fig. 5. Two-port switching circuit.

VII. Experimental verification the natural balancing mechanism

A test setup was built for the verification of the natural balancing mechanism. A 4-level flying capacitor converter was put together by connecting half bridge modules in series. All the half bridge modules stand on themselves by having their own gate voltage supplies and all the necessary measurements. This way, the converter has a totally modular design, where the number of levels can be easily changed.
The multilevel flying capacitor converter is controlled by a FPGA (Virtex-II Pro from Xilinx). The PSCPWM was implemented in the FPGA.
To be able to see the time constant of the balancing mechanism, a step in the voltage V_t was given. This gives a reaction in the clamped-capacitor voltages v_{C_i}. A voltage step of 100V is given in Fig. 6 and 7, each time with a different fixed duty cycle. A pure resistive load was used, the clamped capacitors are 2200μF. In Fig. 6, a high time constant is seen in comparison with Fig. 7. Fig. 6 has a higher current because of the higher duty ratio, but the clamped capacitors are only connected in series with the load for a relative short time. The other part of the time, the load is connected directly to the power supply. In the case of Fig. 7, the clamped capacitors are in series with the load all the time because with a duty cycle of 0.5, the output voltage switches between intermediate voltages all the time.

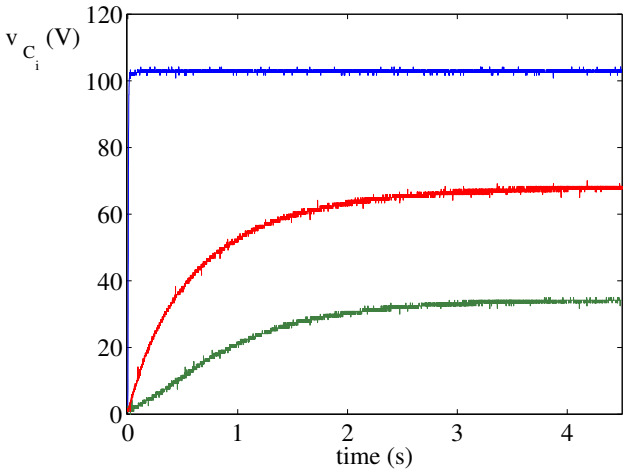

Fig. 6. Step in V_t, duty cycle of 0.88.

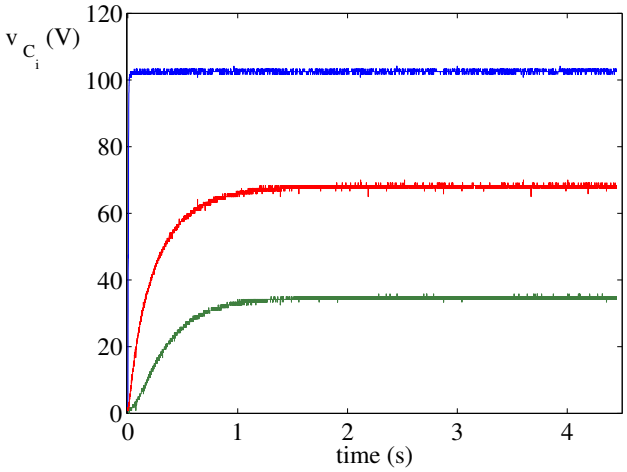

Fig. 7. Step in V_t, duty cycle of 0.5.

VIII. Conclusions

Multilevel converters and flying capacitor multilevel converters in particular were presented. The paper proposed two methods for controlling the clamped capacitor voltages. The first controls the capacitor voltages by measuring them en choosing an appropriate switch state. The second makes use of the natural balancing characteristic of the converter, so the capacitor voltages are balanced without measuring the clamped capacitor voltages. This inherent self-balancing mechanism would ensure safe operation under most operating conditions. A harmonic analysis of the flying capacitor multilevel converter was developed and it was concluded that a clamped capacitor voltage unbalance is possible when the switching frequency is not much higher than the highest frequency of the reference voltage. The load impedance is of high importance and can be manipulated to enhance the effect of the natural balancing mechanism.

The analysis carried out in this paper provides a basic understanding of the balancing mechanisms. In future research the dynamic properties of the natural balancing method will be further explored.

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