A 200 MHz 12-Bit Current-steering DAC in 0.35 μm CMOS

De Backer Els
Bauwelinck Johan
Qui Xing-Zhi
Vandewege Jan

Ghent university, INTEC/IMEC, Sint-Pietersnieuwstraat 41, B-9000 Gent

Abstract

In this paper a 12 b 200 MHz digital-to-analog (D/A) converter integrated in a digital 0.35 μm CMOS technology is presented.
The 12 b DAC is based on a current steering double segmented 6+2+4 architecture.
The DAC is designed to obtain good performances of INL and glitch energy.

1. Introduction

In applications like modern communication systems, high-speed and high-accuracy digital-to-analog converters are indispensable. DACs have a wide range of applications. Of several technology and architecture alternatives CMOS current-steering DAC architectures are suitable for applications with high clock frequency and high dynamic range at low cost.
The current steering DACs have static and dynamic performance limitations due to process variation, current mismatch and glitch energy. They are based on an array of matched current sources that are binary weighted or unit decoded.

This paper describes a high-speed current steering D/A converter with a resolution of 12 b.
In section II an overview of the architecture is presented. DAC linearity is discussed in section III. Some design considerations are described in section IV.

2. Basic Architecture

[1]
For a N-bit resolution DAC there are 2^N different combinations of the N bits, the DAC has 2^N different outputs from 0 to full-scale. The value of one least significant bit (LSB) corresponds to the difference between two adjacent output values. So we can see that 1LSB is given by $FSR/(2^N-1)$, with FSR the full scale range.
If the digital word of an N-bit resolution DAC is represented as (D_0, D_1, … , D_{N-1}), where D_0 is the least significant bit (LSB) and D_{N-1} is the most significant bit (MSB), then the output I_{OUT} of a current output DAC is given by

$$I_{OUT} = 2^0 D_0 I_{UNIT} + 2^1 D_1 I_{UNIT} + ... + 2^{N-1} D_{N-1} I_{UNIT} \qquad (1)$$

Where I_{UNIT} represents a unit current. In a current steering architecture, the DAC has a complementary output, I_{OUTN}, to the DAC full-scale current $I_{FS} = (2^N-1).I_{UNIT}$, and each bit of the digital input word determines if the current it controls is either steered to the output I_{OUT}, or to the complementary output I_{OUTN}.
A straightforward implementation of (1) is *the binary weighted architecture* (Fig. 1). Basically, it consists of N current sources each providing a current that is a successive power of 2 multiple of the current I_{UNIT}.

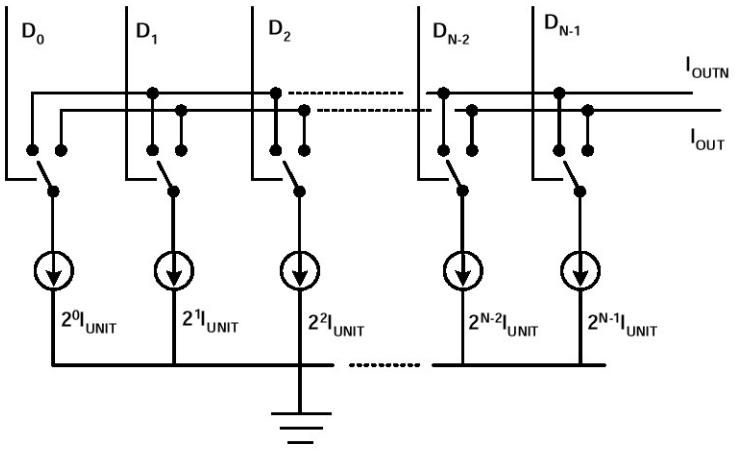

Fig. 1

Another architecture is the *unit element architecture or fully segmented architecture* (Fig. 2).
For a N-bit resolution DAC there are 2^N-1 identical current sources, each providing a current I_{UNIT}, connected to I_{OUT} or to the I_{OUTN} by 2^N-1 switches. To control the switches, the N-bit input word is thermometer decoded into 2^N digital signals that control the switches.

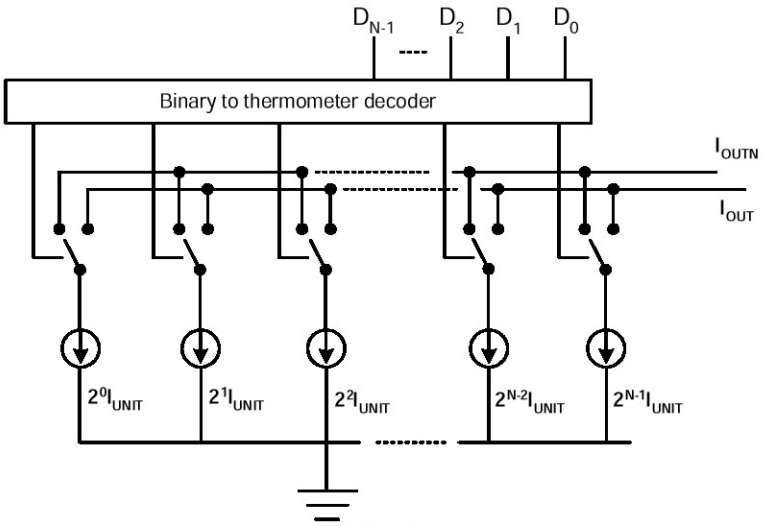

Fig. 2

The fundamental difference between the binary weighted and the unit element architecture is that in the first architecture the unit current sources are hard wired to define the weights, while in the second architecture the unit current sources are individually controlled.
The second architecture has a better linearity because the sources are better matched. However the settling time increases and the decoder becomes more complex, as the number of switches increases.

The two previous architectures are often combined in what is called the *segmented architecture.* The N_1 more significant bits control $2^{N_1} - 1$ equal current source segments of value $2^{N_2} I_{UNIT}$. The N_2 less significant bits control N_2 binary weighted current sources.

If the number of bits N_2 of the binary weighted part of the DAC is much smaller than the total number of bits, then the linearity and the glitch energy specifications are substantially reduced. However for every bit that is not implemented in a binary weighted architecture, the number of current source segments doubles, and so does the number of control lines needed to select these current sources. A direct consequence is often a reduction in the maximum operating speed. Equally important is the fact that the area used by the decoding logic complexity increases and consequently the process and electric systematic errors become more difficult to compensate. The key point to preserve a very high update rate is to keep an intrinsically simple and compact decoding logic. The best alternative consists of implementing a fast row-column decoding scheme.

The *segmented architecture,* which combines the binary weighted array with the unit decoded matrix, is desirable since it trades off glitch energy, DNL errors, decoding logic complexity, and overall chip area.

The architecture of the proposed 12 b DAC is a *6+2+4 segmented architecture*. The 12 b DAC consists of a 6 b unit element DAC, reproduced four times, a 2 b unit element DAC, and a 4 b binary weighted DAC.

The six most significant bits of the DAC select the 6 b unit element DAC. The 6 b unit element architecture consists of 256 unit array current sources, arranged in a 16x16 matrix. The matrix is logically seen as being composed of four 8x8 arrays, side-by-side (Fig. 3). The thermometer decoder is a two-stage decoder reproduced four times. There is a (3 to 7) b (Table 1) thermometer row decoder and a (3 to 7) b thermometer column decoder. A row-column decoder of six bits requires only AND and OR gates with at most three inputs.
The four 6 b DACs are mirrored in the layout with respect to the vertical and horizontal axis.

B3	b2	b1	d7	d6	d5	d4	d3	d2	D1
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Table 1

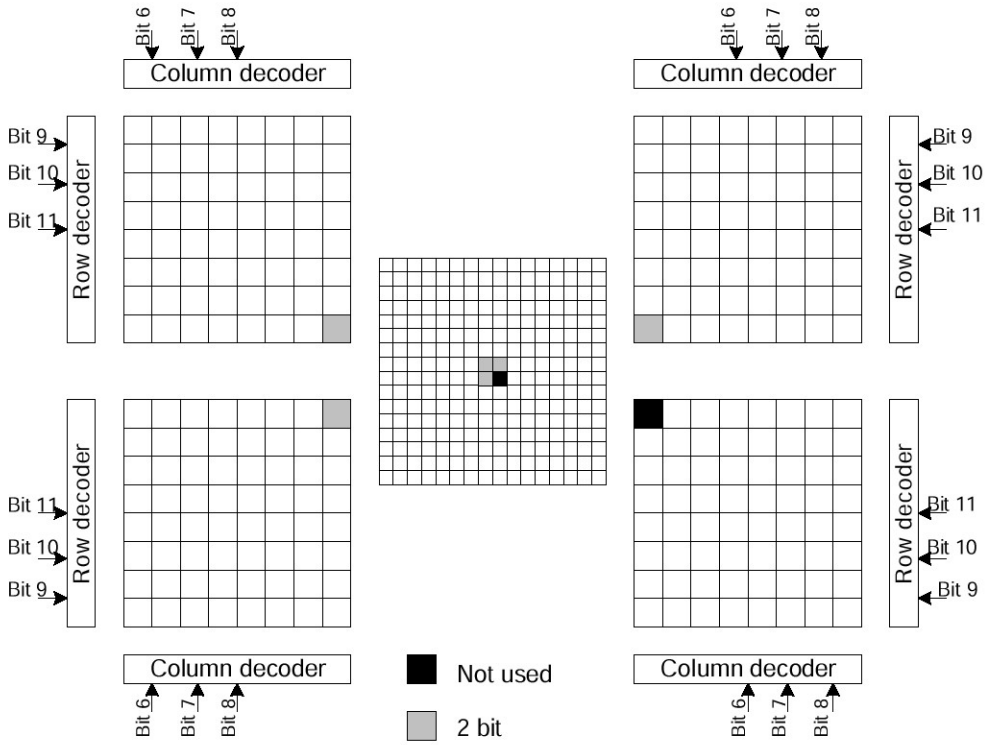

Fig. 3

The two intermediate bits of the DAC are also thermometer decoded ((2 to 3) b decoder). These bits select zero, one, two or three unit array current sources, which are placed in the center of the matrix.

The remaining four less significant bits select a simple PMOS 4 b current divider. These current sources will be placed in two columns next to the matrix.

The 4 b current divider generates the currents $I_0/2$, $I_0/4$, $I_0/8$, $I_0/16$, $I_0/16$. The first four currents are each switched by a two-way switch to I_{OUT} or I_{OUTN}. The last current is switched to I_{OUTN}.

3. DAC linearity

The static linearity of the DAC is given by its integral non-linearity specification. This is the worst-case deviation of the DAC input/output characteristic from the ideal straight-line characteristic (Fig. 4). [2]

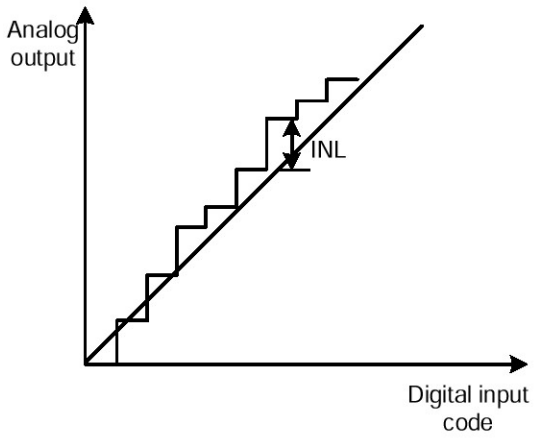

Fig. 4

In order to have an INL specification of ***1/2LSB*** a minimum requirement is that each and every current source of the DAC has a current error $\sigma(\Delta I_n)$ smaller than ***1/2LSB***

$$INL < \frac{1}{2} LSB \Rightarrow \frac{\sigma(\Delta I_n)}{I_n} < \frac{\frac{1}{2} LSB}{2^n LSB} \tag{2}$$

Noting that $1I_{UNIT}=1LSB$, a one sigma confidence value for the ***INL*** is given by

$$INL \cong \sqrt{2^{N-1}} \left(\frac{\sigma_1}{I_{UNIT}} \right) LSB = \frac{1}{2} LSB \tag{3}$$

For the design a 5σ confidence is used to obtain a very good yield and to have sufficient margin for secondary error contribution e.g. parasitic resistance of the interconnections.

$$INL \cong \sqrt{2^{N-1}} \left(\frac{5\sigma}{I_{UNIT}} \right) LSB = \frac{1}{2} LSB \tag{4}$$

For the design of the 12 b DAC a full-scale range (FSR) of 20 mA is implemented, so the least significant bit is 4.88 μA.
The relative standard deviation of I_{UNIT}, for a 5σ confidence, must be smaller than 0.22%.

To characterize the DAC dynamic linearity, the glitch energy, defined as the maximum time integral of the output transient for any two consecutive codes, is an important specification because the glitches, being for the most part code dependent, introduce distortion that reduces the DAC spurious free dynamic range. There are a number of factors affecting the glitch energy, namely charge injection and charge feedthrough at the switches, as well as timing mismatches.

Suppose there is only a timing mismatch ΔT_d between the control signals that turn ON and OFF a current source, when there are n unit current sources being switched, the glitch energy E_{glitch} is

$$E_{glitch} \cong n\Delta T_d I_{UNIT} \tag{5}$$

The worst case occurs at the MSB transition $(0\ 1\ \ldots\ 1 \rightarrow 1\ 0\ \ldots\ 0)$, when there are 2^{N-1} sources being switched.

$$E_{glitch}(MSB\ transition) \cong 2^{N-1}\Delta T_d I_{UNIT} \tag{6}$$

The worst case glitch energy must be smaller than the glitch energy corresponding to 1 LSB (E_{LSB}). The glitch is correlated with the output and introduces harmonic distortion, decreasing the spurious free dynamic range of the DAC.

$$E_{LSB} = 1LSB \cdot T_S \qquad T_s\text{: sampling period= 5 ns} \tag{7}$$

The least significant bit is 4.88 μA, so E_{LSB} is 24 fAs.

4. Design considerations

Ideally, there are no internal capacitances that need to be charged (or discharged) in a current steering architecture DAC (because currents are used instead of voltages), and this is why it is particularly suited for high-speed applications. Practical, the current source transistors are big because of the accuracy requirement, and so they have a large drain diffusion capacitance. This capacitance does not degrade the dynamic performance as long as it is not charged or discharged, that is, as long as the voltage at its terminal is kept constant. [3], [4]

4.1. Modelling formula for MOS matching

An important design consideration is the transistor matching. Random mismatch degrades INL. So it is important that the current sources are well matched. The mismatch on the drain current is defined by the mismatch for the threshold voltage and the mismatch for the transconductances.

For a given pair of transistors T_1 and T_2, V_{t1}, V_{t2}, β_1 and β_2 are the threshold voltages and the transconductances defined by

$$\beta = \mu_0 C_{ox} \frac{W}{L} \tag{8}$$

Mismatching for threshold voltage is

$$\sigma(\Delta V_t) = \frac{A_{V_t}}{\sqrt{WL}} \tag{9}$$

A_{Vt} is a constant, W and L unit are in μm

Mismatching for transconductance

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} + B_\beta \tag{10}$$

A_β and B_β are constants, W and L are in μm

Mismatch on drain current

$$\left(\frac{\sigma(I_d)}{I_d}\right)^2 = \frac{4\sigma^2(\Delta V_t)}{(V_{gs} - V_t)^2} + \sigma^2\left(\frac{\Delta\beta}{\beta}\right) \tag{11}$$

Considering (11) we can prove that, to reduce the random mismatch of the PMOS current source, we have to choose a rather big W and L.

Systematic, process-related error sources are as important as random error sources for precision analog design. While the random errors are made smaller by increasing the device dimensions, the opposite happens with the systematic errors.

Typical sources of systematic process-related MOS transistor mismatch are variations in the gate dimensions (edge-effects), wafer gradients in the gate-oxide thickness and in the channel doping, photolithographic and etching effects (micro-loading), and source-drain asymmetry. In the absence of a quantitative knowledge about the importance of each of these terms, the circuit designer enforces a set of device layout rules [5]:

- Devices should have the same shape and size, and not simply the same aspect ratio
- Matching devices should be at minimum distance
- Devices should have the same current orientation
- Common-centroid geometry should be used
- Devices should have the same surroundings

However for transistors with large W/L ratios a simple rectangular geometry becomes impractical, because the aspect ratio strongly deviates from one, and introduces transistor placement constraints as well as degradation in the transistor characteristics. When transistors with large W/L ratios are used, the layout style may have an influence on the matching performance. The avoid systematic variations in the transistor drain current, due to electrical, thermal or process gradients, point symmetric structures are recommended. To keep the transistor aspect ratio close to one, finger-style structures are the preferred layout style [6].

4.2. Architecture

In Fig. 5 you can see a basic current source and switching transistors. As discussed in previous section the current source transistor has to be rather big for better matching and for better linearity. The currents are each switched by a two-way switch to I_{OUT} or I_{OUTN}.

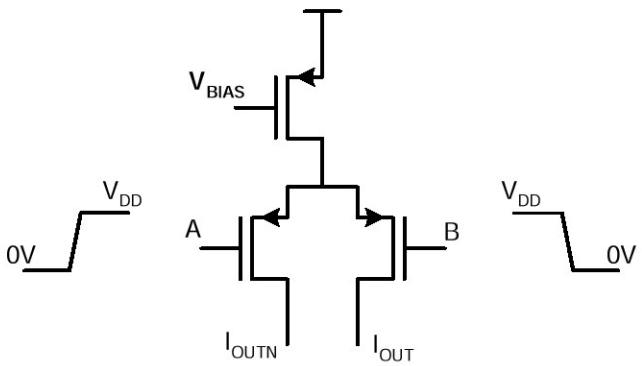

Fig. 5

The cross-point voltage of the control signals can be seen in Fig. 6 (dotted line). To reduce the glitch energy a driver circuit is necessary.

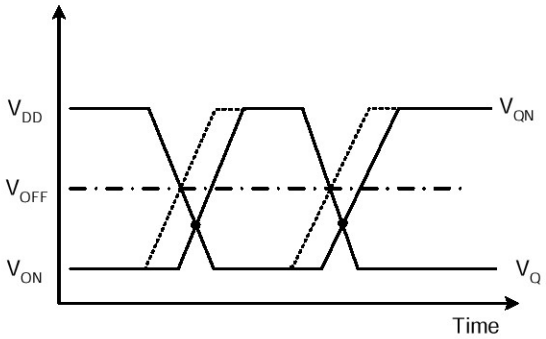

Fig. 6

This *driver* (Fig. 7) reduces the cross-point voltage of the control signals (Fig. 6 full line). By doing so the voltage swing at the drain of the current source is reduced during switching. This swing must be limited because the current source has a considerable capacitance since they are relatively big to achieve a good matching. This capacitance does not degrade the dynamic performance as long as it is not charged or discharged, that is, as long as the voltage at its terminal is kept constant.

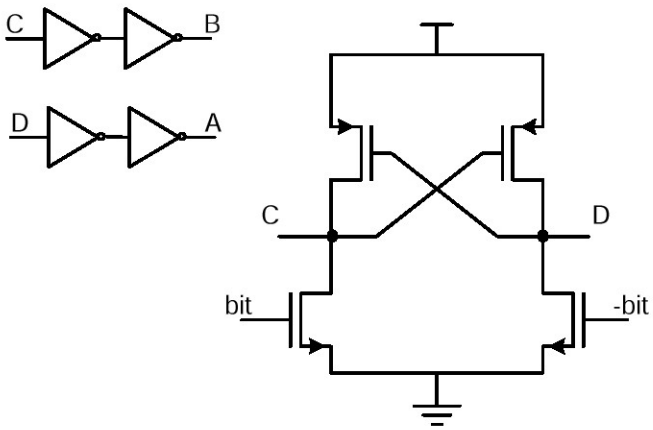

Fig. 7

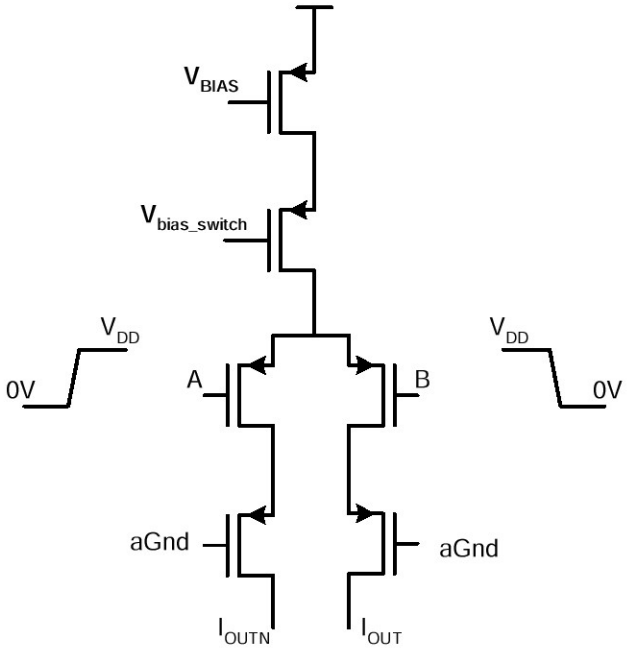

Fig. 8

Another cause of glitches is charge feedthrough. To reduce the glitch the switch circuit (Fig. 5) is modified [7]. An extra cascode transistor is added (Fig. 8) to provide the necessary high output impedance and the charge feedthrough is partially compensated by inserting dummy transistors.

Fig. 9 shows a simulation result for the INL caused by systematic errors (e.g. due to finite output impedance). This simulation is done in a typical case. The INL is smaller then 0.15 LSB.
By doing corner simulations the worst case INL caused by systematic errors has been determined and is 0.29 LSB. The DAC has been simulated for temperature variation from –40 ^{o}C to 125 ^{o}C.
The supply voltage is 3.3 V. The simulations had been done for a variation from 2.95 V until 3.65 V.
Fig. 10 shows a transient response in a typical case. The analog output is shown for an increasing digital input. The digital input increases from 1 to 19. The transition from 7 to 8 (at 40 ns) causes a glitch of 8 fAs.

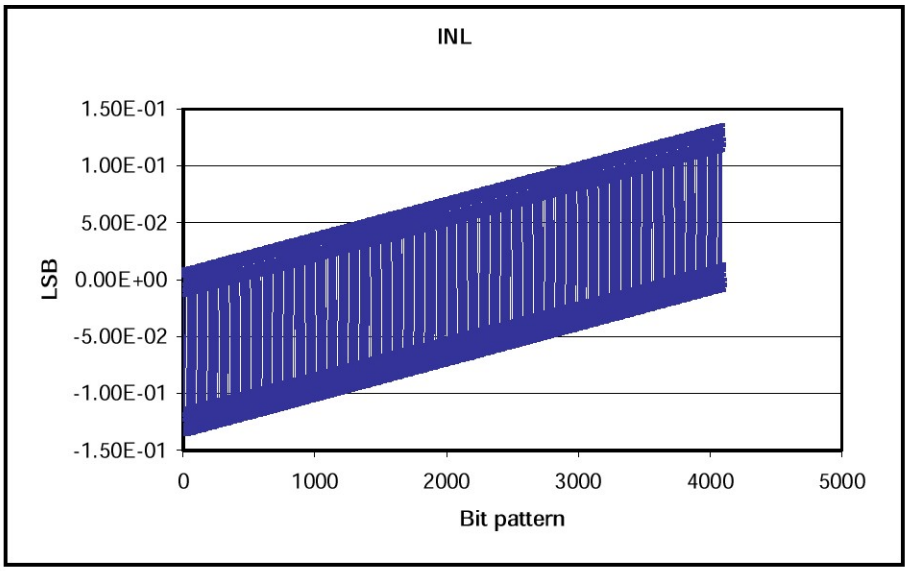
INL
1.50E-01
1.00E-01
5.00E-02
0.00E+00
-5.00E-02
-1.00E-01
-1.50E-01
LSB
0
1000
2000
3000
4000
5000
Bit pattern

Fig. 9

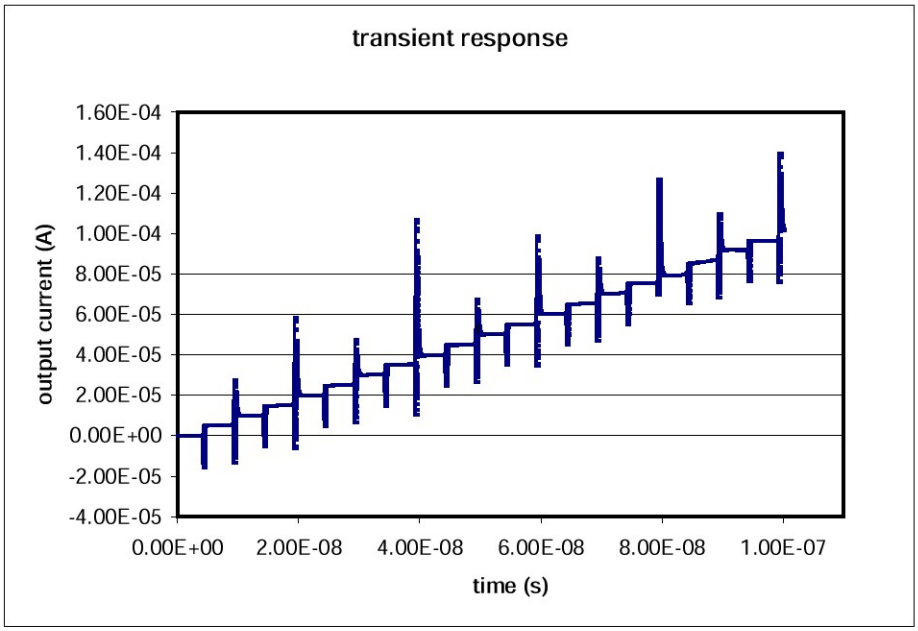
transient response
1.60E-04
1.40E-04
1.20E-04
1.00E-04
8.00E-05
6.00E-05
4.00E-05
2.00E-05
0.00E+00
-2.00E-05
-4.00E-05
output current (A)
0.00E+00
2.00E-08
4.00E-08
6.00E-08
8.00E-08
1.00E-07
time (s)

Fig. 10

5. Conclusion

A 200 MHz 12 b current-steering DAC has been proposed. Different design considerations to improve the DAC linearity have been discussed.
The simulated worst case INL caused by systematic errors is smaller than 0.29 LSB.

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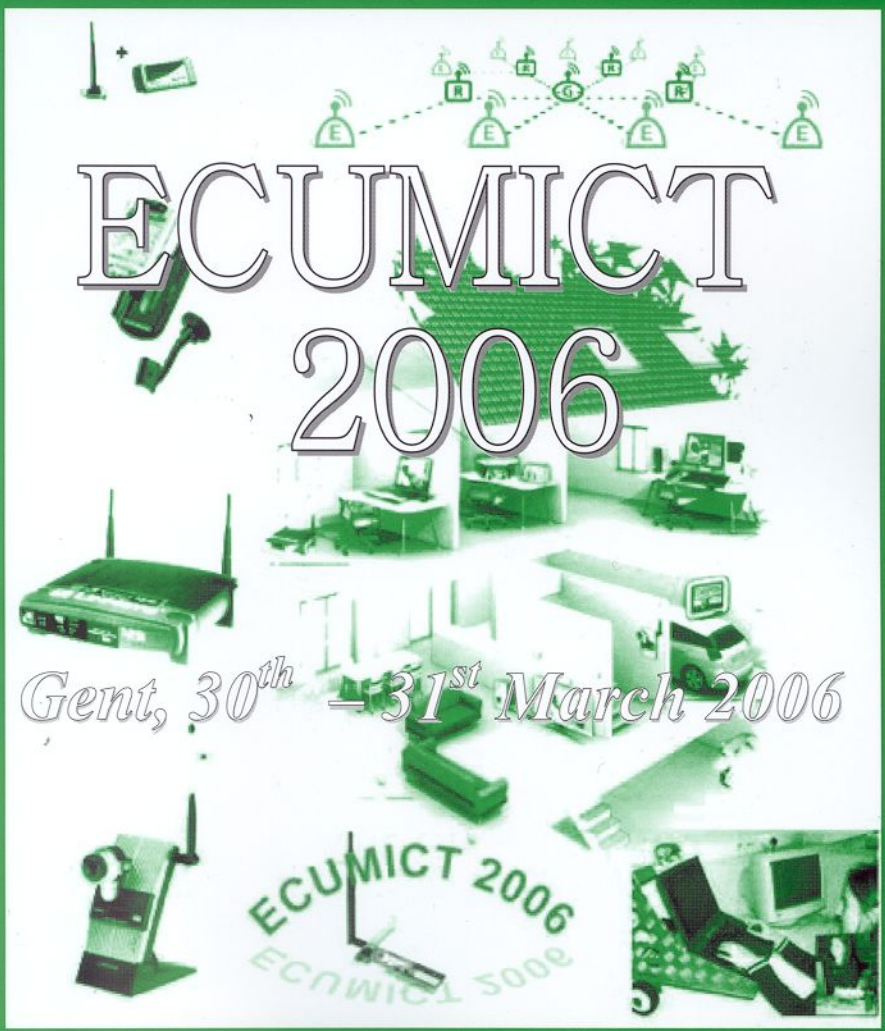

Luc De Backer (editor)

KaHo St Lieven, Department of Industrial Engineering / Electronics

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