IST-LASAGNE: Demonstration of all-optical label-swapping functionalities employing optical logic gates and optical flip-flops

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Abstract

The IST-LASAGNE project aims at designing and implementing the first, modular, scalable and truly all-optical photonic router capable of operating at 40 Gb/s. The main results achieved in the project are presented in this paper, with emphasis on the implementation of network node functionalities employing optical logic gates and optical flip-flops, as well as an economical study on the proposed all-optical node architecture. Experimental results on clock recovery, packet-rate clock recovery and 2-bit label reading are provided employing optical gates based on active Mach-Zehnder interferometers as the basic building block. The obtained results are very promising towards the goal of building an all-optical photonic router for label-swapping networks.

I. INTRODUCTION

The huge growth of Internet traffic during the last years is forcing next generation Internet Protocol (IP) networks to increase their capacity, performance and packet forwarding rates. Future IP-based all-optical networks will require technologies to enable packet routing at Terabit/s bit-rates supporting new streamlined IP routing protocols such as Multi-protocol Label Swapping (MPLS) [1]. Optical network node implementations reported so far perform label packet processing in the electrical domain using alternative modulation formats or subcarrier multiplexing at lower bit-rates (i.e. IST-STOLAS [2] or IST-LABELS [3] projects) through hybrid optoelectronic node architectures. However, in order to achieve high data-rate operation [4], packet-format transparency [5] and high transmission efficiency, all network node functionalities, such as switching, routing and forwarding must be carried out directly in the physical layer. Likewise, the node optical layer needs to implement the required "intelligence" to look up the routing table and forward the packets.

All-optical label swapping (AOLS) has been proposed as a viable approach towards resolving the mismatch between fibre transmission capacity and router packet forwarding capacity [6]. In such an AOLS scenario, all packet-by-packet routing and forwarding functions of MPLS are implemented directly in the optical domain. By using

optical labels the IP packets are directed through the core optical network without requiring O/E/O conversions whenever a routing decision is necessary. The main advantage of this approach is the ability to route packets/bursts independently of bit-rate, packet format and packet length increasing network flexibility and granularity, attributes highly desirable in broadband networks characterized by bandwidth-on-demand applications. In addition, compared to previous node implementations [2,3,7], the all-optical network node must be capable of operating with in-band serial-bit label signalling at the line-rate, attaining high bandwidth utilization and simplified transmitter implementation. The ability to process labels at the line-rate through all-optical techniques eliminates the necessity for O/E/O conversions and allows for high information capacity to be encapsulated in the labels compared to lower-bit rate approaches [6]. Further, the labels are generated with the same light sources and intensity modulators as the payload [8], a major requirement for implementation of next generation truly all-optical networks.

LASAGNE objectives include studying, proposing and validating the use of all-optical logic gates based on commercially available technologies to implement network functionalities at the metro/core network nodes in AOLS networks. In this paper, the main results achieved in the LASAGNE project are presented, with emphasis on the experimental results of all-optical label swapping functionalities employing optical logic gates and optical flip-flops. Experimental results on clock recovery, packet-rate clock recovery and 2-bit label reading are provided employing optical gates as the basic building block. These optical gates are based on ultrafast nonlinear interferometers (UNIs) or active Mach-Zehnder interferometers (SOA-MZIs). Furthermore, a first study on the economical viability of the proposed all-optical node is reported, where the cost of all-optical nodes is compared with the cost of nodes employing electronic header processing.

II. EXPERIMENTAL RESULTS

In this section, the main results of all-optical label swapping functionalities employing optical logic gates and optical flip-flops are described.

40 Gb/s Packet Clock Recovery and Packet-Rate Synchronization

Two synchronization sub-systems were designed, theoretically modelled and experimentally demonstrated within the first year of the project. A clock recovery circuit operating at the line rate was designed, simulated and implemented for 40 Gb/s operation. The optical circuit operates on a per-packet basis, where packet clock signals are self-extracted from each incoming data packet. In addition, a packet-rate synchronization circuit capable of generating a single optical pulse per incoming packet was experimentally demonstrated at 10 Gb/s. These packet synchronized pulses are used to drive subsequent optical gates and sub-systems of LASAGNE node. Both synchronization schemes proposed in LASAGNE node do not require local signal generation or synchronization of incoming packets with local optical oscillators. In contrast, the AOLS node was designed to be self-synchronized through "self-extracted" signals that are used to power or control subsequent optical gates and successfully perform the necessary optical signal processing within the node.

Fig. 1 shows the experimental setup used to validate the proof-of-principle of the 40 Gb/s packet clock recovery and consists of the 40 Gb/s packet generator and the clock recovery circuit comprising a low-Q Fabry-Perot filter (FPF) and an optical gate implemented as an UNI [9]. Fig. 2 (a) shows a sequence of three 40-bit long packets

separated by 750 ps at 40 Gb/s. The role of the FPF is to partially fill the zeros within the packet and generate deeply amplitude modulated, but clock resembling packets at its output. When this signal is fed as control into the saturated UNI gate, clock packets with very short rise and fall times are generated and depicted in Fig. 2 (b). Fig. 2 (c) and (d) provide a more detailed view of a single packet and its transformation to an amplitude equalized packet clock signal at the output of the gate. Fig. 2 (d) shows that the clock is captured from the first bit and exhibits a fall time of 16 bits, whereas the amplitude modulation (highest to lowest pulse ratio) within the 40 clock pulses is below 1 dB. The sharp rise time is a result of the heavy saturation of the SOA and determines the lock acquisition time of the circuit, whereas the fall time is due to the lifetime of the filter and determines the minimum intra-packet guard-bands. The circuit was operated with 1 mW of optical power for the CW signal and 80 fJ/pulse for the data signal. The timing jitter performance of the circuit was measured using the precision time base option of an Agilent/HP 86100A Infinium digital sampling oscilloscope. Fig. 2 (e) shows the eye diagram obtained for the input signal at 40 Gb/s with rms timing jitter of 450 fs. The reshaping properties of the power-limiting gate are shown in Fig. 2 (f) through the eye diagram of the recovered clock at 40 GHz with measured timing jitter of 580 fs. The slight increase in rms jitter was due to the difficulty of precisely aligning the bulk FPF used, resulting in small line-rate detuning. This effect can be eliminated by using fibre-based FPFs.
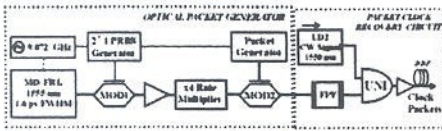

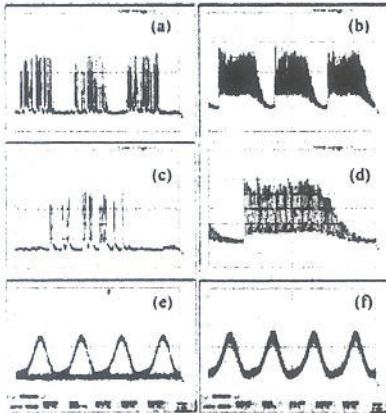Fig. 1: Experimental Setup of 40 Gb/s Packet Clock recovery.

Fig. 2: Experimental results: (a), (b), (c) 40 Gb/s incoming data packets and (b), (d), (f) recovered optical clock.
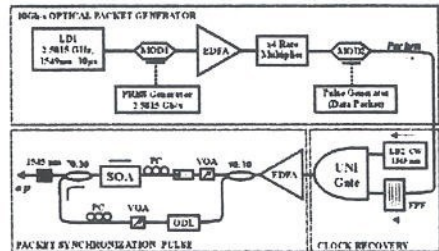

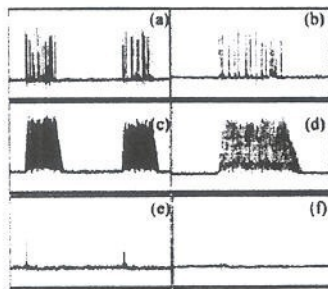Fig. 3: Experimental Setup of 10 Gb/s Packet-Rate Synchronization.

Fig. 4: Experimental results: (a), (b) 10 Gb/s incoming data packets, (c), (d) recovered clock packet, (c), (d) extracted packet pulse.

The experimental setup used to demonstrate the operation of the packet-rate clock recovery at 10 Gb/s is depicted in Fig. 3 and consists of the 10 Gb/s data packet generator, the packet clock recovery circuit and an additional SOA device. In

accordance with the previous section, a clock packet is self-extracted from each corresponding data packet entering the clock recovery circuit. After amplification through an EDFA, the extracted clock packets were split and inserted into a 1.5 mm SOA in a counter-propagating fashion, synchronized with one bit offset. The operation of the circuit relies on cross-gain modulation and the specific temporal synchronization of the involved signals within the amplifier. Due to the single-bit delay induced, only the first clock pulse experiences amplification, whereas subsequent probe pulses are suppressed through the interaction with the counter-propagating strong pump signal incident on the SOA. Fine synchronization of the signals was achieved using optical delay line (ODL1) and both signal polarization states needed adjustments due to the polarization-dependence of the SOA used. Fig. 4 shows typical oscilloscope traces verifying the circuit principle of operation. More specific, Fig. 4 (a) shows the 4 ns optical packets separated by 8.4 ns and Fig. 4 (b) shows a single packet in more detail. Figure 4 (c) and (d) show the recovered clock packets exhibiting 2 bits rise time and 8 bits fall time. This signal is then split and inserted into the SOA responsible for the single pulse extraction. The recovered clock packet acting as the probe signal is within the small-signal-gain region of the amplifier and the first preamble pulse enters the SOA that is fully unsaturated. After experiencing full amplification, it exits the SOA. The remaining clock pulses are suppressed through gain saturation induced by the counter-propagating strong recovered clock signal, acting as the pump. As a result, a single pulse is allowed to exit the SOA and this is shown in the oscilloscope traces of Fig. 9 (e) and (f). The switching power/energies used in the UNI gate were 0.8 mW for the CW power and 110 fJ for the control input. The single pulse extraction required 300 fJ and 15 fJ for the pump and probe signals respectively in order to invoke XGM within the amplifier. Since the circuit relies on saturation effects within an SOA, the operational speed of the circuit is dictated only by the packet clock recovery circuit making the scheme upgradeable to 40 Gb/s. The proposed circuit will be experimentally verified using 40 Gb/s data packets combined with an SOA-MZI packet clock recovery during the second phase of the project.

Address recognition employing cascaded logic XOR gates

The proposed architecture for the all-optical packet header processor or optical correlator is shown in Fig. 5. Its principle of operation as well as some simulation results were already published in [10]. It is mainly based on a cascade of photonic-integrated SOA-MZIs. Each one of these SOA-MZIs (provided by CIP) is configured to perform the logic XOR function as in [11], but using a counter-propagating optical pulse instead of a CW as the control signal. 10 GHz repetition-rate optical pulses with a FWHM of about 2 ps are generated at 1553 nm using a fibre-based pulsed laser, whereupon a MZM encodes the 10 Gb/s data signals from a bit pattern generator. Different bit patterns (data A and data B) are obtained by using a 50:50 optical coupler and optical delay lines (ODLs) at the output of the label data generation module. The pulsed control signal is obtained by modulating a CW optical laser with 1 GHz repetition-rate pulses of 25 ps FWHM.

Both RZ-modulated input data streams (data A and data B) at 10 Gb/s with a FWHM of 9.6 ps (measured with a 65 GHz optical sampling scope) are coupled into the upper and lower branches of the first SOA-MZI with 2.5 mW peak powers, whereas the pulsed control signal at 1550.8 nm and with about 1 mW peak power is coupled into the common SOA-MZI port using a counter-propagation configuration. The output signal from the common port of the first SOA-MZI is the result of the logic XOR operation of the first bits of both data streams. This output signal, after proper optical attenuation

and delay, is also launched into the second SOA-MZI in a counter propagation configuration but synchronised with the second bit of both data patterns. This optical pulse acts as an enabling signal for the second logic XOR gate as in [12]. By cascading the different SOA-MZI structures, the following logic function is obtained [10]:

$$S = \begin{cases} 0, & \text{if } A \neq \overline{B}. \\ 1, & \text{if } A = \overline{B}. \end{cases} \tag{1}$$

where A and B are the input data signals to the optical header processor and S is the output from the second stage. Therefore, the device can be employed as an all-optical correlator for bit-pattern matching applications by introducing the one's complement of one of both data signals or addresses to be compared.

Synchronisation between the data and the control pulses is a must to obtain the proper operation of the cascaded XOR gates and this is achieved by means of adjustable ODLs in the experiments. Both arms of the SOA-MZIs were biased with 300 mA DC currents. Due to the counter-propagation operation, an isolator must also be used between both SOA-MZI stages to avoid saturating the first stage with the second stage signals. Two tuneable filters with a −3 dB bandwidth of 1 nm were also used to minimise the effects of cascading the ASE noise from the SOAs.
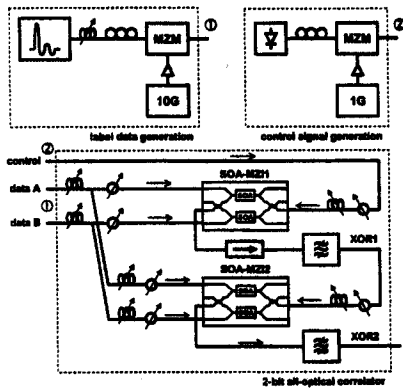

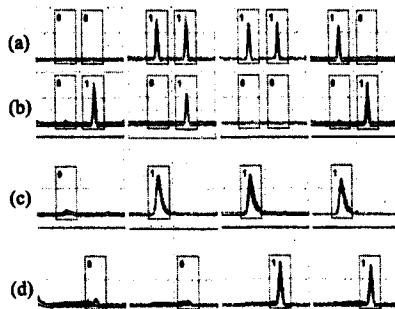Fig. 5: Experimental set-up for the 2-bit XOR correlator.

Fig. 6: Experimental results: (a) data A, (b) data B, (c) XOR1, and (d) XOR2.

Different data pattern combinations were used to evaluate the proposed architecture. The experimental results for the all-optical correlator are shown in Fig. 6 for 4 different bit patterns: 1) A=[0 0], B=[0 1], 2) A=[1 1], B=[0 1], 3) A=[1 1], B=[0 0], and 4) A=[1 0], B=[0 1]. As it can be seen in Fig. 6, the output from the first SOA-MZI (XOR1) is the logic XOR of the first data bits, Fig. 6 (c), whereas the output from the second SOA-MZI (XOR2) is the logic function given by (1), Fig. 6 (d). An extinction ratio of 13 dB and peak power values higher than 5 mW were found for the output, which are very appropriated to control, for example, an optical flip-flop within a photonic network node. A FWHM of 12.8 ps was obtained for the output pulses from the correlator.

Optical flip-flops

The all-optical flip-flop memory that we propose is based on two coupled lasers with separate laser cavities, where light from one laser suppresses lasing in the other one

[13]. A critical issue is the amount of coupling between the two lasers. The minimum amount coupling between the lasers that is required to obtain bi-stable operation depends on the implementation, but the coupling should be strong (typically 40% or larger) [13]. Fig. 7 shows the experimental set-up for an experiment to demonstrate the operation of the optical flip-flop memory. The two SOAs act as the lasers gain media. In this particular set-up a ring-laser configuration is used. We have used Fabry-Perot filters with a bandwidth of 0.18 nm as wavelength selective elements. The SOA 1 was pumped with 168 mA of current whereas the SOA 2 was pumped with 190 mA. The pulses that were used to set and reset the flip-flop had a power of 2 mW. The switching characteristics of the optical flip-flop are presented in Fig. 8. It can be observed from Fig. 8 that, if sufficient external pulse is coupled into the flip-flop, the system changes states. It should be noted that it is also possible to realize optical flip-flops by coupling other optical nonlinear elements than lasers. Examples are given in [14-17] in which flip-flop operation is demonstrated by using coupled nonlinear Mach-Zehnder interferometers and coupled nonlinear polarization switches.
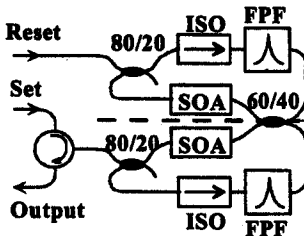
Fig. 7: Ring laser implementation of the optical flip-flop memory. SOA: semiconductor optical amplifier, ISO: isolator, FPF: Fabry-Perot filter.
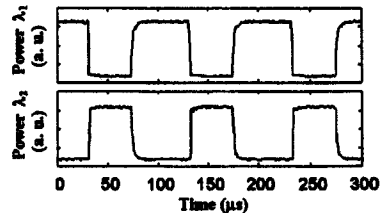
Fig. 8: Oscilloscope traces showing power of laser 1 and laser 2. Regular toggling between the states can be clearly observed.

Photonic integration of optical flip-flops is essential for applications in optical networks. Integrated optical flip-flop memories should have fast (optical) set and reset times, operate at low power, have a high contrast ratio and should have sufficiently small dimensions. An integrated optical flip-flop memory based on laser operation is presented in [17], but the power consumption, the size, and the switching speed of these devices remain an issue, which makes it difficult to couple them in large quantities as required in optical RAM. A more promising all-optical flip-flop concept based on two coupled micro-lasers is presented in [18]. This flip-flop concept has the potential to have the dimensions in the order of the wavelength of light, a switching speed of a picosecond and a switching energy below a femtojoule. If one succeeds to interconnect these flip-flops, densely integrated digital optical logic operating at high speed and low power can be realized.

III. TECHNO-ECONOMICAL STUDY

In this section, the building cost of the LASAGNE node is compared with the cost for other packet-switching nodes (e.g. WASPNET node with electronic header processing, Elect. Header node, [19]). Since all architectures intend to switch at a packet-by-packet level, but each of them is using a different technology, the cost comparison will be dependent on most characteristic parameters for each technology. We will make a distinction between the optical cost and the what-we-call electronic cost. Since a

detailed explanation of the cost functions would lead us far beyond the scope of this paper we will organize this section as follows. First we introduce the parameters to accomplish the cost functions in Table I, and then we give an overview of the building of the cost functions. We close this section with a cost comparison and conclusions.

Table I: The parameters used to describe the cost functions.

Name	Description
F	The number of fibres
W	The number of wavelengths in one fibre
P	The ratio between the optical cost for an FCC and the electronic cost for an OEO, thus P=Cost$_{OEO @ 155 Mbps}$/Cost$_{FCC}$
B	The number of bits in a label
BR	Header bit rate

To compare the optical cost of different node architectures we have defined the number of Fibre-to-Chip Couplings (FCCs) for each of the optical components in the node architectures. This choice is based on the assumption that packaging and, more specifically, the number of interconnections to the outer world dominate the cost of optical components. A sum over all the components in the architecture gives the total number of FCCs for the specified architecture.

To address the electronic cost of a node we have counted the number of OEO conversions. We assume that the reference cost of 1 can be set to the cost of one OEO conversion at a bit rate of 155 Mb/s. For higher bit rates the cost is defined according to the following relation: Bit Rate x 4 → Cost x 2.5. Additionally, we define the Total cost as follows: Total Cost = Optical Cost + P x Electronic Cost.

Costs Comparison

The share taken by the optical cost in the total cost depends heavily on the node architecture. It changes from 100% in the all-optical approaches to 0% in electronic routers. For the Elect. Header node the percentage of the optical cost is influenced by the parameter P. As already mentioned P=Cost$_{OEO@155 Mbps}$/Cost$_{FCC}$ and thus reflects the ratio of the optical cost to the electronic cost. The major drawback of all-optical architectures is that, for each possible incoming label, another hardware component is needed, resulting in hardly scalable switches. According to [20] label stripping could bring in a solution because the dimensions of the all-optical label swapping switch are exponentially dependent on the parameter B. Routing by use of label stripping decreases the number of bits in a label and thus the number of components needed. A comparison of the cost for all-optical nodes to the Elect. Header node is depicted in Fig. 9. Of most importance in these graphs are the intersections of the cost for the all-optical nodes with the Elect. Header node. Going from left to right in the graphs, from the intersection value P the all-optical node becomes cost beneficial to the Elect. Header node. In each of the graphs the cost function for the Elect. Header node is set out for different values of BR. Note that for the label stripping the label length is only 3 bits whereas for label swapping it should be 8 bits [20].

The evolution and improvement of the integration degree of optical components is a key factor on the total cost of an all-optical node. If it would be possible to integrate a number of components and meanwhile to reduce the number of FCCs, the cost will decrease. This issue has a special importance in the LASAGNE node architecture, based on SOA-MZIs as the main building block to implement the label switching functionalities.
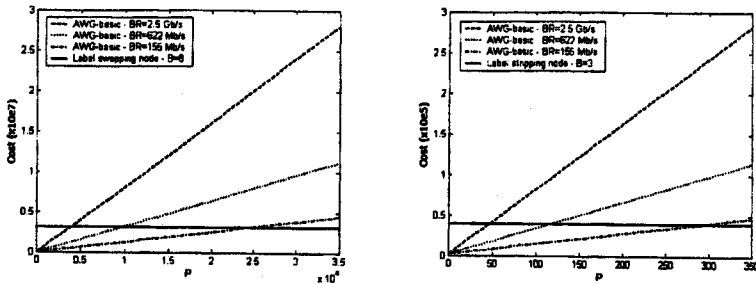
Fig. 9: Cost comparison for all-optical nodes and the Elect. Header node (based on an AWG) architecture with the parameters F = 4, W = 32, and B and BR dependent on the situation.

IV. SUMMARY AND CONCLUSIONS

Experimental results on clock recovery, packet-rate clock recovery and 2-bit label reading, as well as optical flip-flops, were provided employing optical gates as the basic building block. The obtained results were very promising towards the goal of building an all-optical photonic router for label-swapping networks. On the other hand, our cost study showed that the introduction of all-optical nodes will be dependent on integration possibilities and a reduction of the all-optical component cost. Packet routing based on label stripping forms a good solution to accelerate the possible introduction of all-optical nodes, although higher integration levels will be also crucial here.

Acknowledgements

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