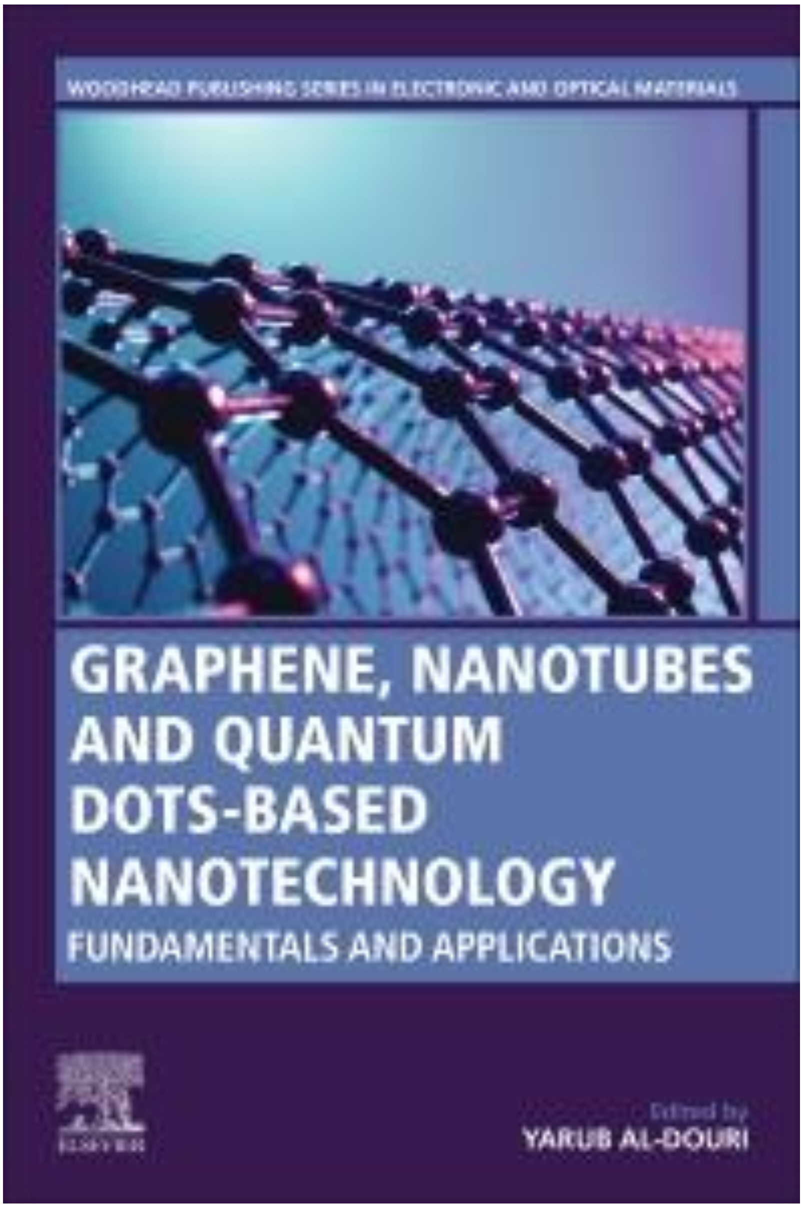

Graphene, Nanotubes and Quantum Dots-Based Nanotechnology

Fundamentals and Applications

Edited by:

Yarub Al-Douri

Woodhead Publishing Series in Electronic and Optical Materials

Graphene, Nanotubes and Quantum Dots-Based Nanotechnology

Fundamentals and Applications

Edited by

Yarub Al-Douri

Engineering Department, American University of Iraq-Sulaimani, Sulaimani, Kurdistan, Iraq; Department of Mechatronics Engineering, Faculty of Engineering and Natural Sciences, Bahcesehir University, Besiktas, Istanbul, Turkey; Nanotechnology and Catalysis Research Centre, University of Malaya, Kuala Lumpur, Malaysia

ELSEVIER

WP
WOODHEAD PUBLISHING
An imprint of Elsevier
elsevier.com/books-and-journals

Woodhead Publishing is an imprint of Elsevier
50 Hampshire Street, 5th Floor, Cambridge, MA 02139, United States
The Boulevard, Langford Lane, Kidlington, OX5 1GB, United Kingdom

Copyright © 2022 Elsevier Ltd. All rights reserved.

No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying, recording, or any information storage and retrieval system, without permission in writing from the publisher. Details on how to seek permission, further information about the Publisher's permissions policies and our arrangements with organizations such as the Copyright Clearance Center and the Copyright Licensing Agency, can be found at our website: www.elsevier.com/permissions.

This book and the individual contributions contained in it are protected under copyright by the Publisher (other than as may be noted herein).

Notices
Knowledge and best practice in this field are constantly changing. As new research and experience broaden our understanding, changes in research methods, professional practices, or medical treatment may become necessary.

Practitioners and researchers must always rely on their own experience and knowledge in evaluating and using any information, methods, compounds, or experiments described herein. In using such information or methods they should be mindful of their own safety and the safety of others, including parties for whom they have a professional responsibility.

To the fullest extent of the law, neither the Publisher nor the authors, contributors, or editors, assume any liability for any injury and/or damage to persons or property as a matter of products liability, negligence or otherwise, or from any use or operation of any methods, products, instructions, or ideas contained in the material herein.

ISBN: 978-0-323-85457-3

For Information on all Woodhead Publishing publications visit our website at https://www.elsevier.com/books-and-journals

Publisher: Matthew Deans
Acquisitions Editor: Kayla Dos Santos
Editorial Project Manager: Fernanda A. Oliveira
Production Project Manager: Kamesh Ramajogi
Cover Designer: Miles Hitchen

Working together to grow libraries in developing countries
www.elsevier.com • www.bookaid.org

Typeset by Aptara, New Delhi, India

Contents

Industrial applications of quantum dots

31

Nur Farha Shaafi and Saifful Kamaluddin Muzakir
Material Technology Programme, Faculty of Industrial Sciences and Technology, Universiti Malaysia Pahang, Kuantan, Pahang, Malaysia

31.1 Introduction

This chapter is divided into seven sections. The first section covers the scenario of electronic device fabrications which focuses on the number of transistors in an integrated circuit (IC) that have shown tremendous increment, that is, from 50 (in ca.1965) to 54,000,000,000 (in 2020) transistors per IC. Despite the ability to manipulate the dimension of the transistor that leads to a high-density IC design, the performance curve of the devices has shown decreasing gradient and approaching saturation point in the recent years. Therefore, a bottom-up strategy could be used which requires exploration of new materials in the form of QDs (which the properties are discussed in the third section) as building blocks of an electronic device. The second section discusses four synthesis procedures that able to produce high crystallinity and narrow size distributions of various QDs in large-scale, that is, colloidal, nonthermal plasma, solvothermal, and lithography synthesis methods. The physicochemical properties of the yield of each method could be optimized by manipulation of multiple synthesis parameters – indicates the chance for new findings in the areas.

The evolution of optoelectronic properties from bulk to QDs for selected materials is discussed in the third section. This chapter would shed fundamental insights before the readers could engage in deep discussions on advancement made in the energy generation technology (photovoltaic technology) – outlined in section four. Multiple exciton generation (MEG) is identified to be the key factor that would trigger the superior performance of a PV device. However, a suitable strategy that favor efficient excited-state electron generations, electron injections and regenerations should be planned via a combination of experimental and theoretical works. Three types of PV devices viz., crystalline, thin-film, and molecular absorber solar cells are discussed along with the best cell efficiencies reported by the National Renewable Energy Laboratory to date. The trend of usage of bulk materials and QDs in the R&D sector of three important industries viz., energy generation, energy storage, and energy emitting devices are discussed in the fifth section. Sequentially, a comparison between the output of theoretical and scale-up studies in terms of academic publications from the year 1993 to 2019 has been summarized in the final section. A strong correlation between the activities is observed; indicates that a bridge that connects the fundamental perspectives with the industry-scale applications has been established. Therefore, the growth of technologies in terms of number of processing machines per device, and efficiency exceeds the predictions made by Moore's Law could be expected.

Graphene, Nanotubes and Quantum Dots-Based Nanotechnology: Fundamentals and Applications.
DOI: https://doi.org/10.1016/B978-0-323-85457-3.00007-4
Copyright © 2022 Elsevier Ltd. All rights reserved.

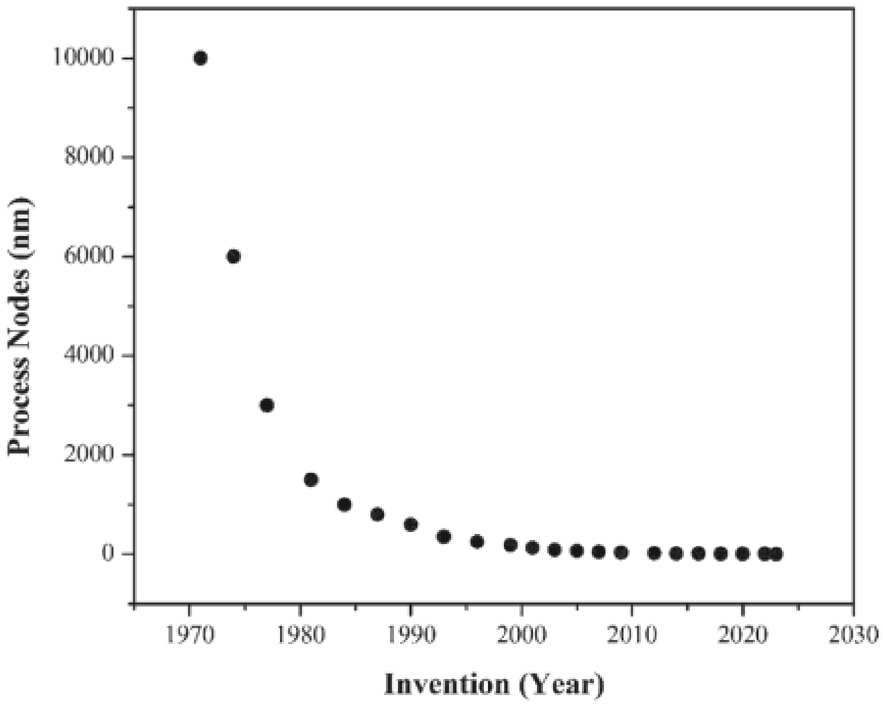

Figure 31.1 The dimensions of fabricated electrical and electronic chips from 1970 to 2020.

31.2 Fabrications of device: From bulk to nanosized materials

The fabrication of silicon-based metal oxide semiconductor (MOS) which is mainly used in integrated circuit (IC) of electrical and electronic devices involves multiple stages viz., photolithography, surface passivation, oxidation, diffusion, and junction isolation. The fabrication technologies have showed improvement from the perspective of dimensions, for example, size and spacing features in a layer of chip, and the density of chips in a single wafer. Fig. 31.1 shows the advancement of chip processing technology which indicates reduction of dimensions and features of the fabricated chip on a wafer from 1970 to 2020 [1–19].

The dimensions of technology node has been scaled down from 10,000 nm which was fabricated using metal oxide semiconductor field effect transistor (MOSFET) process in 1971 [20] to 5 nm which was fabricated using multi-gate MOSFET (MuGFET) with fin field-effect transistors (FinFETs) in 2020 [19]. Note that a further reduction of dimension is predicted in 2022 and 2023 which technology nodes of 3 and 2 nm could be materialized respectively. The size reduction resulted low consumption of raw materials, increment number of fabricated IC per unit area, reduction of current used by each transistor (while maintaining the operational frequency of the IC), reduction of heat generation, and reduction of power consumption [21]; which therefore, the device efficiency per production cost is increased. In 1965, an empirical observation made by Gordon E. Moore has predicted a sudden increment of number of transistors that could

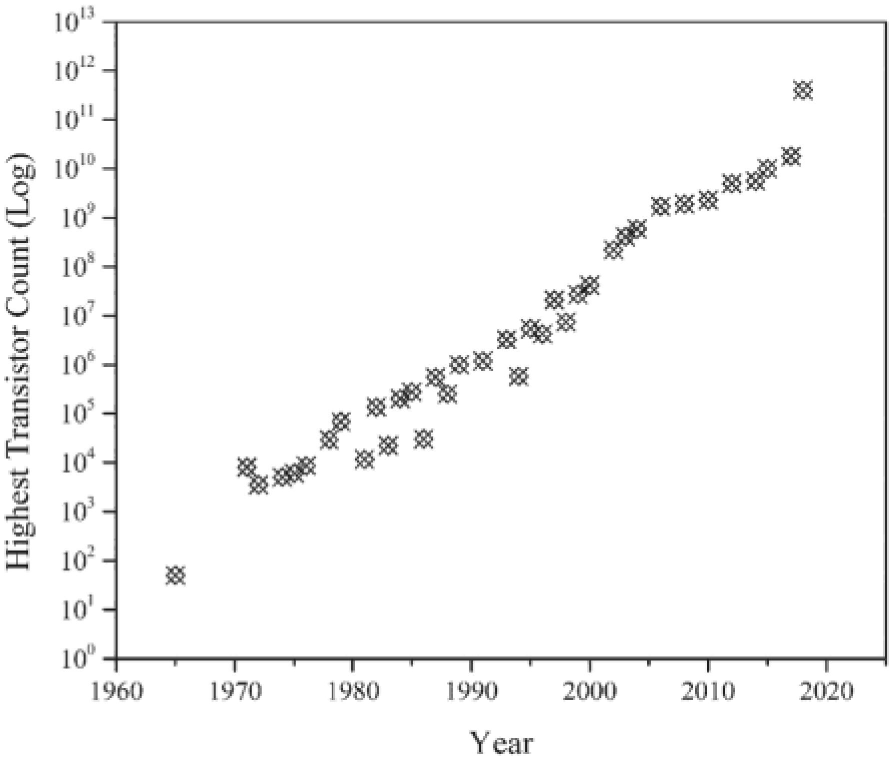

Figure 31.2 The highest number of transistors on IC in specific year (from 1971 to 2018).

be fabricated in a dense IC in every two years [22]. The report stated that a significant shift could be observed from 50 to 65,000 transistors per IC within 10 years – which the goal has been achieved in 1979, exceeds the predicted number ca. 68,000 [23] (Fig. 31.2).

In 1975, however, Moore has suggested that the slope of Moore's graph would start to decrease in 1980 due to limitation of circuit design for a dense device structure. He predicted that the number of transistors in the year 1985 would reach 16,000,000 per IC. Despite the promising number, only 275,000 transistors per IC could be materialized in 1985 [24]. Nonetheless, Moore's prediction has been the main motivation behind the advancement made in the IC fabrications, which have boosted almost every field of technology, for example, data storage, display, and sensors. A surge in demand for information and communication technology (ICT) has been reported in the U.S in the 1990s due to rapid economic growth and successful investment [25]. Fig. 31.3 shows multiple spikes of trends in various research and development fields, for example, photolithography, diffusion, ion implantation, etching, and planarization could be observed in the early-to-mid-1990s. Despite the design limitation, the growth of IC technology has never been ceased. The highest number of transistors that could be fitted in a single IC is ca. 54,000,000,000 has been recorded in 2020 [26].

Despite increasing number of transistors, the performance of the IC, that is, single-thread performance, frequency, typical power, number of cores shows saturated trends since mid-2000 [27]. Fig. 31.4 shows the drawback of a typical nanosized Si-based

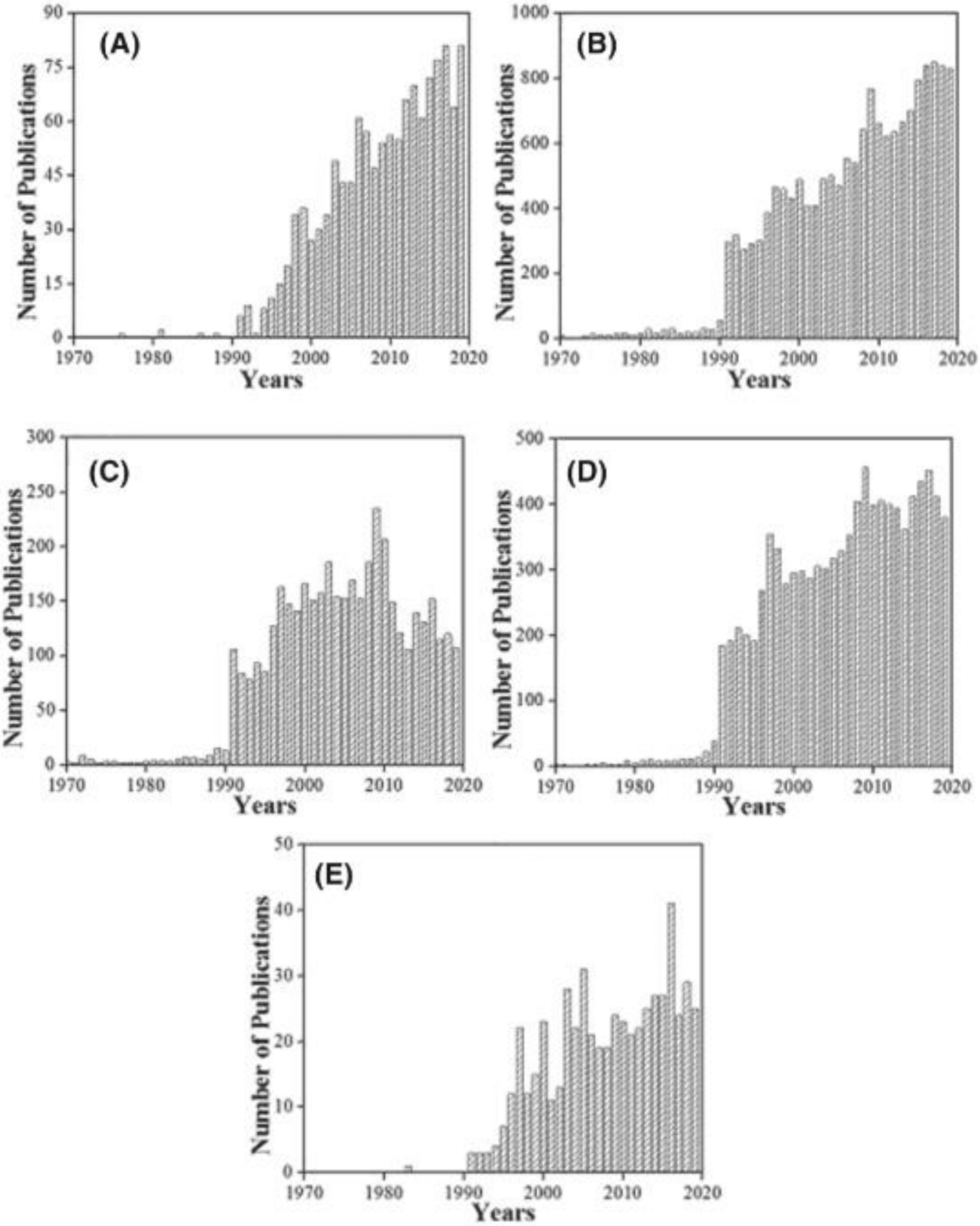

Figure 31.3 Number of papers published from 1970 to 2019; generated from ISI Web of Science using keywords (a) "photolithography" and "semiconductor," (b) "diffusion" and "semiconductor," (c) "ion implantation" and "semiconductor," (d) "etching" and "semiconductor," and (e) "planarization," and "semiconductor."

transistor that has contributed to the trends. Upon size reduction of the transistors within the scale of tens of nanometers, the thickness of SiO_2 (gate oxide) has become smaller than the limit of an electron tunnelling (ca. 2 nm) which has caused unacceptable amount of current leakage [28]. The search for solution from the perspective of

Index

Page numbers followed by "*f*" and "*t*" indicate, figures and tables respectively.

H

R

S

W

X