Robuuste plaatsbepaling met submeterresolutie
steunend op aankomsttijdmetingen rond 2.4 GHz:
haalbaarheidsstudie en realisatie
van een CMOS-ontvanger met laag vermogen

A Robust 2.4 GHz Time-of-Arrival Based Ranging System
with Sub-Meter Accuracy: Feasibility Study and Realization
of Low Power CMOS Receiver

Guy Torfs

Promotoren: prof. dr. ir. J. Vandewege, prof. dr. ir. J. Bauwelinck
Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Informatietechnologie
Voorzitter: prof. dr. ir. D. De Zutter
Faculteit Ingenieurswetenschappen en Architectuur
Academiejaar 2011 - 2012

UNIVERSITEIT
GENT

ISBN 978-90-8578-524-8
NUR 959
Wettelijk depot: D/2012/10.500/50

Dankwoord

Dit proefschrift is het resultaat van bijna 5 jaar onderzoek uitgevoerd als medewerker van het labo INTEC_design van de universiteit Gent. Zoals gekend, kleurt het avondrood van de ondergang alles met de bekoring van de nostalgie, wat dit de ideale plaats maakt om een aantal personen die hebben bijgedragen tot het welslagen van dit werk te bedanken.

Zo wens ik prof. dr. ir. Daniël De Zutter, voorzitter van de vakgroep informatie technologie, te bedanken voor de aangeboden faciliteiten en omkadering.

Het onderzoek, beschreven in dit proefstuk, kaderde in het ELOCA en het ALOHA project. Ik wens het IWT-Vlaanderen (Instituut voor de aanmoediging van Innovatie door Wetenschap en Technologie in Vlaanderen) te bedanken voor hun steun. Verder wens ik ook de andere onderzoekspartner, Essensium n.v., te bedanken en meer in het bijzonder ir. Frederic Stubbe, dr. ir. Huub Tubbax en ir. Peter Spiessens voor de nauwe samenwerking en nuttige discussies op zowel architecturaal vlak als in de gedetailleerde transistor implementaties.

Het INTEC_design laboratorium biedt jonge doctoraatsstudenten de mogelijkheid om zich te vervolmaken in het ontwerpvak. Door nauw samen te werken met verschillende industriële partners wordt een breed gamma van onderzoeksonderwerpen aangeboord en krijgt de student de mogelijkheid om een zee van kennis te vergaren, hoewel er hier en daar nog gebaggerd kan worden. Prof. dr. ir. Jan Vandewege en prof. dr. ir. Johan Bauwelinck, beide promotoren van dit proefschrift, leiden dit labo en ik wens hen te danken voor het vertrouwen en de verschillende ideeën die zij aangereikt hebben alsmede voor het nalezen van deze tekst.

Voorts wens ik mijn collega's van de INTEC_designgroup te bedanken voor de aangename en prettige samenwerking gedurende de laatste jaren. In het bijzonder dank ik dr. ir. Xin Yin en ir. Zhisheng Li voor hun bijdrage aan de ontwikkelde borden en chips, Ing. Jan Gillis voor het frezen van test borden

en ontwikkelen van test software, ir. Jochen Verbrugghe voor zijn inzichten in transitor ontwerp en ir. Christophe Van Praet voor het uitgebreid en kritisch nalezen van deze tekst.

Ik dank mijn ouders om mij de mogelijkheid te bieden dit ingenieursavontuur aan te vangen, wat uiteindelijk geleid heeft tot dit werk en mijn vriendin Charlotte, die in het zicht van een nakende tape-out vele nachten alleen thuis om mij gewacht heeft.

Tot slot wens ik alle mensen, die mij op een of andere manier geholpen of gesteund hebben, te danken.

Gent, mei 2012

Guy Torfs

Table of Contents

Glossary

A

AC Alternating Current
ADC Analog to Digital Converter
ADS Advanced Design System
AGC Automatic Gain Control
AOA Angle Of Arrival
ASIC Application Specific Integrated Circuit

C

CMOS Complementary Metal Oxide Semiconductor

D

DAC Digital to Analog Converter
DC Direct Current
DIP Dual In-line Package
DNL Differential Non-Linearity
DSP Digital Signal Processing

E

EM Electro-Magnetic
ENOB Effective Number Of Bits
ENR Excess Noise Ratio

ESD Electrostatic Discharge

F

FCC Federal Communications Commission
FEM Front End Module
FIB Focussed Ion Beam
FOM Figure Of Merrit
FPGA Field-Programmable Gate Array
FR4 Flame Retardant 4

G

GPIO General Purpose Input Output
GPS Global Positioning System

I

IC Inversion Coefficient
ID Drain current
IEEE Institute of Electrical and Electronics Engineers
IF Intermediate Frequency
IIP3 Input-referred 3rd order Intercept Point
IM3 3rd order intermodulation
INL Integral Non-Linearity
IQ In phase – Quadrature
ISM Industrial, Scientific and Medical
IWT Agentschap voor Innovatie door Wetenschap en Technologie – Agency for Innovation by Science and Technology

L

LNA Low Noise Amplifier
LO Local Oscillator

LOS Line Of Sight
LPC Low Pin Count interface
LSB Least Significant Bit
LVDS Low Voltage Differential Signaling

M

MIM Metal-Insulator-Metal
MIT Massachusetts Institute of Technology
MOS Metal-Oxide-Semiconductor
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

N

NF Noise Figure
NLOS Non-Line Of Sight
NMOS N-type MOSFET
NRE Non-Recurring Engineering

O

OFDM Orthogonal Frequency-Division Multiplexing
OTA Operational Transconductance Amplifier

P

PA Power Amplifier
PCB Printed Circuit Board
PLL Phase Locked Loop
PMOS P-type MOSFET

R

RF Radio Frequency
RFID Radio Frequency IDentification
ROM Read-Only Memory
RSS Received Signal Strength
RSSI Received Signal Strength Indication
RX Receiver

S

SAW Surface Acoustic Wave
SNDR Signal to Noise and Distortion Ratio
SNR Signal to Noise Ratio
SoC System on Chip
SPI Serial Peripheral Interface bus

T

TDOA Time Difference of Arrival
TE Transverse Electric
TIA TransImpedance Amplifier
TM Transverse Magnetic
TOA Time Of Arrival
TWR Two Way Ranging
TX Transmitter

U

UMTS Universal Mobile Telecommunications System
UNII Unlicensed National Information Infrastructure
UWB Ultra Wide Band

V

VGA Variable Gain Amplifier
VNA Vector Network Analyzer

W

WLAN Wireless Local Area Network

Nederlandstalige samenvatting –Dutch Summary–

Recente draadloze sensor netwerken, bestaande uit een aantal onderling verbonden nodes, verzamelen verschillende soorten informatie. Voorbeelden hiervan omvatten meteorologische parameters zoals de temperatuur of de status van machines in een industriële omgeving. Naast de gemeten parameter is de locatie, waar de informatie verzameld is, een belangerijk onderdeel van de informatie zelf. Voor sommige toepassingen, zoals het volgen van personen of goederen, is de plaatsinformatie zelfs de meest belangrijke en mogelijkmakende factor.

De basistechnologie, die nodig is om de positie van een sensor te bepalen, is de meettechnologie die de afstand tot een gekend referentiepunt schat. Door verschillende van deze afstandsmetingen te combineren, is het mogelijk de absolute locatie van de node te berekenen. Er bestaan reeds verschillende technieken die toelaten de positie van een apparaat te bepalen, maar deze hebben elk een aantal onvolkomenheden. GPS werkt bijvoorbeeld enkel buitenshuis en werkt niet wanneer te veel multipad reflecties aanwezig zijn, wat een gevolg is van de kleine bandbreedte en de lange correlatietijden. Andere technieken die het ontvangen zendvermogen meten, zijn slechts in staat een ruwe schatting te geven en hangen sterk af van een vooraf opgestelde blauwdruk. Een meer belovende techniek voor positiebepaling binnenshuis maakt gebruik van ultra-breedbandige (UWB) signalen. De grote bandbreedte van deze signalen vertaalt zich in korte pulsen in het tijdsdomein, die gebruikt kunnen worden voor een aankomsttijd (TOA) gebaseerde meetmethode. Deze korte tijdspulsen zijn immuun voor multipad reflecties maar er is enkel een beperkt zendvermogen beschikbaar, bepaald door de spectrale regelgeving. Wanneer dit gecombineerd wordt met de hoge werkfrequentie, resulteert dit in een korte werkafstand. Verder veroorzaakt de hoge bandbreedte een stijging van de ingangsruis wat dan weer nadelig is voor het linkbudget.

Door een relatief lage radiofrequentie (RF) (2.4 GHz) en een hoge bandbreedte ($\approx$200 MHz) te gebruiken, wordt robuuste, mulitipad resistente, TOA gebaseerd afstandsbepaling mogelijk over een afstand van 300 meter met submeter nauwkeurigheid. De lage frequentie zorgt voor een hoog linkbudget terwijl de hoge bandbreedte voldoende nauwkeurigheid verzekert bij de afstandsbepaling, sinds de te verwachten fout in eerste benadering omgekeerd evenredig is met de bandbreedte. In een eerste fase werd dit innovatieve systeem geëvalueerd met behulp van met commerciële componenten, en van een aangepaste 2.4 GHz draadloze, lokale netwerk (WLAN) zendontvanger (TX/RX). De start van het WLAN pakket wordt vervormd tot een steile flank, wat resulteert in een puls met hoge bandbreedte aan de start van elk pakket. Sinds enkel de start van het pakket de steile flank vertoont, wordt de spectrale regelgeving niet geschonden zolang de herhalingsfrequentie laag genoeg is. De steile flank werd gemaakt door een GaAs schakelaar voor de WLAN vermogensversterker (PA) te plaatsen, wat resulteert in een stijgtijd van 3.25 ns aan het begin van elk pakket. Dit afstandsbepalingspakket wordt vervolgens verzonden naar een referentie node, die de informatie ontvangt door middel van een voortrap met grote bandbreedte. Deze ontvanger bestaat uit twee lage-ruisversterkers, een I/Q menger, basisband filters en versterkers en een snelle 8 bit 500 Msps analoog naar digitaal omvormer (ADC). De bemonsterde informatie wordt vervolgens verder verwerkt in het digitale domein. Deze demonstrator toont de mogelijkheid van nauwkeurige afstandsbepaling aan: een submeter nauwkeurigheid met één enkele meting die verbeterd kan worden door uitmiddeling zodat de fout nadert tot de golflengte van de draaggolf (ongeveer 12.5 cm @ 2.4 GHz). Niettegenstaande de goede nauwkeurigheid die behaald wordt, is het getoonde prototype enkel bruikbaar in een beperkt aantal toepassingen. Dit door de hoge kost van de componenten en het hoge energieverbruik (10 Watt). Om het energieverbruik en de kost van de componenten te verminderen, wordt het gedemonstreerde systeem als startpunt gekozen voor verdere integratie van het systeem op silicium.

In het volgende deel van dit proefstuk wordt de integratie van de CMOS voortrap beschreven, één van de delen met het hoogste energieverbruik. Het ontwerp wordt geïmplementeerd in een 0.13 μm CMOS technologie en is opgedeeld in twee delen: de hoogfrequente lage-ruisversterker (LNA) en de I/Q menger, en de basisband filters en de ADC. De LNA en de menger zijn ontworpen met behulp van een gestructureerde ontwerpsmethodologie. Dit resulteerde in een compact en laagvermogen ontwerp, gerealiseerd in een korte ontwerpstijd. Slimme technieken op architecturaal niveau maak-

ten het mogelijk om de TX/RX schakelaar en extra spoelen van het LNA ingangsaanpassingsnetwerk te verwijderen door de drainuitgangsspoel van de vermogensversterker te hergebruiken. De cascade van de LNA en de menger resulteerde in een ruisgetal van $7.5\ \mathrm{dB}$, $28\ \mathrm{dB}$ versterking en een bandbreedte van $250\ \mathrm{MHz}$. Dit alles verbruikt slechts $10\ \mathrm{mW}$.

Door de grote bandbreedte van de ontvanger wordt sterke interferentie van nabijgelegen UMTS zenders verwacht. Om deze stoorsignalen uit het basisband spectrum te verwijderen en de robuustheid van de ontvanger te garanderen, zonder de nauwkeurigheid van de afstandsbepaling te schaden (dus door voldoende bandbreedte te garanderen), werd een scherp 10e orde sourcevolger gebaseerd filter ontworpen. Source-volger gebaseerde filters zijn inherent lineair door de ingebouwde terugkoppeling tussen gate en source wat een laagvermogen realizatie toelaat. Een minpunt van een sourcevolger is zijn beperkte spanningsversterking (typisch 0.7). Door kruiselingsgekoppelde transistoren toe te voegen, kan de versterking verhoogd worden, wat dan weer de ruisbijdrage van volgende secties vermindert. In de zoektocht naar lineaire sourcevolger gebaseerde filters bleek dat harde afknijpingsverschijnselen voorkwamen wanneer het filter aangestuurd werd met sterke signalen. Een alternatief terugkoppelingsmechanisme werd voorgesteld om het lineair ingangsgebied van het filter uit te breiden en om de sterke afknijpingsverschijnselen te onderdrukken. Het voorgestelde I/Q basisbandfilter verbruikt $2\ \mathrm{mW}$, heeft een bandbreedte van $130\ \mathrm{MHz}$ en een onderdrukking van $33\ \mathrm{dB}$ op $225\ \mathrm{MHz}$.

De snelle ADC is het onderdeel dat het meeste energie verbruikt in de voortrap gebouwd met discrete componenten. Om dit vermogen drastisch te doen dalen werd een 4 bit flits ADC ontwikkeld. Voorgaande ontwerpen toonden aan dat vergelijkers met ingebouwde drempelspanning leden onder terugslagruis. Deze terugslagruis veroorzaakt geheugeneffecten als het signaal wordt aangestuurd vanuit een bron met een te hoge uitgangsimpedantie zodat een breedbandige buffer met lage uitgangsimpedantie, die veel vermogen verbruikt, noodzakelijk is. Om de terugslagruis te verminderen is een nieuwe vergelijker voorgesteld, die door het verminderen van de terugslagruis een meer nauwkeurige kalibrering toelaat. Door 15 van deze vergelijkers samen te voegen tot een 4 bit ADC, werd een ontwerp bekomen dat slechts $4.3\ \mathrm{mW}$ verbruikte op een werkfrequentie van $700\ \mathrm{Msps}$ met een performantiemaat (FOM) van slechts $0.57\ \mathrm{pJ}$ per monster en per effictieve bit.

Om de ontvangersketen te vervolledigen, wordt in het laatste hoofdstuk

van dit proefschrif het ontwerp en de implementatie van een differentiële, volle golflengte lusantenne beschreven. De bandbreedte van de antenne is voldoende groot gemaakt om de ontvangst van afstandsbepalingssignalen mogelijk te maken en door zijn magnetische eigenschappen wordt de invloed van storingen in het nabije veld gereduceerd. Door de differentiële opbouw van de antenne wordt de nood aan extra omzettingen van gebalanceerde naar ongebalanceerde signalen vermeden. Dit resulteert in een hogere versterking en lagere ruis van de gehele zendontvanger.

De combinatie van al deze bouwblokken maakt het mogelijk een volledige voortrap voor een afstandsbepalingsontvanger te bouwen. Dit geheel brengt de initiële demonstrator een stap dichter bij een implementatie met laag vermogen en een beperkte prijs.

English summary

Nowadays, wireless sensor networks, consisting of multiple interconnected nodes, gather different kinds of information, for example meteorological parameters such as temperature or machine health status parameters in an industrial setup. Besides the measured parameter, the location where the information is gathered, is a crucial part of the information itself. For some applications, such as people and asset tracking systems, location information is even the most important and enabling factor.

The basic technology needed to determine the position of a sensor is the ranging technology, which estimates the distance to known reference points. By combining several distance measurements, the absolute location of the node can be calculated. There already exist different technologies to determine the position of a device, but all of these have certain limitations. The GPS, for example, only works in outdoor scenarios and isn't capable of handling multipath reflections due to low signal bandwidth and long correlation times. Other techniques make use of received signal strength measurements, which can only providing a rough estimate, and rely on extensive fingerprinting. A more promising technique for indoor applications makes use of UWB signals. The wide bandwidth translates to short pulses in time domain, and allows for a time-of-arrival (TOA) based ranging method that makes the ranging signals immune for multipath reflections. However, due to spectral regulations, only limited transmit power is allowed. Combined with the high operating frequency, this results in a relatively short operating range. Furthermore, the high bandwidth increases the input noise which is a disadvantage for the link budget.

By using a relatively low (2.4 GHz) RF frequency and a high ($\approx$200 MHz) bandwidth, a sub-meter accurate, multipath reflection robust, TOA based ranging system is shown to operate over 300 meter. The low frequency offers a high link budget while the high bandwidth ensures the ranging accuracy, since, in first order, the expected error is inversely proportional to the bandwidth. This system, prototyped on a PCB with off-the-shelf com-

ponents, makes use of a modified 2.4 GHz WLAN transceiver. The onset of a WLAN packet is modified to produce a steep edge, generating a high bandwidth pulse at the start of each packet. Since only the start of the packet has a steep edge, spectral regulations aren't violated as long as the repetition rate is low. The steep edge is generated by a fast GaAs switch placed in front of the WLAN PA, which offers rise times of 3.25 ns at the beginning of the packet. This ranging packet is transmitted to a reference node, capturing the information with a high bandwidth front-end, consisting of two LNA's, a I/Q mixer, baseband filters and amplifiers and a fast 8 bit 500 Msps ADC. The sampled information is further processed in the digital domain. This first prototype yielded a single shot accuracy of less than one meter. After averaging, the error could be minimized downto the carrier wavelength (about 12.5 cm @ 2.4 GHz). Although good ranging accuracy is achieved, the demonstrated prototype is only practical in a limited number of situations due to the high component cost and high power consumption (10 Watt). To lower the power consumption and component count, the proof-of-concept is used as starting point for silicon integration of the system.

Further on, the CMOS integration of the front-end, one of the most power consuming parts, is described. A 0.13 μm CMOS technology is used to implement the design, which is divided into two parts: the high frequency LNA and I/Q mixer, and the baseband filters and ADC. The LNA and mixer are designed via a structured design methodology and resulted in a compact low power design achieved via a short design cycle. Clever architectural techniques made it possible to remove a full TX/RX switch and extra inductors from the LNA input matching network, by reusing the drain output inductor of the PA. The cascade of LNA and mixer resulted in a NF of 7.5 dB, 28 dB gain and a bandwidth of 250 MHz while only consuming 10 mW.

Due to the high receiver bandwidth, high interference of nearby UMTS transmitters is expected. To remove these signals from the baseband spectrum and thus, to ensure the robustness of the receiver, while still enabling accurate ranging (thus preserving enough bandwidth), a steep 10th order source-follower based filter is implemented.
Source-follower filters are inherently linear devices due to the built-in feedback between gate and source, allowing low power linear operation. A downside of a source follower is its limited voltage gain (0.7 typical). By adding an extra crosscoupling transistor, the gain can be increased, reducing the noise contribution of the subsequent stages. The search for a linear

source-follower based filter showed that hard clipping occurs when the filter is driven with strong signals. An alternative feedback structure is proposed to extend the linear input range and to reduce the hard clipping effects of the source follower filter. The proposed I/Q baseband filters consume $2\ \mathrm{mW}$, have a bandwidth of $130\ \mathrm{MHz}$ and an attenuation of $33\ \mathrm{dB}$ at $225\ \mathrm{MHz}$.

The high-speed ADC is the most power consuming block of the proof-of-concept PCB. To reduce the power consumption dramatically, a low power 4 bit flash ADC is developed. Previous designs showed the use of comparators with built-in threshold voltages but suffered from severe kickback noise. This kickback noise can result in memory effects when the signal source output impedance is too high, requiring a high power broadband input buffer. To reduce the kickback noise, a novel comparator is proposed, which due to the reduced kickback noise, enabled a finer calibration. Combining 15 of such comparators in a 4 bit ADC, led to a $4.3\ \mathrm{mW}$ design working at $700\ \mathrm{Msps}$ with a FOM of $0.57\ \mathrm{pJ}$.

To complete the receiver chain, the last chapter of this dissertation presents the design and implementation of a differential full wave loop antenna. The antenna is made sufficiently broadband to allow reception of ranging signals and makes use of its magnetic properties to reduce the influence of disturbances in its near field. The differential nature of the antenna removes the need for on or off-chip baluns, allowing higher gain and lower noise of the overall TRX.

The combination of all these building blocks realizes a complete ranging receiver front-end, bringing the initial proof-of-concept PCB one step closer towards a low power and low cost implementation.

List of publications

Publications in international journals

1. G. Colman, G. Torfs, J. Bauwelinck, and J. Vandewege. Low-cost circuit incorporates mixing and amplifying functions. *EDN*, 53(14):77, JUL 10 2008

2. X. Yin, J. Bauwelinck, G. Torfs, P. Demuytere, J. Vandewege, H. Tubbax, J. Wouters, P. Debacker, J. Olbrechts, P. Spiessens, F. Stubbe, and J. Danneels. Embedded ranging system in ISM band. *Electronics Letters*, 44(17):1043–1044, AUG 14 2008

3. J. Bauwelinck, E. De Backer, C. Melange, G. Torfs, P. Ossieur, Xing-Zhi Qiu, J. Vandewege, and S. Horvath. A 1024-QAM Analog Front-End for Broadband Powerline Communication Up to 60 MHz. *IEEE Journal of Solid-State Circuits*, 44(5):1477 –1485, May 2009

4. G. Torfs, Z. Li, J. Bauwelinck, X. Yin, J. Vandewege, and G. Van Der Plas. A Low-Power Reduced Kick-Back Comparator with Improved Calibration for High-Speed Flash ADCs. *IEICE Transactions on Electronics*, E92C(10):1328–1330, OCT 2009

5. G. Torfs, Z. Li, J. Bauwelinck, X. Yin, G. Van der Plas, and J. Vandewege. Low-power 4-bit flash analogue to digital converter for ranging applications. *Electronics Letters*, 47(1):20–21, JAN 6 2011

6. G. Torfs, Z. Li, J. Bauwelinck, J. Vandewege, and P. Spiessens. A novel large input range source-follower based filter architecture. *IEICE Electronics Express*, 8(24):2025–2028, 2011

7. R. Pierco, Z. Li, G. Torfs, X. Yin, J. Bauwelinck, and X.Z. Qiu. Diode string with reduced clamping-voltage for ESD-protection of RF-circuits. *Electronics Letters*, 48(6):317 –318, 2012

8. Z. Li, G. Torfs, J. Bauwelinck, X. Yin, J. Vandewege, C. Van Praet, P. Spiessens, H. Tubbax, and F. Stubbe. A 2.45-GHz + 20-dBm Fast Switching Class-E Power Amplifier With 43% PAE and a 18-dB-Wide Power Range in 0.18- μm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, PP(99):1 –5, 2012

9. Z. Li, J. Bauwelinck, G. Torfs, X. Yin, and J. Vandewege. A New Common-Mode Stabilization Method for a CMOS Cascode Class-E Power Amplifier with Driver Stage . *IEICE Transactions on Electronics*, E95C(4):765–767, APRIL 2012

Publications in international conferences

1. H. Tubbax, J. Wouters, J. Olbrechts, P. Debacker, P. Spiessens, F. Stubbe, J. Danneels, J. Bauwelinck, X. Yin, G. Torfs, and J. Vandewege. A Novel Ranging Technique for 2.4GHz ISM Band. In *The IASTED International Conference on Sensor Networks*, Sept.-Oct. 2008

2. H. Tubbax, J. Wouters, J. Olbrechts, P. Debacker, P. Spiessens, F. Stubbe, J. Danneels, J. Bauwelinck, Xin Yin, G. Torfs, and J. Vandewege. A novel positioning technique for 2.4GHz ISM band. In *IEEE Radio and Wireless Symposium*, pages 667–70, 2009

Publications in national conferences

1. G. Torfs, X. Yin, Z. Li, J. Bauwelinck, and J. Vandewege. Embedded indoor ranging system with decimeter accuracy in the 2.4 GHz ISM band . In *9e UGent-FirW Doctoraatssymposium*, pages 208–209, 2008

2. G. Torfs, J. Vandewege, and J. Bauwelinck. Integrated subblocks for RF ranging applications. In *11e UGent-FirW Doctoraatssymposium*, page 160, 2010

Patents

1. G. Van der plas, P. Nuzzo, F. De Bernardinis, J. Bauwelinck, Z. Li, G. Torfs, J. Vandewege, and X. Yin. A/D Converter Comprising a Voltage Comparator Device. Continuation in part of WO2007088175, US7652600 (B2), granted on 26 Jan. 2010

2. J. Bauwelinck, Z. Li, G. Torfs, J. Vandewege, and X. Yin. Amplifier Circuit for a Ranging Transceiver. EP 2 429 075 (A1), published on 14 Mar. 2012

1 Introduction

1.1 Background

In wireless sensor networks, sensors convert physical parameters like pressure and temperature to electrical information and transfer this wirelessly to an application server where it can be further processed for the benefit of its users. Besides the sensor information, the accurate location where this information is generated, adds extra value to the sensor read-out. In some applications, it can even be the most valuable information communicated (e.g. all asset and people tracking applications). So far, most of the activity in the domain of wireless sensor networking has focused on the aspect of (low power) communication of sensor information while the requirements for the sensor to acquire accurate position information were neglected. Positioning is considered to be an afterthought and hence the performance, i.e. position accuracy is useless for most applications.

One of the basic technologies for the sensor to accurately determine its position is the ranging technology. Ranging technology estimates the distance between two points, one being the sensor node, the other being a node with a known location. Combining several ranging measurements provides several distances to known, fixed devices, from which positioning algorithms provide a good estimation of the most likely absolute coordinates of the sensor.

Figure 1.1 shows a classical setup to determine the location of a floating

node. Three basestations use a ranging method to measure the distance to the floating node, yielding the distances R_1, R_2 and R_3. These allow to determine a region in which the floating node is likely to be found. To determine the position in a plane, two base stations are insufficient, yielding 2 different intersect points on 2 circles. A third one solves the ambiguity problem and gives extra redundancy, used to estimated and to compensate measurement errors.

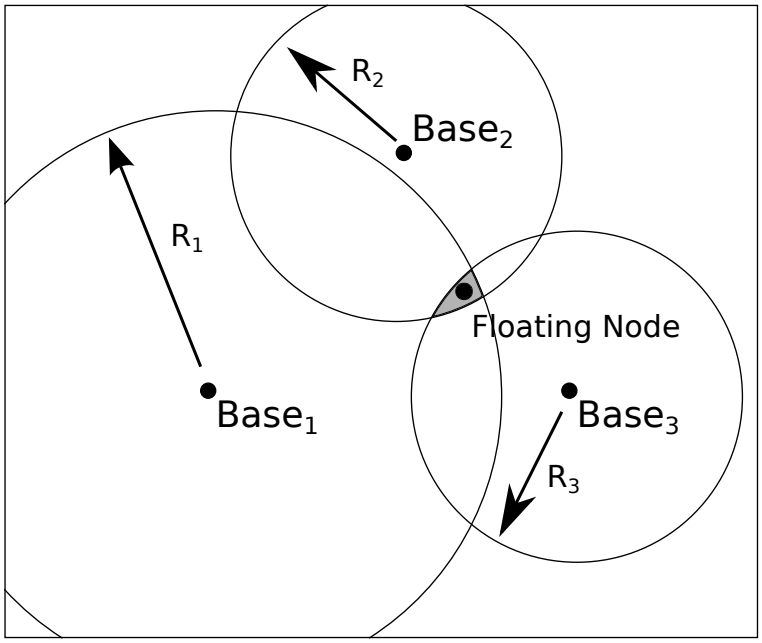


Figure 1.1: Ranging based location determination.

Well-established technologies for position determination are mostly addressing outdoor scenarios, the Global Positioning System (GPS) being the most widespread and well known example. While these techniques have adequate performance outdoors when sufficiently strong line-of-sight signals are available, they suffer from low accuracy in indoor environments. The key reason for this performance degradation is that received signals consist of multiple superimposed, attenuated, delayed and phase rotated copies of the line-of-sight signals caused by reflections [1]. Especially due to the narrow-band nature of the transmitted signals, these copies have a wide span in the time-domain and hence tend to overlap. As a result, copies having travelled several meters more typically can not be distin-

guished from the line-of-sight path by the receiver, thus introduce errors in the position estimation of the same order of magnitude.

Figure 1.2 shows the effect of multipath reflections on a narrowband ranging system. If a weak line-of-sight signal is followed by a strong reflected signal, the narrowband filtering will result in a signal of which the maximum is aligned with the reflected signal. This time shift in signal will result in ranging errors.

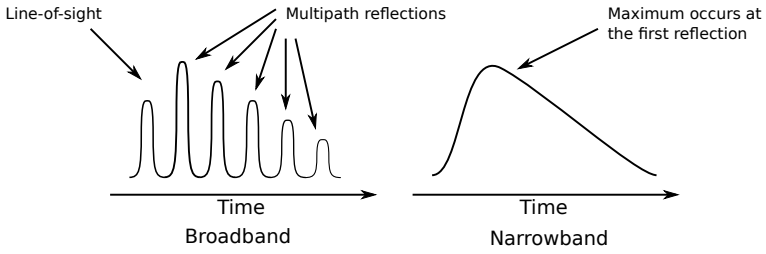


Figure 1.2: Effect on the ranging accuracy due to multipath reflections.

1.2 Overview of the work

This dissertation describes the research the author has conducted during the past 4 years at the INTEC_design laboratory of the department of information technology (INTEC) at Ghent University.

The INTEC_design group offers young engineers the opportunity to skill themselves in the design of electronical systems at the PhD level. By collaborating with industrial partners, there is an opportunity to solve real-world problems. In this way the training is not limited to a pure theoretical study but comprises the system study, integration and realization of first prototypes, and concludes with the final testing and demonstration of the new system concepts.

This work in particular is based on the research performed in the framework of the IWT ELOCA (Embedded LOCation Awareness in wireless modules) and IWT ALOHA (Advanced LOcation with High Accuracy) project. Both projects were financed by the Agentschap voor Innovatie door Wetenschap en Technologie – Agency for Innovation by Science and Technology (IWT) and have been conducted in close cooperation with IMEC spin-off Essensium. Essensium is a fabless chip company, situated in Leuven and specialized in system-on-chip Application Specific Integrated Circuit (ASIC) design, for low power solutions and wireless communications.

The IWT project ELOCA focused on the basic technology for accurate ranging in indoor environments. The proof-of-concept ranging transceiver, developed using commercially available components, showed a significant improvement in precision (< 1 m resolution) compared to existing technologies, thanks to the high dynamic range of the transceiver and accurate real-time positioning algorithms. Besides the realization of the transceiver, coexistence with very low mutual interference with ongoing data traffic in the same frequency band was demonstrated. In this project, it was also shown that it is feasible to integrate the functionality on chip, paving the way for a follow-up project, ALOHA.

The IWT ALOHA project is a continuation of the ELOCA project. ALOHA targeted the low cost and low power silicon integration of the ranging transceiver functions, together with data communication functions, in a single front-end. This is mostly driven by the demands for autonomy (so low power) and miniaturization (portability). Our research in this project was mainly focused on the Radio Frequency (RF) building blocks of the transmitter and the receiver, including the antenna design and the co-optimization of the antenna with the RF circuits. The transmitter design will be discussed in detail in the PhD of our colleague Zhisheng Li.

1.3 Outline of the dissertation

This dissertation is organized as follows. Chapter 2 provides an overview of existing ranging technologies and discusses their advantages and disadvantages with respect to accurate indoor ranging. Based on these insights a new ranging technique, patented by Essensium, is presented. This new concept combines the advantages of both broadband and narrowband signals to achieve a high ranging accuracy in presence of strong multipath reflections, to achieve a good link budget and to be compliant with the spectral regulations. The fundamental idea is that also relatively narrowband radios such as those used in Wireless Local Area Network (WLAN) products exhibit and/or can be stimulated to generate wideband transient signals. And these wideband signals can then be leveraged for improved positioning accuracy at the receiver, by processing them with a higher bandwidth than required for the narrowband communication signal. A system level study and a Printed Circuit Board (PCB) demonstrator were developed to prove this new concept in various field trials.

This PCB demonstrator allowed to identify the circuit-level trade-offs (e.g. ranging accuracy vs. power consumption) and to derive the integrated circuit specifications for the integration of the ranging transceiver. The re-

mainder of this work focuses on the integration of the RF and analog ranging receiver functions. Chapter 3 describes the design methodologies and measurement results of the high-dynamic range low noise amplifier and mixer. Chapter 4 describes the integration of a highly linear baseband filter and a high-speed 4-bit analog to digital converter. To complete the receiver functionality, chapter 5 described the design of a broadband PCB antenna, and its co-design with the ranging transceiver. This dissertation ends with chapter 6. This chapter concludes with a summary of the main findings of this work and highlights potential areas of related future research.

Bibliography

[1] S. Gezici, Z. Tian, G.B. Giannakis, H. Kobayashi, A.F. Molisch, H.V. Poor, and Z. Sahinoglu. Localization via ultra-wideband radios: a look at positioning aspects for future sensor networks. *IEEE Signal Processing Magazine*, 22(4):70 – 84, Jul. 2005.

2 Ranging System

2.1 Introduction

To enable accurate ranging, different techniques have been proposed, each one of them showing both advantages and disadvantages for use in indoor environments.

2.1.1 RF-based Ranging

Numerous techniques that perform ranging by means of RF signals exist. Each technique measures some characteristic of the RF signal that can be related to the distance the signal has travelled. The choice of characteristic determines the properties of the obtained ranging technique. In this overview, received signal strength indication, time of arrival, angle of arrival and proximity detection will be discussed.

RSSI

Received Signal Strength Indication (RSSI) measures the incoming power exploiting the principle that the power decreases with the distance. In free space, signal power decays proportionally with d^n, with d representing the transmitter-receiver distance and n = 2 the path-loss coefficient. However, in real-world channels, multipath fading causes the RSSI to correlate poorly with distance, resulting in inaccurate distance measurements.

Deviations from the general model will occur on both small (looking like noise on top of the model) and large scale (the model parameters seem different). The small scale fading can be somewhat mitigated through averaging. The large scale fading can be addressed by so-called fingerprinting: the environment is characterized before the actual operation, such that the model parameters can be fitted to optimize the ranging accuracy.

The drawback is that the accuracy degrades if the environment changes, requiring the cumbersome fingerprint procedure to be repeated for every significant deviation. In optimal conditions RSSI can reach about $1\ \mathrm{m}$ accuracy, though only over a small range as shown in figure 2.1, as the error with respect to the average distance estimate increases dramatically with distance.

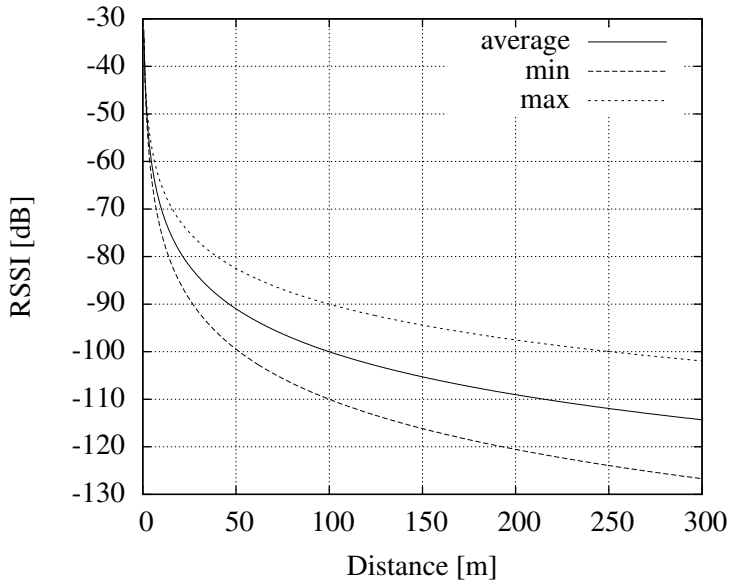


Figure 2.1: Relation between RSSI and distance.

RSSI measurements are relatively inexpensive and simple to implement in hardware, as the RSSI of radio signals can be measured by each receiver during normal data communication without additional bandwidth or energy consumption. Only minimal additional hardware is needed since most communication protocols require that an RSSI measurement is made available upon request by an application. RSSI is often used in combination with WLAN [1] or Zigbee [2]. In summary, RSSI is attractive because of its low

complexity and compatibility with most standards, but it is a very rough measure of distance at its best.

Time of Arrival

Time Of Arrival (TOA) measures the travel time of the radio signal between two nodes. This timing information can be translated into distance information in a number of ways. If two wireless nodes have a synchronized clock, the node receiving the signal can determine the TOA of the incoming signal that is time-stamped by the transmit node. The transmitter-receiver distance can then be derived by multiplying the time-of-flight (i.e., TOA minus time-of-transmission) with the propagation velocity, i.e. the speed of light for RF ranging systems.

When there is no time synchronization between a given node and the reference nodes, but the reference nodes are synchronized, then the Time Difference of Arrival (TDOA) technique can be employed. In this case, the TDOA of two signals travelling between the given node and two reference nodes is estimated, which determines the location of the node on a hyperbole, with foci at the two reference nodes.

In the absence of a common clock between the nodes, the round-trip time between two nodes can be measured to estimate the distance between two nodes, which is also referred to as Two Way Ranging (TWR). This results in two TOA detections and eliminates the need of tight synchronization between the nodes, but still limits the amount of clock drift that can be tolerated between the two nodes. To eliminate the clock drift constraint, double-side two-way ranging can be employed [3] : each node initiates a two-way ranging event, effectively resulting in 4 TOA detections. In such a setup, the clock drift will impact the timing estimations, once positively and once negatively, nilling the impact (assuming the clock remains constant during the packets exchange).

The timing can be extracted from the RF signal in a number of ways. The most direct way to derive the timing information of an RF signal is to detect the leading edge of the packet, such as in traditional radar systems [4]. Despite the low emission power, this principle can be used for Ultra Wide Band (UWB) when keeping the distances limited [5]. To fight noise and interference, the receiver typically correlates with a large portion of the signal to determine the TOA. In the GPS system [6] for instance, the receiver correlates over the $1\ \mathrm{ms}$ long Coarse/Acquisition code which allows to get good accuracy out of a narrowband signal. In other systems such as

Nanotron [7], an inherently wideband signal is used (60 MHz chirp) to get a relatively good accuracy out of a single measurement.

For an ideal single-path channel, it can be shown that the accuracy of a one-shot TOA estimate depends on the signal bandwidth (which defines the time-resolution) and Signal to Noise Ratio (SNR) [8]. Thus, the accuracy of TOA-based ranging can be improved by increasing the SNR or the signal bandwidth. These two parameters allow to make an initial estimate on the performance of different systems: UWB uses a bandwidth of at least 500 MHz and can thus obtain very good accuracy (down to about 15 cm), but due to the low emission levels the coverage is quite poor (<60 m in LOS and <20 m indoors); Nanotron uses a 20 MHz to 60 MHz chirp, resulting in best case 2 m accuracy over a few 100 meters; WLAN uses a 20 MHz bandwidth, yielding an accuracy of 8 m over a few 100 meters. In practice, the quality of TOA measurements depends also on the receivers ability to accurately estimate the arrival time of the Line Of Sight (LOS) signal. This estimation is mainly hindered by multipath propagation that creates the following error sources:

- Early arriving multipath. Many multipath signals arrive shortly after the LOS signal, and their contribution obscures the real time-of-flight information given by the LOS signal. This is the case if the processing bandwidth is too small to discern between the different paths or if the signal used for locking is too long. This is for instance the case for GPS and chirp signals.

- Non-Line Of Sight (NLOS) propagation results in large positive errors in the TOA estimates. Obstacles such as walls and buildings block the LOS path and, as such, the signal arrives at the receiver via reflections on other surfaces. For each individual measurement, it is very hard to distinguish between a LOS and NLOS measurement. The distinction can e.g. be made using statistics on a large amount of measurements: the spread on NLOS measurements is typically larger than on LOS measurements. Another way is to track the distance measurements: when an object moves behind a wall, a sudden jump in measured distance can occur, which is not physically possible considering the limited speed of the object.

Angle of Arrival

Angle Of Arrival (AOA) measurement systems provide the direction to neighboring sensors. The most common method to measure the AOA is to use a sensor array and apply array signal processing techniques to estimate

the AOA by determining the differences in arrival time for a transmitted signal at each element of the array. Therefore, AOA measurements need a large array to realize a sufficient angular resolution and the signal processing should be multipath tolerant. Many systems use AOA to augment basic ranging information, e.g. Ubisense [9].

Proximity detection

A very rough measure of distance is simple proximity detection. If the signal from a known reference source is detected, then the mobile node is within the operational range of that reference point. This operational range can be very short, e.g. in case of Radio Frequency IDentification (RFID) systems [10], resulting in good accuracy, but requiring a huge amount of reference points to get good coverage. Or the range can be very large, e.g. in WLANs, resulting in poor accuracy, but excellent coverage. Several proximity detection mechanisms with different ranges can be combined to make an accuracy/coverage trade-off.

2.1.2 Non-RF-based Ranging

A number of systems try to estimate the distances by detecting or measuring non-RF signals. A variety of techniques are shown to give an overview of their benefits and limitations.

(Ultra)Sound

An alternative carrier is a sound wave. The Cricket system (see figure 2.2) as developed by Massachusetts Institute of Technology (MIT) uses a 40 KHz ultrasound signal. Ultrasound is a pressure wave, just like sound waves, but with a frequency above the range of human hearing.

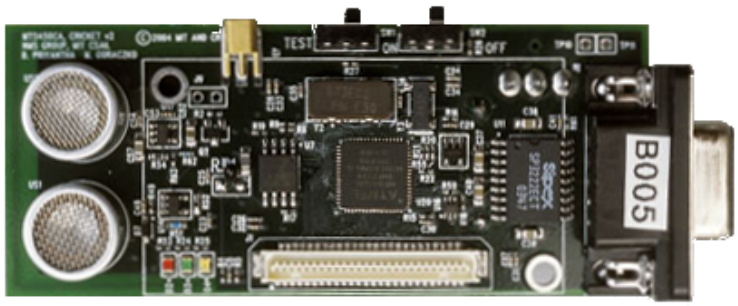


Figure 2.2: Cricket System from MIT.

Because of the significantly lower propagation speed of sound compared to RF signals, it requires simpler processing to obtain good accuracy. Cricket can reach $5\ \mathrm{cm}$ accuracy [11]. On the other hand, there are a few disadvantages associated with the use of ultrasound: ultrasound does not propagate through walls and diffracts even worse than audible sound through doors and windows [11]. Therefore, ultrasound positioning is confined within rooms and thus mostly suited for large open areas. Moreover, the use of speakers make small scale integration harder.

Laser

Laser-based ranging systems often feature very impressive accuracy/range combinations: most systems offer accuracies down to $2\ \mathrm{mm}$ over a range of $500\ \mathrm{m}$ or more, both indoor and outdoor. Therefore, laser is used intensively for distance measurements. As the laser needs to be pointed on the target, this technique is not really suitable for positioning. Moreover, a clear LOS is required, which reduces the usability to outdoor and open indoor environments.

Camera

The position of an object in a camera image can be directly related to the real position in the physical world, yielding immediately the position instead of combining several distance measurements. As a clear LOS is required, camera-based positioning does not handle obstacles well; this can be somewhat mitigated by combining several cameras with different positions and angles in order to completely cover an area.

Infra-red

Infra-red propagates well within a confined area, but not through walls. This makes the technique ideally suited for in-room detection. Infra-red transmitters and receivers are inexpensive, making infra-red positioning systems cheap and well suited for a number of specific applications but hard to implement as a generic system.

2.1.3 Conclusions

Based on the overiew of different ranging techniques, the following conclusions can be drawn. To devise a positioning system that offers a good – one-shot – accuracy indoors, one needs to use:

- RF signals, because these propagate well indoor, compared to other signals such as light, ultrasound and infra-red and present a good path to silicon integration.

- TOA: which allows to get good accuracy if a wideband signal is used. In the presence of strong reflections which is typical for indoor environments there is no strong correlation between the Received Signal Strength (RSS) [12] and the distance. This requires to determine and use sophisticated path loss models in combination with an accurate characterization of the environment.

- Broadband signals: By measuring the propagation delay of narrowband signals such as WLAN packets [13]. The achieved accuracy is only $8\ \mathrm{m}$, which is not sufficient for most indoor applications. If more broadband signals are used such as UWB signals [14], a higher accuracy can be achieved. The broadband nature of the signal comes from the very short span used in the time domain and hence provides improved resolution to separate the line-of-sight propagated signal from the reflected copies. However, UWB signalling has serious disadvantages with respect to narrowband communication in terms of link budget. When also taking into account the high frequency at which UWB communication usually takes place, it is not surprising the operation range of such systems tends to be significantly lower than that of classical narrowband systems. Since the UWB approach offers superior ranging capacities and the narrowband approach offers superior communication properties due to the higher link budget, the two techniques should be united to combine the benefits and get rid of the drawbacks.

2.2 System architecture

To add low cost location awareness to sensor networks, the communication radio should be reused. As concluded in section 2.1.3, to add ranging capabilities to the existing narrowband radio used for communication, the transmitter should be able to transmit a broadband signal. To limit the cost, and to reuse existing transceivers, a fast amplitude modulation technique is proposed. This way the signal will exceed the narrowband communication channel and a broadband signal is formed, which has superior ranging properties. To obtain a spacial resolution of less than $1\ \mathrm{m}$, a steep edge with a rise time of less than $3.3\ \mathrm{ns}$ (the spatial resolution divided by the speed of light) is required. The proposed method and the design requirements are described in this section.

2.2.1 Ranging Transmitter

The RF ranging pulse can be generated from a narrow band WLAN signal by forcing a very steep edge at the beginning of the packet. Two different ways of modifying a standard WLAN transmitter are illustrated in figure 2.3.

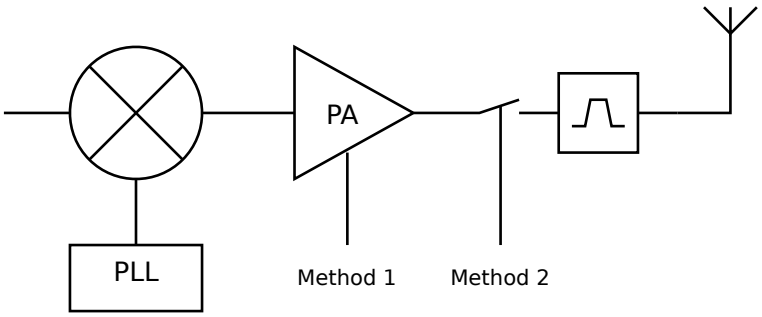


Figure 2.3: Different methods to generate a ranging pulse.

1. Quickly enabling and disabling the Power Amplifier (PA), which varies the generated output power.

2. Gating the generated RF power by using RF switches with a fast control interface. The switch can be placed before or after the PA.

To estimate the effect on the performance, the different pulse generation techniques were experimentally evaluated.

Method 1: Pulse generation using PA activation

One method to generate steep RF pulses, consists of fast enabling and disabling the PA inside the transmitter chain (by disabling its bias current). The benefit of this approach is that it requires absolutely no additional RF hardware, reducing the implementation cost. The drawback is that the interfacing and even the possibility to quickly change the PA bias depend on the properties of the PA, which differ from product to product. Anyhow, to test the feasibility of the approach, a WLAN Front End Module (FEM) was selected that contains a biasing interface that can be used for generating RF pulses with fast rising edge. The block diagram of the Epic Communications FM7704 FEM [15] is presented in fig. 2.4 showing two PAs, one for the 2.45 GHz Industrial, Scientific and Medical (ISM) and Unlicensed National Information Infrastructure (UNII) band respectively.

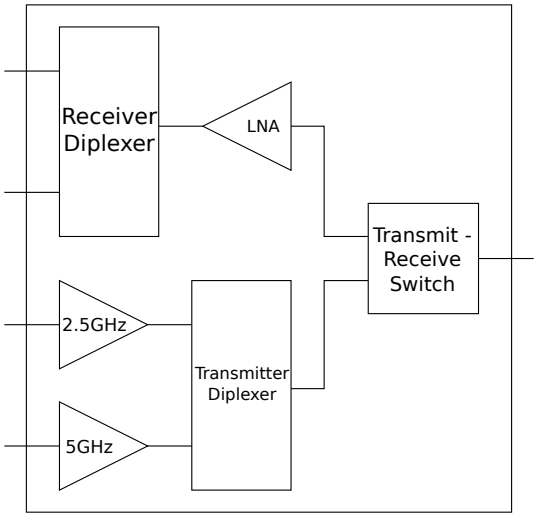


Figure 2.4: Block diagram of the FM7704 WLAN front-end module.

The PA bias interface needs a fixed 2.8 V to operate. To disable the PA this signal was pulled down to 2 V. If the bias is pulled down to as low as 0 V the resulting rise time is lower. The resulting 10 % - 90 % rise time was measured to be 2.81 ns. The resulting isolation was 64 dB.

Method 2: Pulse generation with a RF switch

The ranging transmitter should generate pulses with rise and fall times that exceed the values typically used for the communication channel. The simplest method to enable a narrowband transmitter to generate wideband RF pulses is to add a RF switch in the main transmitter chain that can toggle fast between its on and off state. The requirements for such a switch are:

- low RF insertion loss
- adequate bandwidth that allows the RF signal to pass
- high switching speeds

To test this concept the Hittite Microwave HMC427LP3 GaAs MMIC positive control transfer switch [16] was selected. Its datasheet states that the switch is able to generate pulses with typical rise and fall times of $2\ \mathrm{ns}$, which is definitely better than what is required. Moreover, the switch can change state with simple $5\ \mathrm{V}$ logic interfaces. As the control signals are single ended, a Low Voltage Differential Signaling (LVDS) buffer was required that interfaces from a fast differential LVDS signal and generates a single ended signal with adequately steep rising edges. This Hittite switch can be placed, as explained before, before and after the PA.

The switching was performed on a $2.45\ \mathrm{GHz}$ carrier. The resulting $10\ \%$ - $90\ \%$ rise time of the generated pulse is $3.25\ \mathrm{ns}$ which is sufficient to perform ranging with adequate accuracy. The position of the switch inside the transmitter chain is arbitrary. The two positions, right before and right after the output PA, were tested. The linearity of the switch is adequate for both locations. The switch itself has limited isolation between the on and off state. During the off-state the transmitted signal should be small enough, so that the first rising edge can be detected without problems. The switch before the PA of the FEM had an isolation of $54\ \mathrm{dB}$ and the switch after the PA of the FEM resulted in $45\ \mathrm{dB}$ isolation. This number is certainly adequate to distinguish the first rising edge of the detected RF pulse.

Bandwidth requirements for Ranging

Taking the assumption of a first order system, the rise time of the system can be expressed as:

$$t_{r10\%\rightarrow 90\%} = 0.35/bandwidth \tag{2.1}$$

This results in a minimum bandwidth of the pulse generator of at least $100\ \mathrm{MHz}$ and preferably more to reach $1\ \mathrm{m}$ accuracy. The transmitter should fulfill Federal Communications Commission (FCC) spectral regulations. Normally, the spectrum should be very pure for continuously transmitting equipment, in case the transmission only happens from time to time (e.g. a hundred times per second), as is the case for a ranging transmitter, the average transmitted power is considerably lower and therefore, the spectral congestion will be minimized. This allows to generate a broadband signal which fits in the narrowband spectral mask defined by the FCC regulations. Moreover, the RF pulse generation methods that were discussed before do not offer a very well defined modulation bandwidth. When compared to a WLAN quadrature modulator for example, this bandwidth is very well defined and restricted to the $20\ \mathrm{MHz}$ WLAN channels. For the RF pulse generation it is "best effort". Yet previous remarks showed that a wider bandwidth is not a problem as long as the repetition rate is low and the full signal travels through the RF filter without severe deformation. So in conclusion the transmitter bandwidth is chosen large enough not to compromise the measurement accuracy, but not too large to prevent that part of the RF pulse spectrum is filtered by the WLAN RF filter.

Spectral content

The spectral content of the most simple ranging pulse signal, a gated sine wave, was evaluated experimentally. The power of the ranging signal depends on the repetition rate of the ranging pulse. Considering the maximal packet transmission rate is once every $80\ \mu\mathrm{s}$. The spectrum of the aforementioned pulse generation methods was measured with a spectrum analyser, and with the parameters described in section 17.3.9.2 of the Institute of Electrical and Electronics Engineers (IEEE) 802.11a standard [17]. The pulse width was chosen at $11\ \mathrm{ns}$, which is appreciably higher than the rise and fall times after the receiver filtering so the ranging pulse can be detected at maximum power. The chosen center frequency equals $5.15\ \mathrm{GHz}$, but similar conclusions could be made when modulating a carrier from the ISM band.

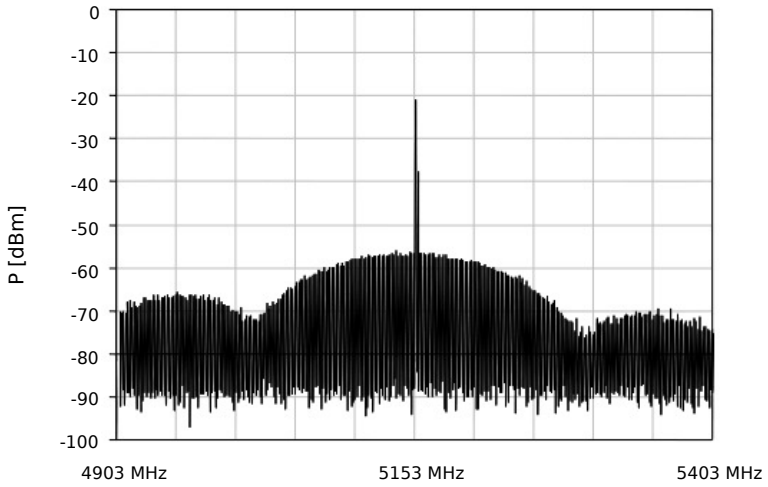


Figure 2.5: Spectrum of a ranging pulse.

Figure 2.5 shows the measured spectrum of the signal with $10\ \mathrm{dBm}$ peak output power. The plot is worth a closer look: the RF carrier clearly stands out. When transmitting an output signal of $17\ \mathrm{dBm}$ with a duty cycle of $11\ \mathrm{ns}$ each $80\ \mu\mathrm{s}$, the resulting output power is $17 + 10 \cdot \log 11/80000 = -22$ dBm. The repetition rate can be measured via the spacing of the notches of the resulting sync spectrum, $80\ \mu\mathrm{s}$ corresponds with $6\ \mathrm{MHz}$. The isolation is estimated to be close to $30\ \mathrm{dB}$, a typical value for GaAs switches.

2.2.2 Ranging Receiver

The ranging transmitter is a narrowband system with a minimum of modifications to realize the broadband ranging pulse. On the receiver side the broadband modulated RF pulses need to be detected. Broadband detection is needed to achieve adequate accuracy for the ranging event. Different solutions exists:

- threshold detection with a RF power detector,
- downconversion with a baseband threshold detector,
- downconversion with a fast Analog to Digital Converter (ADC) and threshold detection in the digital domain.

RF power detector

A RF power detector extracts the RF signal after the antenna or after the Low Noise Amplifier (LNA) in case its bandwidth is adequate, and performs threshold detection on this signal. This approach is really simple, and requires very little hardware.

Therefore this approach was selected at first to test the feasibility of pulse transmission and reception after propagation through a warehouse-like environment with very little interfering signals. The RF detector was implemented by using a fast oscilloscope which was able to digitize the RF signal in real time. The threshold detection was performed offline by means of software processing.

On the downside, the feasiblity is questionable because:

- Building an RF detector with more than $100\ \mathrm{MHz}$ bandwidth which works up to $2.5\ \mathrm{GHz}$ is very hard, since it would require a selective filter (very high Q-factor) to attenuate interferers.
- This solution suffers from limited sensitivity and interference rejection. The only bandwidth limitation in the system is the RF band selection filter (ISM/UNII) which is not adequate. Out-of-band blockers can distort the measurement tremendously due to the high detector bandwidth.

Downconversion with a baseband threshold detector

If the RF signal is first downconverted, adequate filtering can be implemented before the threshold detection. Moreover, it is much more feasible to design a fast baseband threshold detector rather than an RF threshold detector. The downside of this approach is that an additional wideband demodulator is required after which the baseband detector can perform the ranging. Moreover a quadrature downconversion is required which doubles the amount of detection electronics.

Downconversion with a fast ADC

A threshold detector is in fact nothing more than a 1 bit ADC. To have more accuracy, an ADC with more bits can be used. This is only possible after downconversion because ADCs which sample at RF are very expensive and consume a lot of power. A bonus to having more bits is that other offline processing techniques can be used in order to improve the signal to noise ratio. Specifically correlation techniques could prove very useful to reach

higher distances with a similar bandwidth. The downside of this approach is that the ADC adds quite some additional hardware to the system and increases the cost of the transceiver.

2.2.3 Bandwidth requirements

Setting forward an accuracy of 1 meter in $95\ \%$ of the cases and given the speed of light in air, the uncertainty on the arrival of the pulse in a one-dimensional positioning system is limited to $3.33\ \mathrm{ns}$. In the three dimensional case, three of four delay measurements should be combined to achieve X, Y and Z coordinates. This triangulation process is a research topic covered by the VUB and Essensium in a closely related IWT project.

In case of threshold detection, the threshold will be fixed $10\ \mathrm{dB}$ above the noise floor not to trigger too many false alerts. On the other hand, the power of the received pulses varies as the channel changes due to environment changes and distance variations. Therefore the trigger moment in the rising edge of the pulse will be different from case to case.

It is safe to assume that this jitter – and hence the measurement accuracy – will be smaller than the $10 - 90\ \%$ rise time. In case a very strong pulse arrives the ranging pulse will cross the threshold already at its $10\ \%$ level, while a pulse at the edge of sensitivity will cross the threshold at its $90\ \%$ level.

$$t_r = \frac{0.35}{bandwidth} \tag{2.2}$$

By means of equation 2.2, which expresses the $10 - 90\ \%$ rise time of a first order system, the acceptable inaccuracy of $3.33\ \mathrm{ns}$ on the delay estimation can now be expressed in terms of a minimum receiver bandwidth of $100\ \mathrm{MHz}$. On the other hand, a bandwidth limitation is mandatory to obtain a good receiver SNR, since in case the received pulse power is very small, noise will contribute to the estimation errors. In practice, the receiver bandwidth will be of higher order, since multiple poles of different building blocks will be present. In order to maintain sufficient rise time, the minimum required system bandwidth needs to be increased.

2.2.4 Frequency selection and path loss

An important specification of the system consists of the description of the frequency bands to be used. Different unlicensed frequency ranges exist among which the ones used for WLAN, UWB, Zigbee, ... To make a well-founded decision on the frequency range, path loss and signal to noise ratio

are compared. Frequency bands lower than the 2.4 GHz ISM band don't offer sufficient bandwidth which would result in interference issues.

ADS Ptolemy simulations were performed to asses the influence of different channel models, both urban and suburban, which take large scaling effects (reflections via the ground, buildings, and other obstacles) into account and a simpler path loss based channel with a loss of $1/r^{3.3}$, thus independent of frequency. Both the urban and suburban models in the simulator are based on the classical Hata model [18].

Pathloss model	Pathloss (dB)	Received Power (dBm)	SNR (dB)
urban	105	-89	-4.0
suburban	89.3	-73.3	11.5
$1/r^{3.3}$	96	-80	4.9

Table 2.1: Simulation results for a carrier frequency of 5.25 GHz.

Pathloss model	Pathloss (dB)	Received Power (dBm)	SNR (dB)
urban	96.5	-80.5	4.5
suburban	83.6	-67.6	17.4
$1/r^{3.3}$	96	-80	4.9

Table 2.2: Simulation results for a carrier frequency of 2.45 GHz.

The simulation results for a 16 dBm transmitter at 5.25 GHz and a receiver with bandwidth of 200 MHz and a noise figure of 6 dB, modeled as additive white noise at the receiver input with spectral density of -168 dBm/Hz resulting in a total received noise of -85 dBm at 50 m are summerized in table 2.1. The results for a 2.45 GHz transmitter-receiver combination are shown in table 2.2.

To obtain a high ranging accuracy of up to 50 m, the 2.45 GHz frequency band is the obvious choice, since it offers the highest SNR in all cases.

2.2.5 Signal to noise ratio versus bandwidth

To investigate the effect of the receiver bandwidth on the SNR of the detected signal, the bandwidth is swept from $20\ \mathrm{MHz}$ to $600\ \mathrm{MHz}$ in a system level Advanced Design System (ADS) model, and the corresponding SNRs are plotted in figure 2.6. It reveals that the SNR of the received pulse depends on the receiver bandwidth. Indeed reducing the receiver bandwidth reduces the noise bandwidth and results in a lower effective integrated noise. Of course caution must be taken that the bandwidth reduction does not compromise the spatial accuracy of the ranging estimation process.

The limited rise time also decreases the accuracy of the detected delay in case the received pulse power is varied from the maximum to the minimum. In case the bandwidth is equal to $125\ \mathrm{MHz}$, the rise time equals $2.8\ \mathrm{ns}$, which corresponds to a maximum distance error under $1\ \mathrm{m}$. Therefore a $125\ \mathrm{MHz}$ bandwidth is certainly adequate, but results in a little worse SNR. Note that the definition of this bandwidth is done in base band. A $125\ \mathrm{MHz}$ bandwidth would result in a $\pm 125\ \mathrm{MHz}$ or $250\ \mathrm{MHz}$ pass band centered on the RF carrier of $2.45\ \mathrm{GHz}$ or $5.25\ \mathrm{GHz}$.

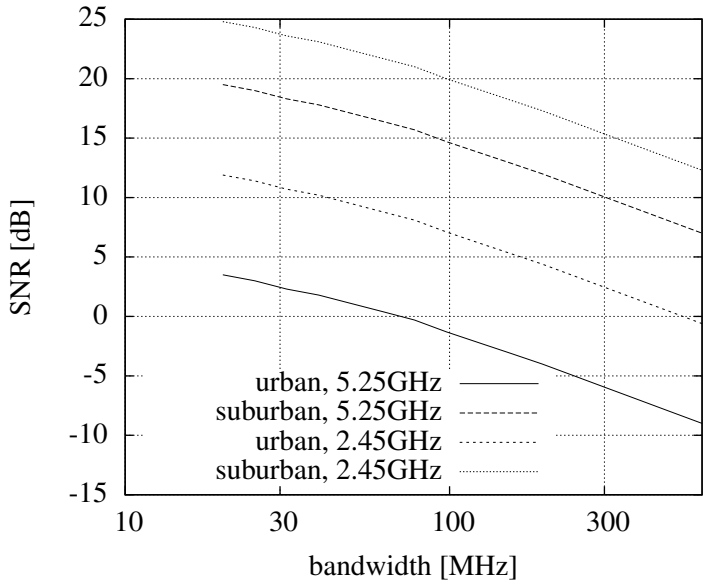


Figure 2.6: Variation of SNR with respect to receiver bandwidth.

2.2.6 Signal to noise ratio versus distance

To analyse the effect of the ranging distance on the SNR at the receiver side, the distance is swept from $10\ \mathrm{m}$ to $50\ \mathrm{m}$ and the corresponding SNRs are plotted in figure 2.7. All four cases, as expected, clearly show that the SNR at receiver side is a logarithmic function of the ranging distance.

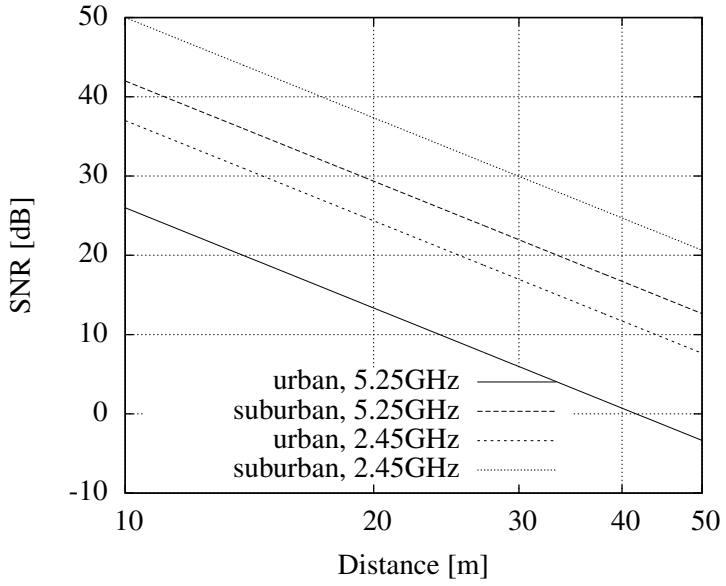


Figure 2.7: Variation of SNR with respect to the distance between RX and TX.

2.3 Proof-of-concept

To prove the concept of indoor ranging with sub-meter accuracy in the $2.45\ \mathrm{GHz}$ ISM band, a ranging transceiver has been developed, by making use of off-the-shelf components. The architecture of the prototype is shown in figure 2.8. A picture of the resulting PCB design is shown in figure 2.9. It is an 8 layer board made of standard Flame Retardant 4 (FR4) material, containing a total of 593 components including passives. The board includes all functions needed for ranging: the RF front-end, baseband ADC, filtering, a high-speed Field-Programmable Gate Array (FPGA), etc. While designing the board, special care was taken to ensure a proper power supply distribution, maximize signal integrity and reduce crosstalk, etc.

The operation of the board can be configured in various ways:

- with Dual In-line Package (DIP) switches,
- via push buttons,
- and via standard interfaces such as: serial port, Serial Peripheral Interface bus (SPI), Low Pin Count interface (LPC) and General Purpose Input Output (GPIO).

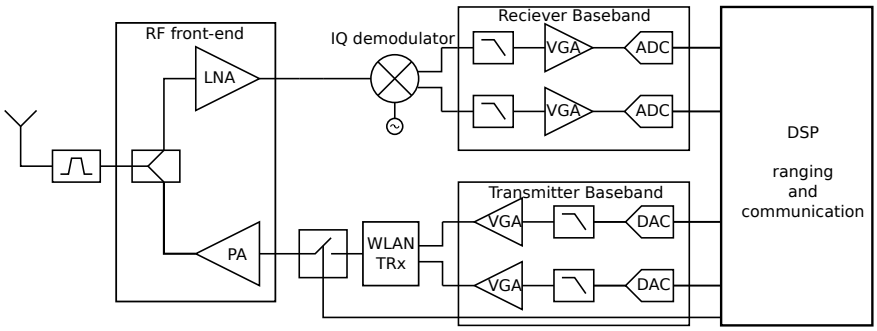


Figure 2.8: Functional block diagram of the ranging transceiver.

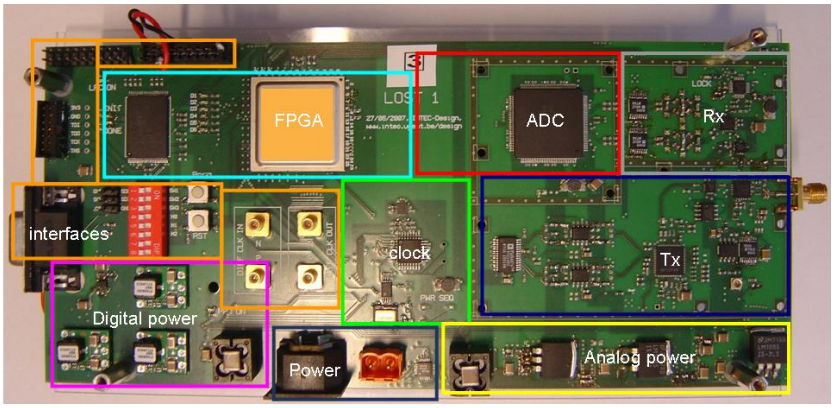


Figure 2.9: Ranging transceiver PCB.

An aluminum cover, shown in figure 2.10, was milled to shield the RF part. Measurements confirm a 0.5 dB improvement of the Receiver (RX)

noise figure. Since the performance is sufficient without shielding, most experiments were performed without.

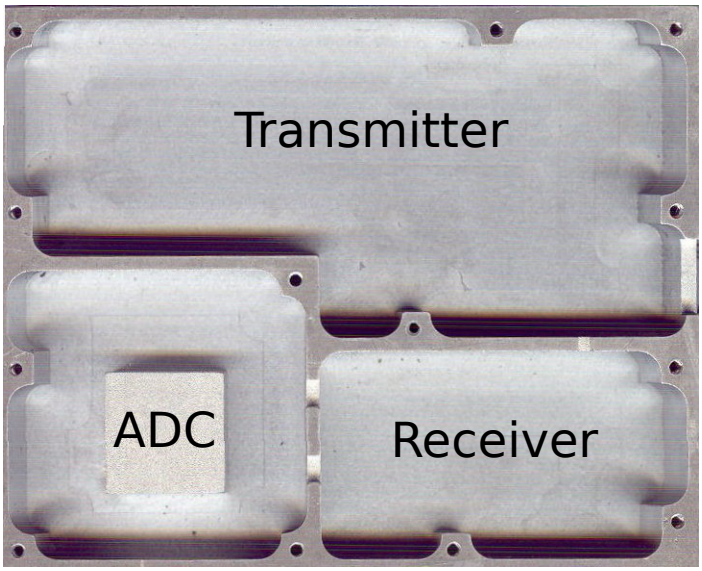


Figure 2.10: Metal enclosure to shield the sensitive PCB parts.

2.3.1 Ranging Transmitter

The transmitter design offers 3 possibilities to generate the ranging pulse: by switching the bias of the PA or by using an RF switch before or after the PA (see figure 2.3).

- The fast enabling of the PA bias provides the shortest rise time but relies on the specific (GaAs) PA component used. Implementation in Complementary Metal Oxide Semiconductor (CMOS) technology may not be feasible.
- From a ranging point of view, both locations of the RF switch provide sufficient isolation and rise time. As this is a more general solution, this will be preferred. Both locations of the RF switch result in a similar rise time. Since the signals in front of the PA are much smaller, this is the most obvious location to place the switch. This will result in higher isolation and lower distortion.

To demonstrate that communication signals can indeed accommodate the proposed ranging technique, a modified WLAN packet is used, contain-

ing only a short preamble to be used for Automatic Gain Control (AGC), timing synchronization, frequency offset estimation, ... The first symbol of the short preamble will be switched to generate the fast edge. These ranging packets are generated using a Digital to Analog Converter (DAC) and upconverted to 2.45 GHz by a WLAN transceiver chip. In between the WLAN transceiver and the PA, a high speed switch is used to generate a fast rising edge at the beginning of the ranging packet. The standard short preamble waveform duration is 8 μs (10 "short training sequences", 800 ns long, shown in figure 2.11) and contains only 12 (out of 52) carriers. Due to the Orthogonal Frequency-Division Multiplexing (OFDM) multicarrier modulation, the burst envelope is not constant, but has a certain peak-to-average ratio.

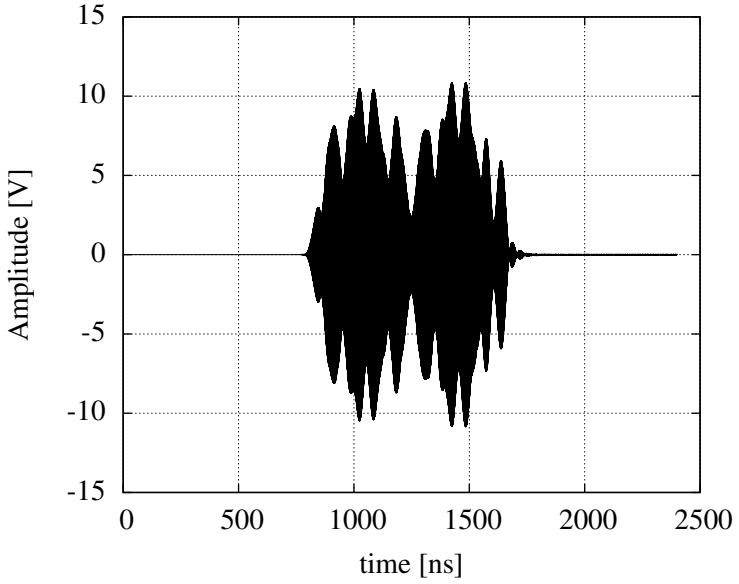


Figure 2.11: WLAN short preamble.

2.3.2 Ranging Receiver

The ranging receiver has a zero-Intermediate Frequency (IF) architecture, as most wireless transceivers nowadays. The baseband system contains a variable gain amplifier which can be used to compress the dynamic range of the received signals. If required the gain setting can be fixed for a given ranging distance, while saturating the amplifier annex ADC at short dis-

tances. The required gain range is approximately 40 dB, and the RF bandwidth is up to 200 MHz (2 times the 100 MHz baseband bandwidth).

To limit the receiver's bandwidth a differential 5th order Bessel filter (for minimal pulse distortion) with following specifications is implemented: baseband bandwidth of 100 MHz and improved coupling between in- and output (to reduce the attenuation at high frequencies). Care was taken to match the impedance of the In phase – Quadrature (IQ) demodulator which is $65\ \Omega$ in parallel with 5 pF to the input impedance of the AD8369 (Variable Gain Amplifier (VGA)) which is $200\ \Omega$.

According to Nyquist, the ADC will require a sampling speed of at least 400 Msps, and preferably not much higher as this might cause problems with the high-speed interfacing of the data lines to the FPGA. The National Semiconductor ADC08D500 8-bit ADC is able to sample at speeds up to 500 Msps, and contains two ADCs per package. The ADC output contains demultiplexers, yielding 32 LVDS signals at 250 Msps.

The analysis of the Noise Figure (NF) of the receive path is shown in table 2.3. A legend with the stage numbers can be found in table 2.4. The NF of a cascade of building blocks depends on both the individual noise figures as well as their respective gains. This analysis shows that the RX path requires a second LNA in front of the LT5575 IQ demodulator to achieve a low noise figure (4.65 dB). The latter is dominated by the first LNA (3.0 dB), however, increased by the loss of the band pass filter (1.5 dB) giving 4.5 dB. Without the second LNA, the NF of the IQ demodulator will augment the total receiver NF.

The AD8369 VGA can vary the gain over 40 dB and the HMC605LP3 LNA offers a bypass mode to decrease the gain by 20 dB. This high dynamic range is adequate for ranging up to 500 m.

stage nr		1	2	3	4	5	6	7
Gain (dB)	min	-1.5	10.0	-1.9	2.0	-0.5	-10.0	-3.0
	max	-1.5	10.0	20.0	2.0	-0.5	35.0	-3.0
Cascade	min	-1.5	8.5	6.6	8.6	8.1	-1.9	-4.9
Gain (dB)	max	-1.5	8.5	28.5	30.5	30.0	65.0	62.0
NF (dB)	min	1.5	3.0	1.1	15.7	0.5	49.2	6.0
	max	1.5	3.0	1.1	15.7	0.5	7.2	6.0
Cascade	min	1.50	4.50	4.56	10.32	10.33	41.10	41.11
NF (dB)	max	1.50	4.50	4.56	4.64	4.64	4.65	4.65

Table 2.3: Noise figure analysis of the receive path.

stage 1	bandpass filter
stage 2	LNA of the RF Front-end module
stage 3	2nd LNA
stage 4	Demodulator
stage 5	Low pass filter
stage 6	VGA
stage 7	resistor divider (due to the input impedance of the ADC)

Table 2.4: Description of the receiver stages.

2.3.3 Clock synthesis

The RF modulator and demodulator and especially the fast ADC require a good and dedicated high speed clock. The ADC's clock could be generated directly by a $450\ \mathrm{MHz}$ Surface Acoustic Wave (SAW) oscillator and could be divided down for the other components. However, this solution is expensive and not flexible. An alternative is to use a clock synthesis IC that converts a low-frequency crystal oscillator clock up to the value required for the ADC. The resulting clock jitter is higher but still adequate for our application ($< 10\ \mathrm{ps}$). An example is the NBC12439 family from On Semi, which allows clock synthesis between $50\ \mathrm{MHz}$ and $800\ \mathrm{MHz}$. Other clock synthesizers use external Voltage Controlled Oscillators (VCOs) with lower phase noise, which result in lower jitter on the synthesized clock, but provide a lower frequency flexibility and a higher cost.

The ADCs and the FPGA require a coherent differential clock. There are, however, other components which require other clock frequencies. The RF synthesizer can accept clocks from 10 up to $250\ \mathrm{MHz}$. The WLAN transmitter requires a clock between 20 and $44\ \mathrm{MHz}$. The NBC12439 requires a clock between 10 and $20\ \mathrm{MHz}$. The logic conclusion is to select $20\ \mathrm{MHz}$ as reference oscillator. The $20\ \mathrm{MHz}$ CMOS clock will be distributed over the different components by a 1:4 clock buffer, after which it is applied to the NBC12439 (which generates a $500\ \mathrm{MHz}$ clock for the ADC), the RF synthesizer, the FPGA and the WLAN transmitter. The multiplied $500\ \mathrm{MHz}$ clock which drives the ADCs will be split and routed to the ADC and FPGA. This will require an additional differential clock splitter. All clock generation/distribution components are in the digital supply domain, except the Phase Locked Loop (PLL) RF synthesizer, which uses the $3.3\ \mathrm{V}$ analog supply.

2.3.4 Power supplies

A single Direct Current (DC) voltage (7 to 9 V) is supplied to the board. This voltage is used to derive the analog and digital supplies. The analog and digital domain are isolated by a filter to reduce interference problems. A single ground plane is used for all parts to keep the ground impedance as low as possible. To minimize crosstalk, the return paths are minimized by the well considered placement of sensitive analog and digital blocks. The analog supply voltages (1.9 V, 3.3 V, 5 V) are derived using linear regulators, whereas the digital supply voltages (1.2 V, 1.8 V, 2.5 V, 3.3 V) are derived using switching regulators. Switching regulators offer a much higher efficiency, but generate more noise, that could impact the sensitivity of the analog front-end.

Several supply voltages are needed for the different components. These supplies are powered on in a well defined order, as required by the ADC. At power up, the ADC supply voltage starts automatically, this triggers the enabling of the analog 5 V, followed by the analog 3.3 V, the digital 1.2 V (FPGA core supply voltage), and finally all other digital supply voltages). This sequence is controlled by a quad voltage sequencer/monitor from Maxim with a capacitor-based adjustable timing. For safety reasons, this component shuts down the system when one of the supplies drops below a specified value.

Special care was required for the digital supplies to prevent false detection of supply problems, as during programming of the FPGA high current peaks occur, resulting in large drops on the supply voltage.

A maximum current of 0.645 A at 3.3 V, 0.324 A at 5 V and 0.737 A at 1.9 V is required. To provide sufficient margin, two 3.3 V regulators are required for the analog part and the digital/clocking part. The fast ADC will have a dedicated regulator to reduce mutual coupling through the power supply.

2.3.5 Ranging FPGA

All digital processing is performed on a FPGA. This FPGA generates the ranging and communication signal, controls the ranging switch and processes the received signal on which it performs threshold and edge detection. Next to the ranging related tasks, the FPGA accommodates a processor used for control tasks and programming the different analog chips.

The 500 MHz 8-bit ADC demultiplexes the digital words so in total (I and Q) 32 bit streams, clocked at 250 MHz have to be transmitted to the FPGA.

To handle these high throughputs an FPGA from the Virtex 4 family was chosen. Flash memory is used to store the bit file, so that the system boots automatically at power up.
The FPGA configuration is developed by Essensium.

2.4 Measurements

By making use of the PCB demonstrator, different aspects of the ranging system are evaluated. The measurement campaign started with the verification of the RF specifications crucial to the ranging performance such as the fast switching, output power, receiver gain and noise figure. After these fundamental specifications were verified, the ranging functionality could be tested and quantitative results such as maximum range and accuracy could be obtained.

2.4.1 Transmitter

The Transmitter (TX) measurements were performed with a TX level of $17\ \mathrm{dBm}$. A transmitted ranging WLAN packet is shown in figure 2.12, and a detail of the start of the packet is shown in figure 2.13 (cf. figure 2.11) and figure 2.14, clearly showing a $2.5\ \mathrm{ns}$ rise time. This ranging packet is a modified short preamble, with longer symbol lengths ($1\ \mu\mathrm{s}$ instead of $0.8\ \mu\mathrm{s}$, giving a total length of $10\ \mu\mathrm{s}$). The measured total current consumption of the ranging transceiver board is $1.485\ \mathrm{A}$ (at $7\ \mathrm{V}$, so $10.4\ \mathrm{W}$) in TX mode.

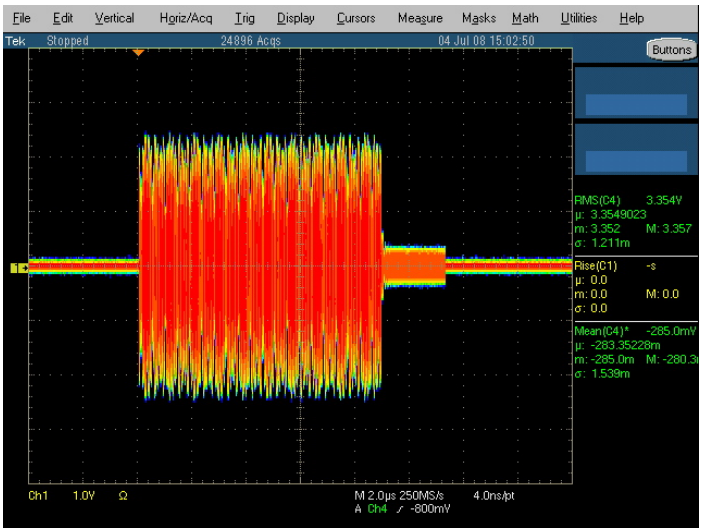


Figure 2.12: A measured ranging WLAN packet (timescale 2 μs/div).

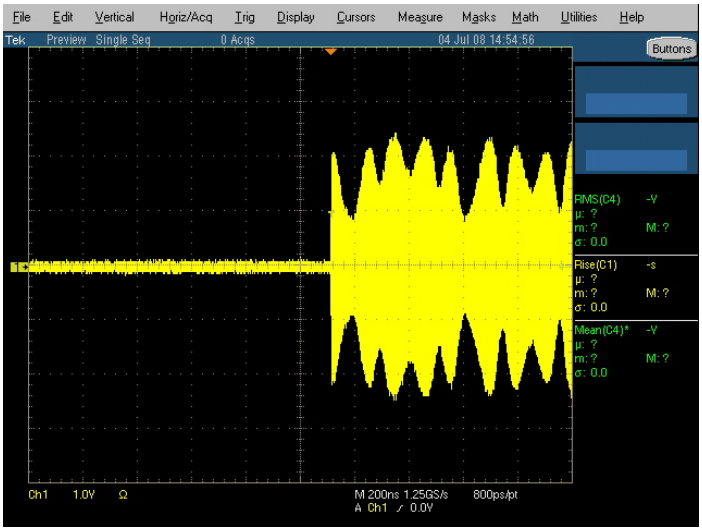


Figure 2.13: A measured ranging WLAN packet (timescale 200 ns/div).

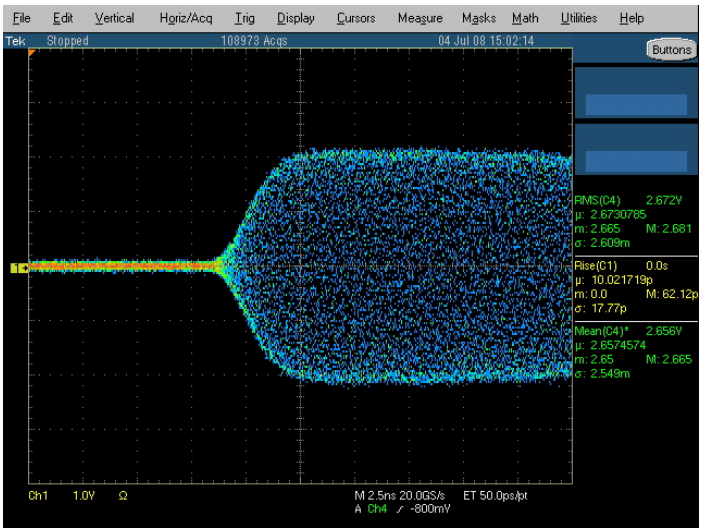


Figure 2.14: A measured ranging WLAN packet (timescale 2.5 ns/div).

The corresponding spectrum is shown in figure 2.15. This measurement shows that the transmitted signal (1000 WLAN ranging packets per second) complies with the 802.11g spectral mask. The spectrum shows the 12 carriers used in the WLAN preamble together with a Local Oscillator (LO) feedthrough component.

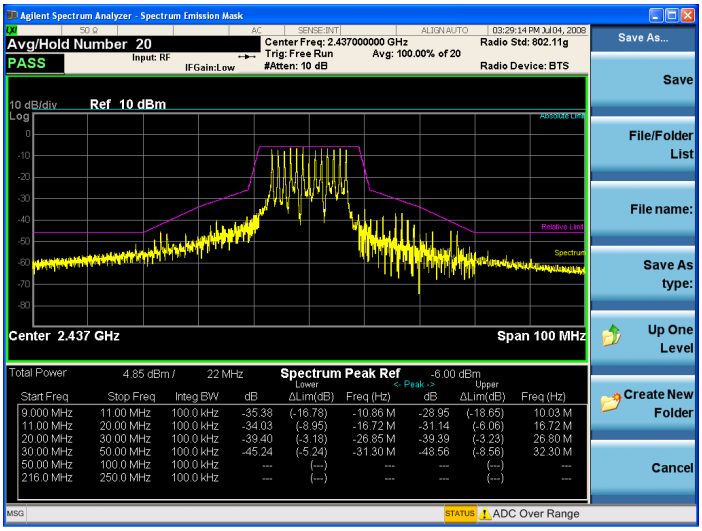


Figure 2.15: Spectrum ranging WLAN packet.

2.4.2 Receiver

The measured frequency behavior of the receiver is shown in figure 2.16. Due to the frequency conversion in the mixer, these Alternating Current (AC) characteristics were measured by sweeping the RF frequency, for a fixed LO frequency at 2.4 GHz. The low pass filters in the baseband section were designed for 125 MHz. The measured I bandwidth is 111 MHz, the Q bandwidth is 106 MHz. The in-phase and quadrature bandwidth are slightly lower than 125 MHz due to the bandwidth limitation of the mixer, however, providing more than 200 MHz bandwidth at RF, more than needed to allow sufficiently short rise times.

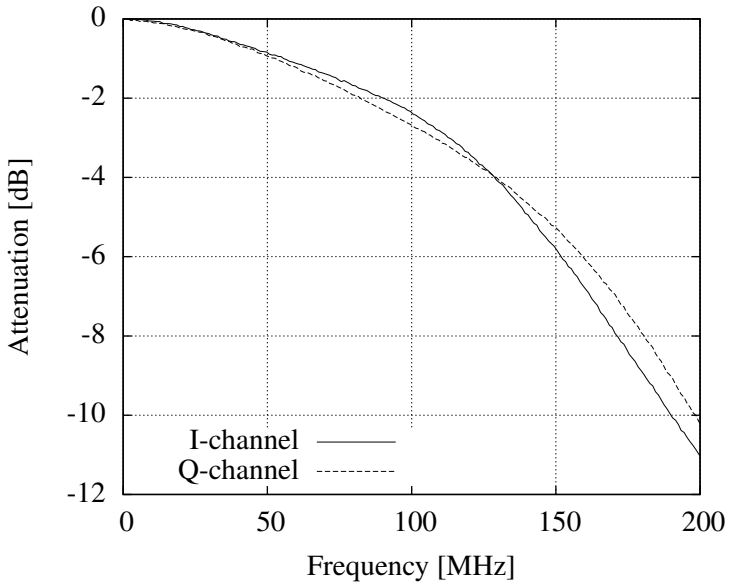


Figure 2.16: Receiver bandwidth measurement.

The measured gain and noise figure of the receiver are compared to the theoretical value in table 2.5. The measured gain is 4 to 9 dB lower than calculated due to mismatch and losses. However, this gain range is more than wide enough.

		I channel	Q channel	Estimated
Gain (dB)	max	53.1	53.1	62
	min	-8.3	-8.1	-4.9
NF (dB)		5.5	5.6	4.7

Table 2.5: Comparison gain and noise figure measurements.

The measured NF is very close (within 1 dB) to the 4.7 dB estimated. This shows that the degradation due to the digital circuitry, digital switching regulators, common ground plane, crosstalk, mismatch, etc. is low and that high-frequency design and layout techniques were correctly applied. The measured input-referred 1 dB compression point is -21.5 dBm, determined by the front-end module.

2.4.3 Ranging Functionality

To evaluate the complete ranging system, the PCB demonstrator is used to perform ranging measurements using a two-way ranging method. The distance was incremented in steps of $2\ \mathrm{cm}$ and at every point, a thousand distance measurements were performed. The measurement results are shown in figure 2.17. This plot shows that the measurements are insensitive to noise since all measurements (without considering averaging) are within a $\pm\ 0.5\ \mathrm{m}$ range, limited by the ADC's sampling frequency, determining the spacial resolution.

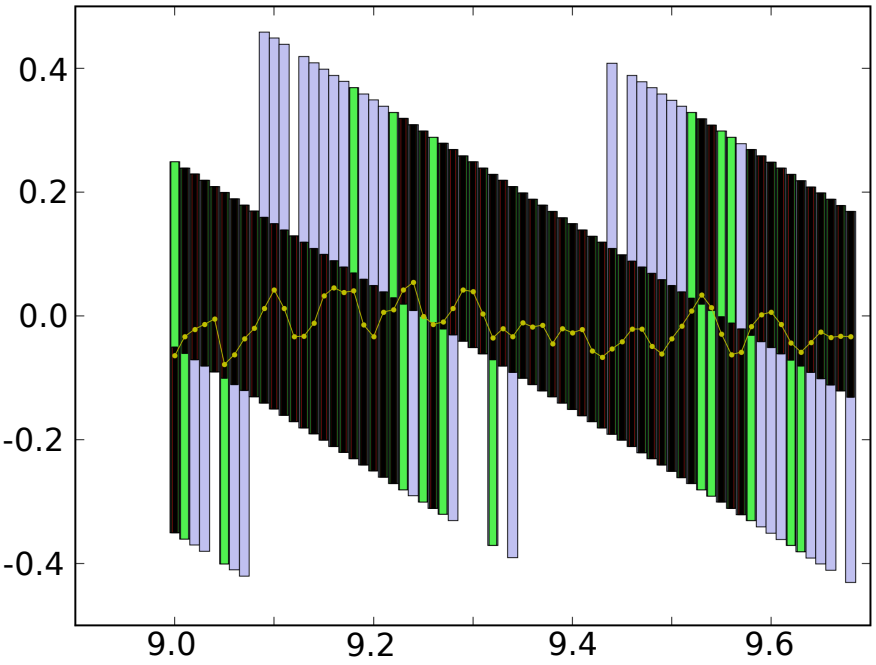


Figure 2.17: Percentiles versus distance (yellow: average, black: $68\ \%$ percentiles, green: $95\ \%$ percentiles, blue: $100\ \%$ percentiles.

After averaging, the measurement accuracy is $\pm 12\ \mathrm{cm}$. A possible cause for this effect is the carrier waveform ($2.4\ \mathrm{GHz}$), which was not modelled: the start of an edge can only be detected on a peak of the carrier waveform. Since the ADC clock, the clock generating the switching signal and the carrier are all generated from a same local crystal, the relative phase deviation is much smaller compared to the phase variation of the clocks on different boards, the latter ensures unbiased measurements due to two-way ranging.

The periodicity in the average error corresponds to the wavelength of the carrier.

The same measurement procedure was repeated over a distance of $300\ \mathrm{m}$ with steps of $25\ \mathrm{m}$. The result is shown in figure 2.18. It can be seen that a $1\ \mathrm{m}$ accuracy is obtained over the complete range.

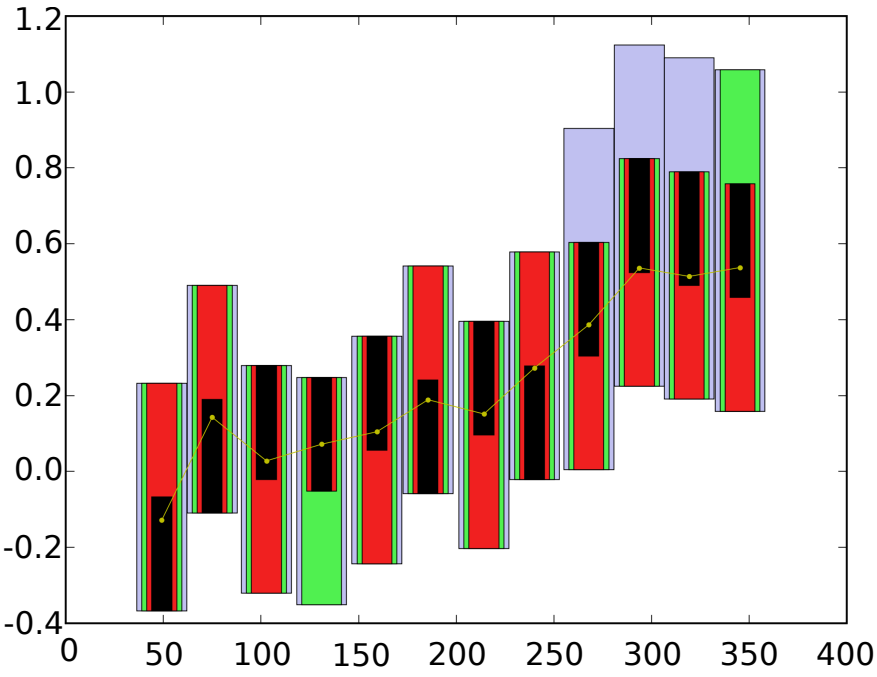


Figure 2.18: Percentiles versus distance (yellow: average, black: $68\ \%$ percentiles, green: $95\ \%$ percentiles, blue: $100\ \%$ percentiles.

The measurements were repeated with a reduced ADC resolution, showing that accurate ranging was possible with a resolution of only 4 bit. This finding severly reduces the demands on further integration steps.

2.5 Conclusion

This chapter introduced the basics and trade-offs of various ranging systems. In this work, together with Essensium, a new concept was evaluated that combines the advantages of both narrowband (long reach) and broadband systems (high accuracy, robust against reflections). The feasibility of

this approach was evaluated in practice through the design of a dedicated ranging transceiver using commercial components. A ranging transceiver incorporating a ranging switch was realized, allowing to generate pulses with a rise time of less than $3\ \mathrm{ns}$ and to perform accurate ranging up to $300\ \mathrm{m}$ with sub-meter accuracy.

This proof of concept resulted in several publications: [19–23]. Currently, this ranging system is deployed in the Antwerp Harbour and on Brussels Airport [24].

The cost and power consumption of this ranging technique can be further reduced by integrating the system into a System on Chip (SoC). The integration of the analog receiver front-end is described in the subsequent chapters. Chapter 3 focusses on the RF part: the integration of the low noise amplifier and the frequency conversion which will produce a base-band signal. Chapter 4 describes the filter used to suppress the mixer spurs and aliasing frequencies to conclude with the description of the ADC used to digitize the signal. Chapter 5 proposes a low cost solution to integrate an antenna, completing the integration of the reception system. The transmitter is designed by my colleague Zhisheng Li and will be discussed in detail in his PhD dissertation.

References

[1] U. Grossmann, M. Schauch, and S. Hakobyan. RSSI based WLAN Indoor Positioning with Personal Digital Assistants. In *4th IEEE Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications*, pages 653 –656, Sept. 2007.

[2] J. Blumenthal, R. Grossmann, F. Golatowski, and D. Timmermann. Localization in Zigbee-based Sensor Networks. In *IEEE International Symposium on Intelligent Signal Processing*, pages 1–6, Oct. 2007.

[3] S. Ko, J. Takayama, and S. Ohyama. A novel RF symmetric double sided two way range finder based on Vernier effect. In *International Conference on Control, Automation and Systems*, pages 1802 –1807, Oct. 2008.

[4] Wikipedia – Radar. http://en.wikipedia.org/wiki/Radar.

[5] I.D. O'Donnell and R.W. Brodersen. An ultra-wideband transceiver architecture for low power, low rate, wireless systems. *IEEE Transactions on Vehicular Technology*, 54(5):1623 – 1631, Sept. 2005.

[6] Wikipedia – GPS. http://en.wikipedia.org/wiki/GPS.

[7] nanoLOC TRX. http://www.nanotron.com/EN/pdf/Factsheet_nanoLOC-NA5TR1.pdf.

[8] G. Shen, R. Zetik, h. Yan, O. Hirsch, and R.S. Thoma. Time of arrival estimation for range-based localization in UWB sensor networks. In *IEEE International Conference on Ultra-Wideband*, volume 2, pages 1 –4, Sept. 2010.

[9] Ubisense Real-time Location System. http://www.ubisense.net/en/rtls-solutions.

[10] Wikipedia – RFID. http://en.wikipedia.org/wiki/RFID.

[11] N. B. Priyantha, A. Chakraborty, and H. Balakrishnan. The Cricket Location-Support System. In *6th ACM International Conference on Mobile Computing and Networking*, pages 32–43, Aug. 2000.

[12] K. Kaemarungsi. Distribution of WLAN received signal strength indication for indoor location determination. In *2006 1st International Symposium on Wireless Pervasive Computing*, page 6. IEEE, 2006.

[13] A. Günther and C. Hoene. Measuring round trip times to determine the distance between WLAN nodes. *NETWORKING 2005*, pages 768–779, 2005.

[14] S. Gezici, Z. Tian, G.B. Giannakis, H. Kobayashi, A.F. Molisch, H.V. Poor, and Z. Sahinoglu. Localization via ultra-wideband radios: a look at positioning aspects for future sensor networks. *IEEE Signal Processing Magazine*, 22(4):70 – 84, Jul. 2005.

[15] FM7704 dual-band 802.11 a/b/g RF front-end module. www.asec.com.tw/upfiles/mark01162519534.pdf.

[16] HMC427LP3, GaAs MMIC positive control transfer switch. http://www.hittite.com/content/documents/data_sheet/hmc427lp3.pdf.

[17] *IEEE Standard 802.11a: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: High-speed Physical Layer in the 5 GHz Band.* IEEE, New York, NY, USA, 1999.

[18] M. Hata. Empirical formula for propagation loss in land mobile radio services. *IEEE Transactions on Vehicular Technology*, 29(3):317 – 325, aug 1980.

[19] X. Yin, J. Bauwelinck, G. Torfs, P. Demuytere, J. Vandewege, H. Tubbax, J. Wouters, P. Debacker, J. Olbrechts, P. Spiessens, F. Stubbe, and J. Danneels. Embedded ranging system in ISM band. *Electronics Letters*, 44(17):1043–1044, AUG 14 2008.

[20] H. Tubbax, J. Wouters, J. Olbrechts, P. Debacker, P. Spiessens, F. Stubbe, J. Danneels, J. Bauwelinck, X. Yin, G. Torfs, and J. Vandewege. A Novel Ranging Technique for 2.4GHz ISM Band. In *The IASTED International Conference on Sensor Networks*, Sept.-Oct. 2008.

[21] H. Tubbax, J. Wouters, J. Olbrechts, P. Debacker, P. Spiessens, F. Stubbe, J. Danneels, J. Bauwelinck, Xin Yin, G. Torfs, and J. Vandewege. A novel positioning technique for 2.4GHz ISM band. In *IEEE Radio and Wireless Symposium*, pages 667–70, 2009.

[22] G. Torfs, X. Yin, Z. Li, J. Bauwelinck, and J. Vandewege. Embedded indoor ranging system with decimeter accuracy in the 2.4 GHz ISM band . In *9e UGent-FirW Doctoraatssymposium*, pages 208–209, 2008.

[23] New ISM-band ranging transceiver allows positioning in decimeter range. In *IMEC Newsletter*, page 5, 2008.

[24] Essensium: News and Events. http://www.essensium.com/news_events.html.

3
RF front-end

3.1 Introduction

To realize a low power, low cost implementation of the PCB demonstrator shown in chapter 2, a single-chip solution is preferred. The architecture of the complete chip is shown in figure 3.1.

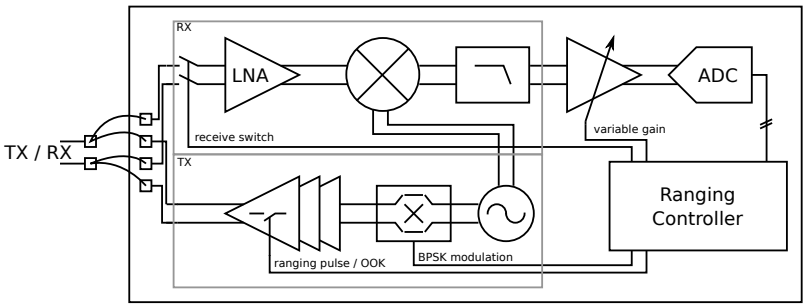


Figure 3.1: Architecture of chip implementation

This chapter describes the first part of the ranging receiver: the RF front-end. Section 3.2 will derive the circuit level specifications and with the aid of these specifications the two main building blocks of the front-end were designed. Sections 3.3 and 3.4 describe the circuit level implementations

of the LNA and the down converter respectively.

3.2 Derivation of the circuit-level specifications

To derive the circuit-level specifications, a quantitative estimation is needed of the signal bandwidth, the range of input power levels, the minimum signal to noise ratio and the location and power level of the most dominant interferers and blocking signals.

The measurements conducted in chapter 2, show that $250\ \mathrm{MHz}$ RF bandwidth and $10\ \mathrm{dB}$ SNR is needed to ensure accurate ranging. Given a receiver NF of $6\ \mathrm{dB}$ yields a total input refered noise of ($-174\ \mathrm{dBm}$ + NF + $10\log_{10}250\ \mathrm{MHz}$ =) $-84\ \mathrm{dBm}$. Given the required SNR, the lowest input signal level that can be dealt with is $-74\ \mathrm{dBm}$. The maximum transmit power allowed in the $2.4\ \mathrm{GHz}$ ISM-band is $20\ \mathrm{dBm}$, ensuring – based on the Friis transmission equation – a maximum ranging distance of $500\ \mathrm{m}$, futher degraded by the reduced antenna efficiency. The LNA gain should be sufficient high to reduce the impact of noise as implied by Friis's noise formula, yet linearity considerations pose an upper limit. Based on the gain and NF measured on the demonstrator board, the total RF gain can be limited to $29\ \mathrm{dB}$. Based on realistic NF estimates for LNA and Mixer, the gain can be divided over the two building blocks to ensure a maximum total NF of $6\ \mathrm{dB}$.

Due to the large input bandwidth, out-of-band blocking signals are likely to degrade the receivers sensitivity. Interference from Universal Mobile Telecommunications System (UMTS) transmitters – having an offset frequency of less than $300\ \mathrm{MHz}$ for the downlink and $500\ \mathrm{MHz}$ for the uplink from the ranging carrier – cause saturation in LNA and mixer if linearity is not adequate. A typical UMTS handset has a maximum output power of $21\ \mathrm{dBm}$. This number was used as an upper limit for estimating the worst-case interference, assuming close proximity. If the minimum distance is limited to $0.5\ \mathrm{m}$ and one assumes a combined antenna and on board filtering of $30\ \mathrm{dB}$, the signal strength is expected to be $-40\ \mathrm{dBm}$ at the input of the receiver. This yields a lower limit to the linearity of the receiver, since third order intermodulation products will fold in to the receivers bandwidth. To ensure all in-band intermodulation products are below the receiver's noise floor, the minimum Input-refered 3rd order Intercept Point (IIP3) should be higher than $-18\ \mathrm{dBm}$. To ensure some margin, $-10\ \mathrm{dBm}$ was imposed instead. To reduce the linearity requirements for close transmitters a low-gain option is preferred. A summary of these specifications is given in table 3.1.

	LNA	Mixer	Total
Gain (dB)	17	12	29
NF (dB)	4	18	6
Linearity IIP3 (dBm)	-10	5	-10
Current (mA)	6	4	10

Table 3.1: Receiver specifications.

3.2.1 Technology selection

After determining the circuit specifications, a suitable technology must be chosen. This choice is dominated by the PA and the Digital Signal Processing (DSP). Since the power amplifier is the most power hungry building block, it is important that the technology is optimal for this component. An important factor which will determine the efficiency is the quality factor of the inductors. Copper interconnects were introduced from $0.13\ \mu\mathrm{m}$ processes onwards, reducing resistance, increasing bandwidth and – obviously – increasing Q-factors of inductors. This in turn increases the PA efficiency. The digital parts power dissipation directly correlates with the minimum feature size of the chosen technology node. The dynamic power consumption will be lower but leakage power will rise in more advanced nodes. This as well as economical reasons (a lower Non-Recurring Engineering (NRE) cost) resulted in a design for $0.13\ \mu\mathrm{m}$ CMOS.

3.3 Low Noise Amplifier

3.3.1 Introduction

To ensure proper reception of the RF signal, typically a LNA is used. This first amplifier provides gain while minimizing the added noise. This way, the noise added by the consecutive stages has less negative impact on the SNR (as the signal after the LNA is already much large due to the amplification, so the noise added by these stages is relatively less dominant). To limit the area of the LNA and thus of the total chip, an inductor-less approach is preferred.

3.3.2 Topology overview

In literature, several topologies and LNA architectures have been proposed. They all have their up- and downsides, so a careful exploration of the different topologies is required to choose the one best suited for the ranging

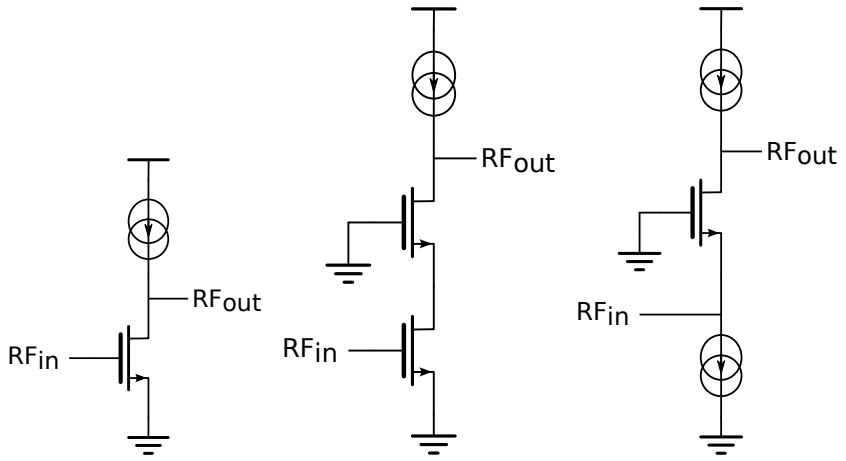
application. Besides gain and noise figure it is also important to discuss the linearity. The latter is more difficult to reach given the high bandwidth of the system, but, due to the same reason, critical for the performance: lack of linearity would decrease sensitivity in presence of blocking signals. Power consumption is yet another important parameter, to increase the autonomy time when battery operated. To discuss the different topologies, they are divided into 3 distinct categories:

- common source amplifiers [1],
- common source amplifiers with enhanced gain due to a cascode transistor [2–5],
- common gate amplifiers [6, 7].

Common Source

One of the most frequently used topologies consists of a common source amplifier (fig. 3.2(a)). This topology offers the best noise behavior when biased with an optimal current density and connected via an optimal matching circuit. The gain-frequency response is dominated by the output pole in combination with feedback through the Miller (gate-drain) capacitance, reducing the gain at higher frequencies. Furthermore, the input is mainly capacitive and needs to be matched to a resistive antenna, which is a challenge without inductors.

Traditional matching techniques such as source degradation are not an option as the use of inductors is required. Another solution is tuning the size of the input transistor which will change its input impedance. This will unfortunately harm the noise performance in exchange of better power matching. If a reasonable compromise is impossible, feedback techniques can be applied to reduce the influence of the transistor.



(a) Common Source (b) Common Source with cascode (c) Common Gate

Figure 3.2: Basic amplifier topologies

Common Source with Cascode Transistor

The Miller capacitance in a common source topology will start to dominate at higher frequencies. To reduce this effect, a cascode transistor is added (fig. 3.2(b)). Due to the low input resistance of the cascode transistor, seen by the common source transistor, the voltage gain towards the drain of the common source transistor is lower and, hence, the Miller effect will be reduced.

The linearity of the circuit, as a downside of this approach, does not remain unharmed as due to the reduced headroom, the signal will already distort at lower input signal levels. Furthermore, the addition of one more active element will certainly not improve the noise figure. An extra difficulty is that due to the change of load of the common source transistor, its input impedance changes. Typically, the input resistance increases while the input capacitance decrease.

Common Gate

A common gate amplifier (fig. 3.2(c)) typically has a higher noise figure than a common source LNA (except for very low bias currents) [8]. This topology, however, is very interesting because of the ability to easily scale its input impedance (1/gm) and its improved linearity.

Topology comparison and selection

Three different LNA topologies have been discussed: a common-source, a common-source with cascode transistor and a common-gate topology. If a rather high NF can be tolerated, the common-gate topology offers very low power consumption as additional benefit. If a lower noise figure is desired a common-source topology should be used. To realize a high gain in the first stage a cascode transistor can be added. This extra active element will increase the noise a little, the cascode will decrease the linearity due to a reduction of the headroom. As the power amplifier [9] will be a differential system, the antenna in the transmit path should also be differential. This eliminates the need for baluns and prevents the extra losses they cause. There are two options for the LNA:

1. A differential configuration: this will increase the input noise figure but will reject common mode noise from supply and substrate and will prevent losses from a balun (estimated at $1.5\ \mathrm{dB}$, which would also increase the overall noise figure).

2. A single-ended configuration: This requires a balun, but allows the noise figure of the LNA to be reduced. The loss of the balun will augment the noise figure. The extra cost of an external balun or the die area needed for an on-chip one should, however, not be forgotten.

The differential approach has more advantages. It is the most straightforward configuration since the PA is built differentially and it will reduce the cost of external components or eliminate bulky on-chip transformers. Furthermore, the differential nature will increase the linearity because the available voltage headroom is doubled.

Transmit-receive switch

The last building block in the RF front-end, is the transmit-receive switch. Because of the stringent linearity requirements combined with high output levels, this switch is hard to design in plain CMOS. However, since the transmitter already has a fast power switch which is necessary for the ranging functionality, it can be disconnected during the receive phase so in fact no additional switch is required in the TX path. Only the on-chip output inductors of the PA will remain connected through the bondwires (L_{bw}) in the off state (fig. 3.3). These can be used to facilitate the matching of the capacitive LNA input. However, a switch is still needed to protect the LNA during the transmit phase. These switches are more easily implemented

since the linearity requirement is relaxed significantly as the RX only processes relatively weak signals.

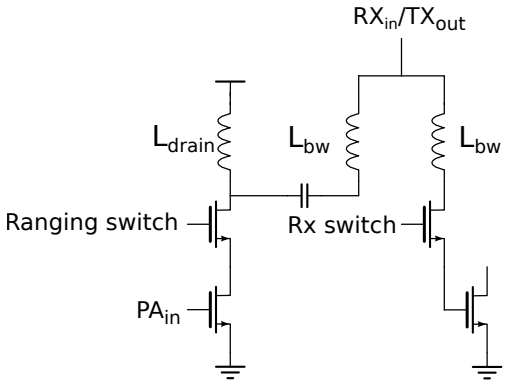


Figure 3.3: Reuse of the PA inductor.

3.3.3 Implementation

The sizing of the transistors in the LNA follows a structural (iterative) design procedure, the values posed are found after a few iterations. First the input transistor will be sized, next the load and afterwards the bypass circuit and the input switch. The LNA makes use of the PA output as matching structure of which the interconnects are shown in figure 3.4. The PA bondwires are in parallel with the input capacitance of the LNA, this way the input impedance of the common-source transistor is made resistive at the resonant frequency.

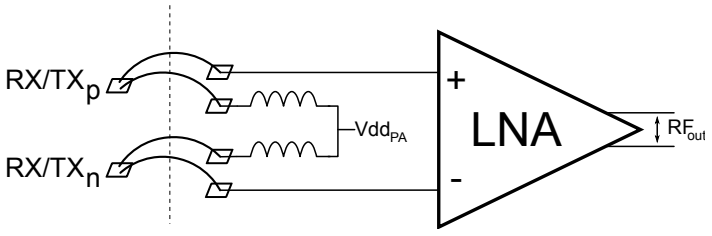


Figure 3.4: LNA interconnect with the PA.

Sizing of the input transistor

The lowest noise topology is a common-source amplifier. Starting the design from one transistor which will function as input stage, loaded with 120 fF (which is a first estimate of the input capacitance of the mixer and the capacitance of the interconnections between mixer and LNA) and a current source, the optimal transistor parameters can be found. Figure 3.5 shows the test-bench. The value of the bond-wire inductance is estimated at 1.5 nH, the output common-mode voltage is fixed at 800 mV by means of a low frequency Operational Transconductance Amplifier (OTA).

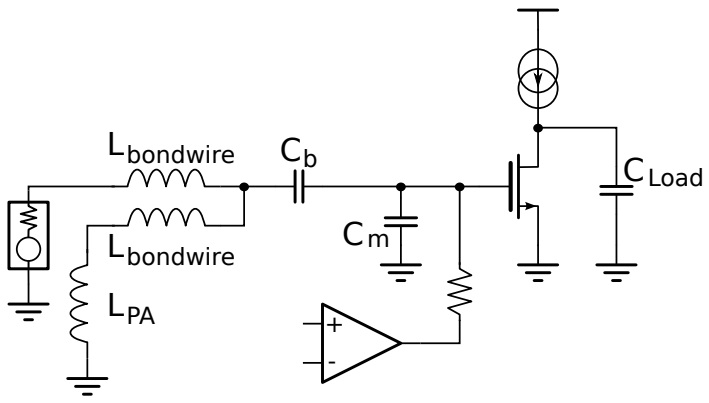


Figure 3.5: Test-bench to size the input transistor of the LNA.

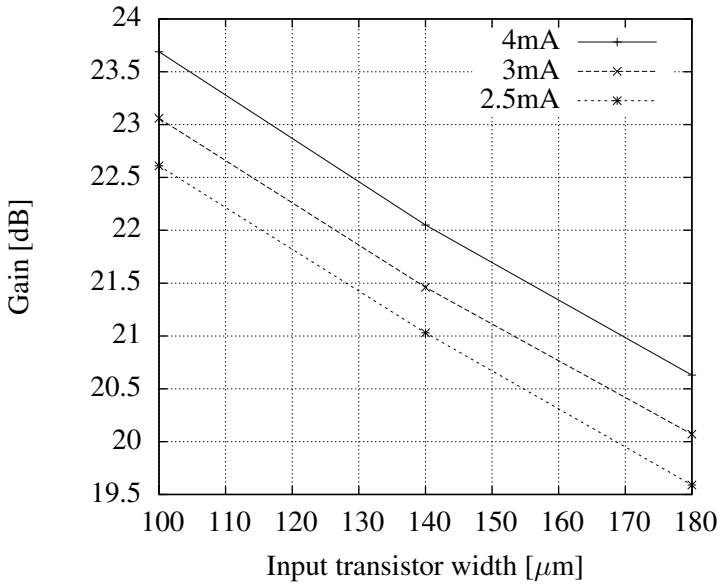


Figure 3.6: Gain of the common-source input stage as function of transistor width, for different bias currents.

The matching capacitance C_m is chosen so to minimize the noise figure of this stage. Figure 3.6 and figure 3.7 show the noise figure and the AC gain of the input stage as function of channel width and bias current. Looking at the measurements we can pick the most suitable corner. A minimum noise figure of $2\ \mathrm{dB}$ and $20\ \mathrm{dB}$ gain are required, yielding $3\ \mathrm{mA}$ current and $140\ \mu\mathrm{m}$ width. In this corner C_m should be $950\ \mathrm{fF}$.

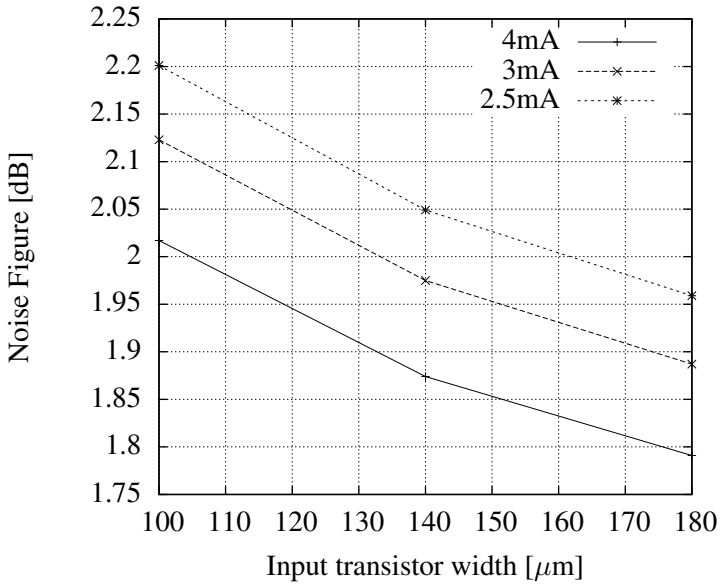


Figure 3.7: NF of the common-source input stage as function of transistor width, for different bias currents.

Sizing of the active load transistor

After sizing the input transistor, the load is considered. This load transistor will act as the output transistor of a current mirror providing the bias current to the input transistor. The width, determined to give the LNA maximum small signal gain, is $32\ \mu\mathrm{m}$. The resulting noise figure is $2.9\ \mathrm{dB}$ and the gain is $19.2\ \mathrm{dB}$. The test-bench is shown in figure 3.8. The lower gain and higher noise figure are due to imperfections of the P-type MOSFET (PMOS) load. To improve on this, an inductive load could be used. Of course, this will increase the die area, and hence the cost, substantially.

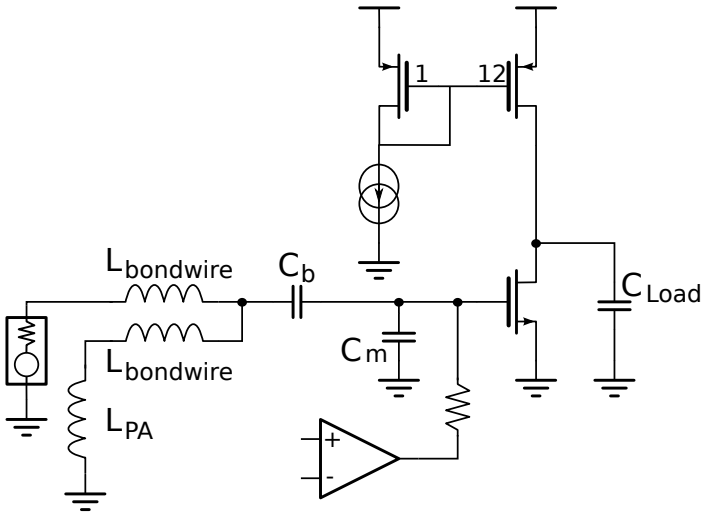


Figure 3.8: Test-bench to sizing the load transistor of the LNA.

Design of the bypass circuit

When high power input signals are received, noise is less of a concern and linearity forms a major limitation on the signal quality. A bypass circuit provides a low gain pass-through in case of high input levels, increasing the dynamic range. Of course when the circuit is disabled, no effect should be noticed on the performance of the LNA. The proposed circuit is shown in figure 3.9. When the bypass switches are activated and the current through the input stage is divided by ten, the resulting gain is only $2\ \mathrm{dB}$. If the current is also switched the gain reduces even further to $-7\ \mathrm{dB}$. This offers 2 configurations with reduced gain. Since the variable gain amplifier is expected to have $35\ \mathrm{dB}$ of configurable gain, as was the case on the PCB demonstrator (chapter 2), the resulting range should provide sufficient dynamic range. The IIP3 during normal operation is $-1.2\ \mathrm{dBm}$. With reduced gain it is respectively $-3.5\ \mathrm{dBm}$ and $-5.4\ \mathrm{dBm}$. Normal operation yields the best IIP3. So an attenuator after the LNA could yield better overall performance but at the cost of extra power consumption. All these linearity figures are satisfactory for the application. The gain reduction is only important for the subsequent mixer and filter stages, to reduce the amplitude of the strong input signals.

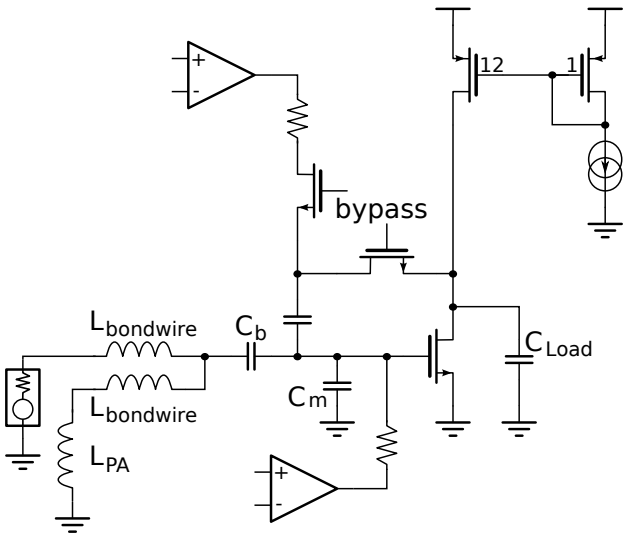


Figure 3.9: Test-bench for the design of the bypass circuit.

Design of the Input switch

The input switch is used to protect the LNA input from the high transmit levels of the PA and to disconnect the impedance of the LNA during transmission so that the TX power is radiated by the antenna and not absorbed by the LNA. The switch is constructed as a binary scaled array of thick gate-oxide transistors. A schematic is shown in figure 3.10. The thick oxide is necessary to withstand the high output power of the PA. When the LNA is connected, the array provides the matching capacitance. The drain-bulk and source-bulk capacitance is always connected, but by choosing the size of the gate, the gate channel capacitance is made variable. This way differences in bond-wire length, and thus inductance, between the different packages can be compensated. The gate adds a resistance in front of the LNA and will thus degrade the noise figure and the overall gain. To fully form the channel it is important to drive the gate with a sufficiently high voltage. Using a level converter the gate is attached to a 3.3 V supply. This results in a noise figure of 3.45 dB and an overall gain of 17.6 dB.

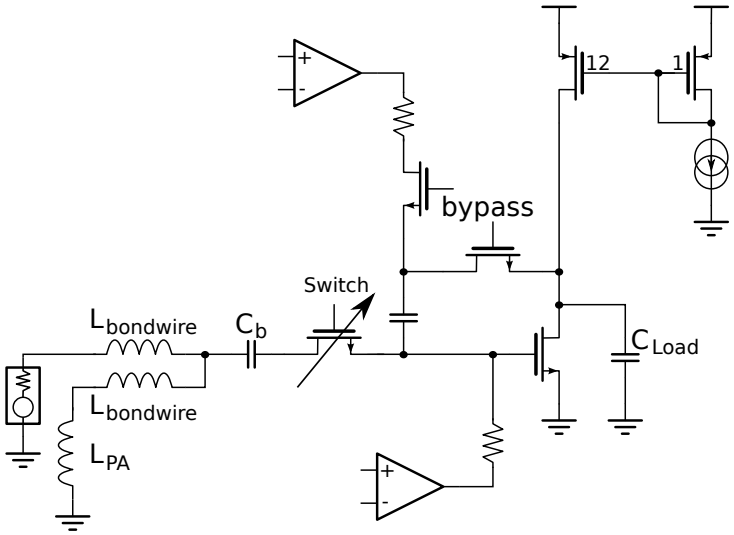


Figure 3.10: Test-bench for the design of the RX switch.

Effect of MIM vs finger capacitances

What's left is the input capacitor (C_b). In the previous simulations the capacitors were ideal. Reliability requires Metal-Insulator-Metal (MIM) capacitors. To reduce the processing steps interdigital capacitors (finger capacitors) were selected as these do not require an extra mask set. Compared to MIMs, finger capacitors have a lower Q factor and higher substrate coupling. The value is chosen to obtain minimal noise figure, which occurs at 6.3 pF. Around this value there is an optimum because on one hand further increasing the capacitance will raise the parasitics and on the other hand lower capacitors will show higher series resistance. Both effects increase the noise figure. The resulting noise figure is 4.1 dB, the gain ends up at 16.6 dB.

If instead a MIM capacitor would be used instead of a finger capacitor, the gain would remain at 17.6 dB and the noise figure would be 3.8 dB. Increasing the MIM to 10 pF lowers the noise figure again to 3.65 dB.

Since the PA is not DC-coupled, one should be able to remove the capacitors completely. Of course, this will increase the risk of damage during an Electrostatic Discharge (ESD) event. Now, a voltage divider is formed between the capacitor and the gate input. An other advantage is that the gate is protected from DC voltages attached to the inputs, which gives more freedom at board level.

Testability

To improve the testability, some parameters are programmable. The common mode voltage at the output, the current through the input stage and the input switch size are configurable. This gives the freedom to compensate for temperature and corner variations.

Layout

A die-micrograph of the LNA is shown in figure 3.11. Special care was taken to reduce the length of the input traces and hence eliminate parasitic capacitance as much as possible.

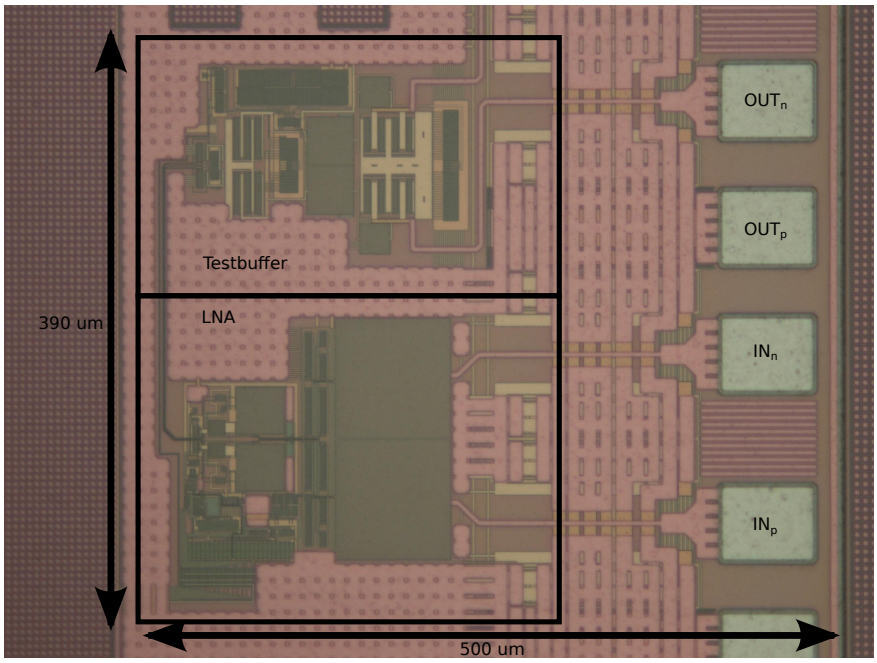


Figure 3.11: Micrograph of the LNA.

3.3.4 Measurements

For measurement purposes, a standalone LNA with an output buffer was included on the SoC. The measurement procedures and results are described in the following paragraphs.

Power consumption

The current consumption has been measured by means of an Agilent E3440 Multimeter in the power supply path of the LNA. The results show good correspondence with the simulations and are shown in figure 3.12.

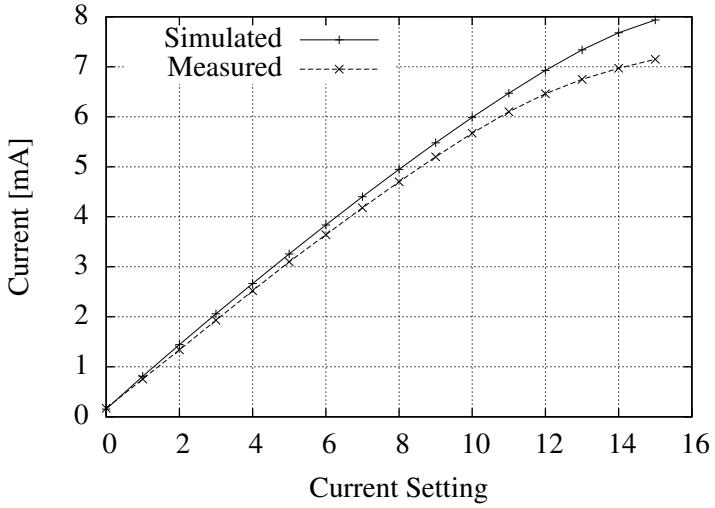


Figure 3.12: Current consumption LNA.

At a higher current setting, the supply current is a bit compressed due to the resistivity of the supply path, which is estimated at $4\ \Omega$.

Matching

To measure the matching, a Vector Network Analyzer (VNA) has been used. The resulting S_{11} characteristic is depicted in figure 3.13 and compared with the simulation. The measurement differs significantly from the simulation.

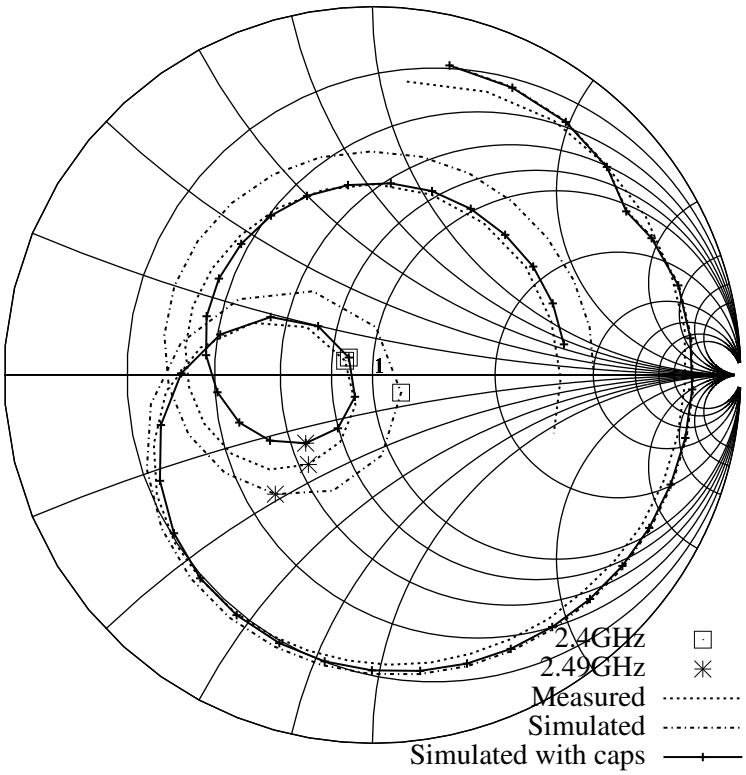


Figure 3.13: Measured and Simulated S_{11} (with and without extra capacitors).

Detailed inspection of the schematics and layout revealed that the post layout simulations did not include sufficient parasitic capacitance. A better estimate of the parasitics led to much better correspondence, as shown in figure 3.13.

Gain - Bandwidth

The S_{21} characteristic was measured and compared to the simulated characteristic. The measurements shows severe degradation compared to the simulation. Careful inspection of schematics and layout brought to light

that the parasitic resistance present at the interconnection of the input capacitor is not correctly modelled. The spice models of the capacitors only included the resistance of the individual fingers, not the interconnection resistance of the fingers. Since this resistance is part of the described component, parasitic extraction won't add the resistance to the extracted netlist. Figure 3.14 compares the measured and simulated S_{21}, along with a new simulation with a better model for interconnect resistivity (2x 27 Ω) which was not included in the used fingercap models. If the losses of the input and output baluns, output buffer and matching network are subtracted the gain of the LNA itself is 12.5 dB, without the extra resistance the simulated gain is 16 dB.

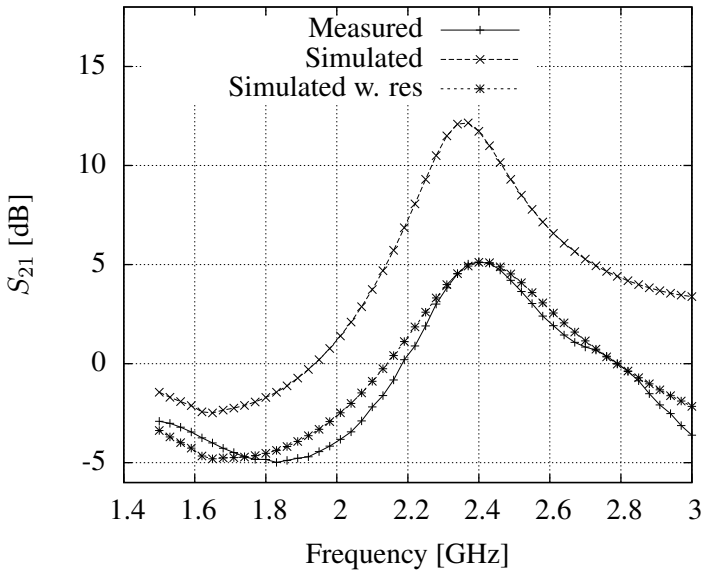


Figure 3.14: Measured and Simulated S_{21}.

To confirm the hypothesis that the wrongly modelled interconnect resistance is indeed responsible for the reduced gain of the LNA, a Focussed Ion Beam (FIB) operation was performed. The fingers of the capacitor were shorted, in this way the capacitor was short circuited and the series resistance was significantly reduced. After the FIB operation the gain increased with 4 dB, which corresponds well to the initial simulation.

Noise figure

The noise figure was measured by means of a noise source with a known Excess Noise Ratio (ENR) and a spectrum analyser with a low-noise pre-amplifier. The output noise is measured when the noise source is on and off and the noise figure is calculated by using the Y-factor method.

The ENR is defined as the ratio of the noise temperature when the noise source is on (T_{HOT}) and off (T_{COLD}).

$$ENR = \frac{T_{HOT} - T_{COLD}}{T_0} \tag{3.1}$$

By measuring the output noise power of the device, when the source is respectively on (N_{HOT}) and off (N_{COLD}), the Y-factor can be calculated.

$$Y = \frac{N_{HOT}}{N_{COLD}} \tag{3.2}$$

The noise factor – and as a result the noise figure – follows directly out of the ENR and the Y-factor.

$$F = \frac{ENR}{Y - 1} \tag{3.3}$$

$$NF = 10 \log \frac{ENR}{Y - 1} \tag{3.4}$$

The measured noise figure was 9.2 dB which corresponds well to the simulated 9.4 dB (when taking the extra resistance into account). The FIB improved the noise figure by an additional 4 dB.

Linearity

The linearity of the LNA is verified by applying a 2 tone signal. The power of the resulting first order and third order intermodulation terms are shown in figure 3.15. The IIP3 is around -1 dBm, related to the a single tone input power. The IIP3 point with improved gain will be around 4 dB lower.

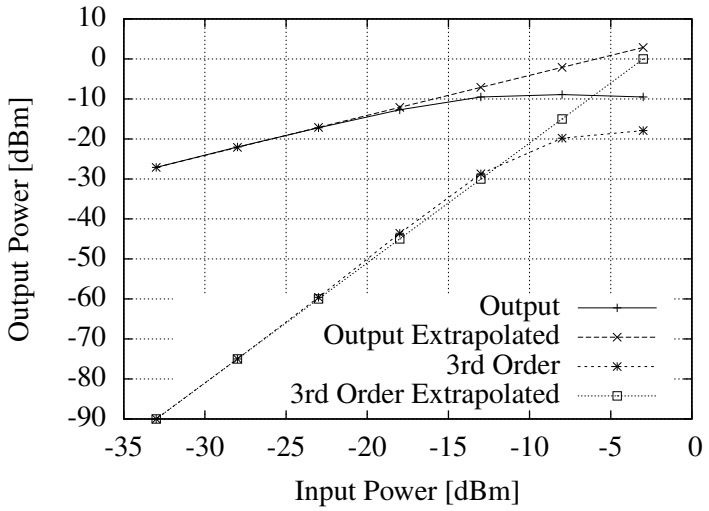


Figure 3.15: LNA Linearity.

3.3.5 Conclusion

A differential LNA is designed by combining two single-ended LNAs. A systematic approach resulted in a short design cycle, fulfilling the specifications posed in table 3.1. After the schematic simulations returned satisfactory results, the layout of the building block was drawn and simulated with extracted parasitics.

The measured results revealed a deviation from the simulated results. Carefull inspection of the post-layout netlist showed that some parasitic resistances in the finger capacitors were not modelled correctly. The simulation was run again including more accurately estimated parasitics. The results showed good correspondence to the measurements.

3.4 Mixer

3.4.1 Introduction

After the RF signal is amplified, it is less sensitive to noise. This gives more freedom on the subsequent signal manipulation. The desired final result – an accurate calculation of the distance – will be done digitally. To minimize the power required to calculate this result, only the desired signal should be processed. The RF signal – situated around 2.45 GHz – should be translated to baseband or a low intermediate frequency. This way slower digitizers (which are less power hungry) can be used. To perform this translation, a mixer is needed.

3.4.2 Topology overview

There are several topologies to realize a mixing function. Comparing these in terms of conversion gain, input intercept point, spurious response, isolation and noise figure will give an indication of the most suitable topology for the ranging system. The main classes of mixers are

- a single device mixer [10–13],
- a single balanced mixer [14–16],
- and a double balanced mixer [17–19].

All of these exist in both active and passive variants. The active variants are preferred, as they provide extra gain and a lower noise figure can be reached. If the linearity is a concern, circuit solutions have to be found or a passive topology will be necessary.

Single device nonlinear mixer

A single-device mixer comprises one active (transistor) or passive (diode) non-linear component. By injecting the LO signal and RF signal into this component the non-linear relationship between current and voltage will realize the mixing function. A diode shows an exponential behavior, whereas a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in long channel regime shows a quadratic behavior, generating fewer unwanted spectral components. However, the simple topology of this mixer doesn't allow much freedom, which results in a few downsides. Both the LO and the RF signal, need to be fed at the entrance of the device. Since we are

aiming for a zero-IF architecture, passive filtering to provide sufficient isolation is impossible (LO and RF signal have the same frequency). This problem can be partially solved by using an active configuration: one could add a cascode transistor which is switched by the LO signal or the LO signal could be injected in the source of the transistor (through a DC-blocking capacitor) (fig. 3.16).

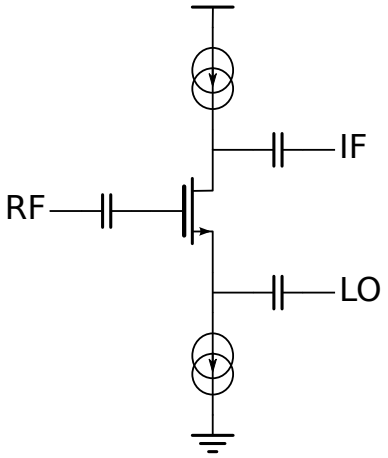


Figure 3.16: Single device mixer.

Single balanced mixer

A common way of implementing a single-balanced mixer is by first converting the incoming RF signal into a current and then performing a multiplication of this current with a square wave with the frequency of the LO signal. Such a multiplication can be easily implemented in CMOS (fig. 3.17), by driving the transistors with a sufficiently large LO signal so that the transistors are switching on and off. Switching mixers rely on time variance rather than on non linearity for generating spectral components not present in the input signal. Due to the switching nature, the output contains the sum and difference components of the LO signal (and its harmonics) and the RF signal. The most obvious choice for the desired IF signal is $(f_{RF} - f_{LO})$, the strongest mixing product with the lowest frequency. To clear the signal from other mixing products, it must be filtered.

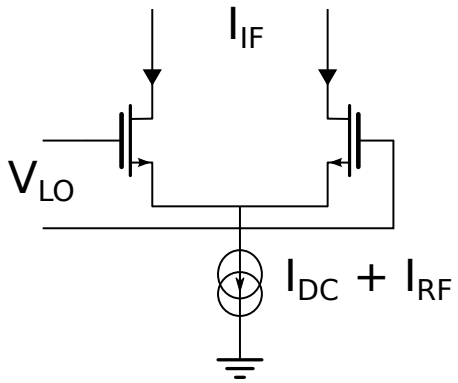


Figure 3.17: Single-balanced Mixer.

The main cause for mixer nonlinearity is the transconductance, the voltage-current conversion of the RF signal. This should be as linear as possible. Different topologies based on common-gate or common-source configurations can realize this.

Double balanced mixer

To provide LO-IF isolation and to suppress the self-mixing of the LO signal, one can combine two single-balanced circuits into a double-balanced mixer. By connecting the two circuits in an anti-parallel configuration the even LO harmonics are removed from the output giving rise to a high LO-IF isolation. The linearity of the mixer is once again limited by the V/I-conversion of the RF-signal.

A typical double balanced mixer is a Gilbert cell (fig. 3.18). This cell converts the incoming RF signal into a current by using a differential pair. This pair is loaded with switches to perform the multiplication with the LO signal. After the multiplication the IF current is converted to a voltage over the output resistors. With proper design, low noise figures and high gain can be achieved with these topologies. In scaled technologies, however, the supply voltages are very limited. This results in a limited voltage swing which reduces the linearity.

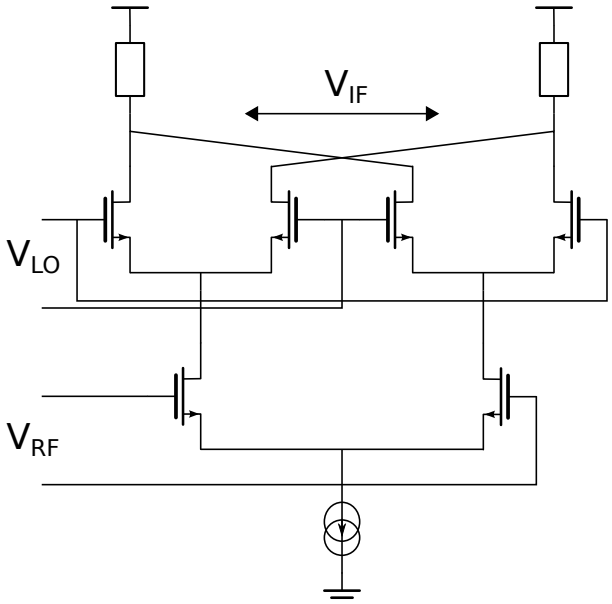


Figure 3.18: Double balanced Mixer.

3.4.3 Topology selection

Gain and noise are important parameters in the receiver. To be able to combine these, an active mixer should be used. A classic topology like a Gilbert cell seems the most promising. The downside of this approach is that the linearity will be limited. There are a few approaches to facilitate the gain linearity trade-off:

1. Current starving: In a Gilbert cell, the RF signal is transformed in to a current by a transconductor stage. This current is then switched and translated into a voltage over the output resistance (either active or passive). The transconductor is directly fed through the output resistors, which will put a limit on either the output resistance or the transconductor drain current. To reduce the voltage drop over these resistors, an extra current source can be added to feed the transconductor (figure 3.19). The resulting circuit has a higher transconductance and can use a higher output resistance yielding a higher gain, while the DC voltage drop over the output resistors can be minimized and hence the drain-source voltage of the transconductors can be higher which in turn will increase the linearity.

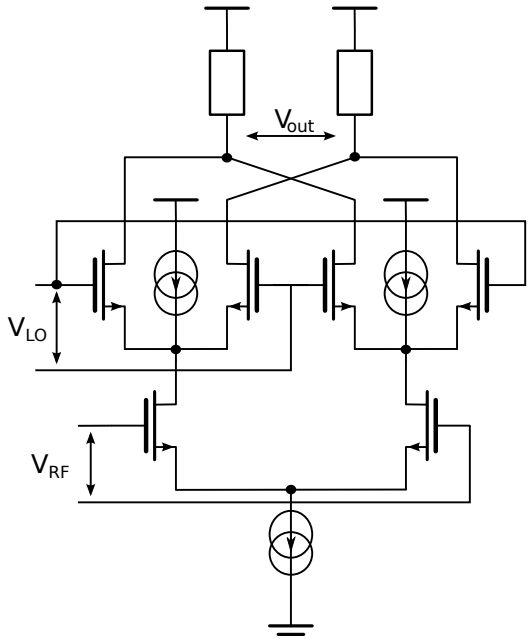


Figure 3.19: Gilbert-cell mixer with current starving.

2. Loading with a TransImpedance Amplifier (TIA): To reduce the voltage swings in the internal nodes, the Gilbert cell can be loaded with a transimpedance amplifier (figure 3.20). This amplifier will offer a low impedance node to the mixer and will thus reduce the voltage on the internal nodes, hence lowering the effect of the non-linear output impedance of the transconductor. The TIA only needs the bandwidth of the base-band signal, and its feedback resistance will determine the transimpedance and the final conversion gain. AC coupling between the TIA and the transconductor allows seperate optimization of both stages. Typicaly a high common mode signal is wanted at the output of the transconductor to maximize linearity while the common mode output of the TIA should be mid-supply to allow maximum voltage swing.

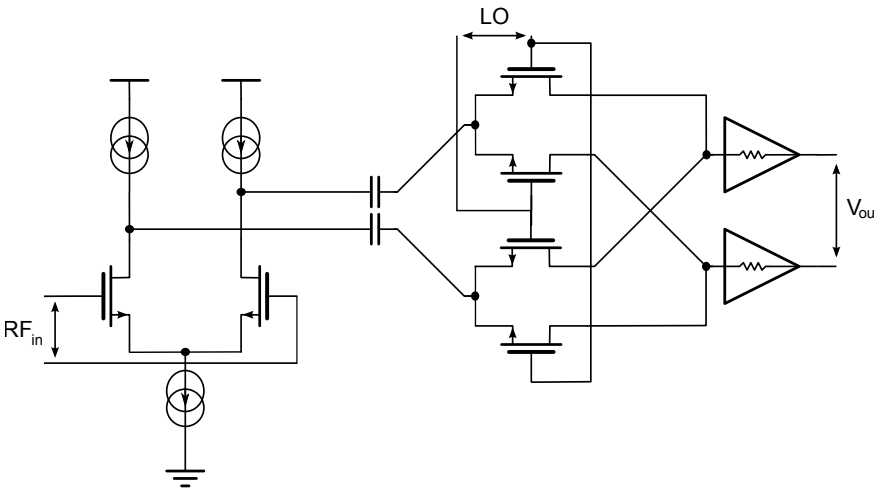


Figure 3.20: Mixer loaded with TIA.

At this stage, linearity is a very important parameter: The LNA offers high gain and there is little selectivity to reduce out-of-band signals. This makes the TIA solution the most promising since the voltages in the circuit can be reduced to a minimum giving maximum headroom to the transconductor stage while reducing the effect of the non-linear output resistance.

3.4.4 Implementation

After selecting the right topology, the circuit elements were dimensioned to meet the specifications in table 3.1. There is, however, one extra requirement: the input capacitance of the mixer stage and its interconnects coming from the LNA should have a combined capacitance of less than 120 fF.

A structural design procedure will be described to realize a highly efficient building block in a short design time. First, the input transconductor, which converts the incoming voltage into a current, is designed. The switches are the next step followed by the loading TIA.

Design of the transconductor

To design the transconductor, the switches are omitted and the transconductor is loaded with an ideal 1.5 kΩ TIA. The schematic is shown in figure 3.21.

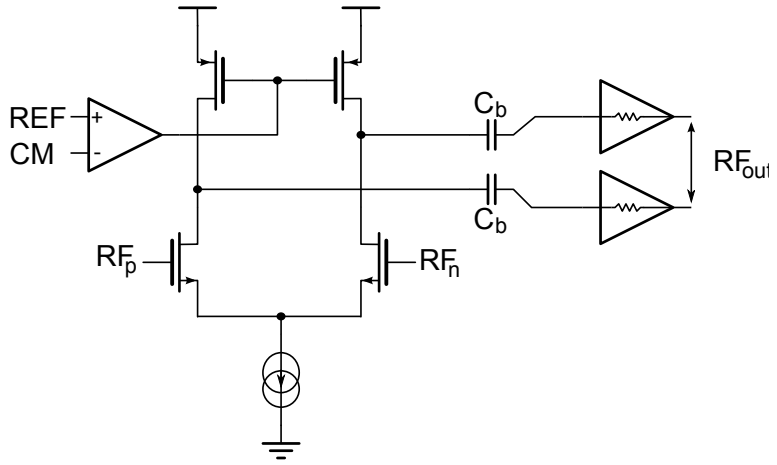


Figure 3.21: Test-bench for the design of the mixer's transconductor.

The design goals for the transconductor are: low noise, high transconductance, while keeping input capacitance and current consumption limited. The output impedance of the N-type MOSFET (NMOS) and the PMOS should be kept sufficiently large to ease the design of the TIA.

These arbitrary specifications can be converted into transistor level specifications:

- The transconductor will be realised by a NMOS differential pair. A minimum transconductance of $8\ \mathrm{mS}$ is required to realize a gain of $20\ \mathrm{dB}$ over the $1.5\ \mathrm{k\Omega}$ transimpedance. The switching itself will add an extra $8\ \mathrm{dB}$ loss, resulting in a total conversion gain of $12\ \mathrm{dB}$.
- The input noise is given by:

$$v_{n,rms} = \frac{\sqrt{4kT \cdot (\Gamma_n \cdot gm_n + \Gamma_p \cdot gm_p)}}{gm_n} \tag{3.5}$$

  The input noise of the mixer should have a minimal effect on the total NF. Since the output noise of the LNA is $7.1\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, a mixer NF of $6\ \mathrm{dB}$ or input noise of $1.25\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ will result in a total receivers NF of $3.6\ \mathrm{dB}$
- The input capacitance can be kept sufficiently small by minimizing the input transistor area. The input capacitance should be smaller than $60\ \mathrm{fF}$ (to have a total capacitance of $120\ \mathrm{fF}$ for the I and Q stage)

- The output resistance is mainly determined by the length of the input transistor (3.6). To increase the resistance, the length is increased to $250\ \mathrm{nm}$ instead of the minimal $130\ \mathrm{nm}$.

$$R_{out} = \frac{1}{\lambda \cdot I_D} \tag{3.6}$$

$$\text{where } \lambda \approx \tfrac{1}{L}$$

The resulting specifications are plotted in an Inversion Coefficient (IC) [20]-Drain current (ID) graph in figure 3.22. The minimum current required is around $1.3\ \mathrm{mA}$, with an inversion coefficient of 23. This results in a width of $25\ \mu\mathrm{m}$.

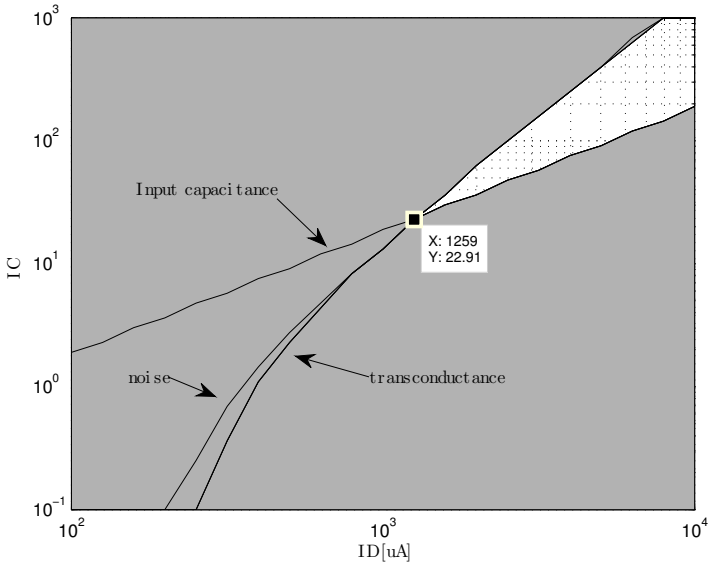


Figure 3.22: IC - ID graph with design constraints for the mixers transconductor.

The active load transistor of the transconductor should be minimized to reduce the noise it generates and to maximize its output resistance. The width is fixed at $20\ \mu\mathrm{m}$.

Design of the switches

The switches realize the frequency conversion. The test-bench used to simulate the performance of the switches is shown in figure 3.23. The current generated by the transconductance is multiplied with a square wave. The resulting product will have its main frequency components around $f_{RF} - f_{LO}$ and $f_{RF} + f_{LO}$. The mixer will perform a down conversion, so the lowest frequency component, will be the one of interest.

In order to get the transistors to act as switches – and to obtain a clean square wave multiplication, they should be driven by a sufficiently strong signal. This signal will be generated by a buffer amplifier. To reduce the power consumption of this buffer, the gate capacitances of the switch should be minimized. Furthermore, the channel on-resistance will come in series with the TIA and should be kept low to force the signal current flowing to the TIA instead of being dissipated in the output resistance of the transconductor.

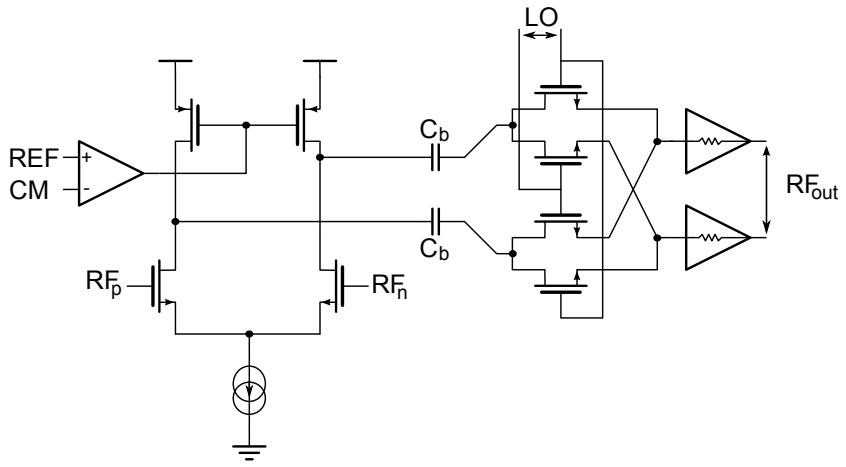


Figure 3.23: Test-bench for the design of the mixer's switches.

Impedance conversion

Due to the frequency conversion, the transconductor will see a transformed load impedance, $Z_{TIA}(s)$. To calculate the load impedance seen by the mixer, the simplified circuit shown in figure 3.24 is considered.

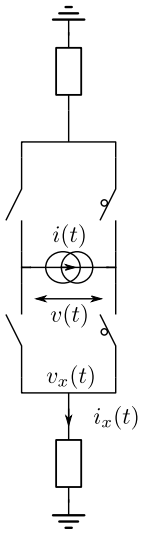


Figure 3.24: Impedance through a switching mixer.

To start the calculation all current and voltages are expressed as a Fourier series:

$$v(t) = \sum_k V_k e^{j(k\omega_{LO}+\omega_{RF})t} \tag{3.7}$$

$$i(t) = I\cos(\omega_{RF}t) = \frac{I}{2}(e^{j\omega_{RF}t} + e^{-j\omega_{RF}t}) \tag{3.8}$$

$$v_z(t) = \sum_k V_{zk} e^{j(k\omega_{LO}+\omega_{RF})t} \tag{3.9}$$

$$i_z(t) = \sum_k I_{zk} e^{j(k\omega_{LO}+\omega_{RF})t} \tag{3.10}$$

$$V_{zk} = Z_{TIA}\Big(j(k\omega_{LO}+\omega_{RF})\Big) I_{zk} \tag{3.11}$$

The mixing function is implemented as a multiplication of the current with

a square wave, yielding:

$$\begin{aligned} sq(\omega_{LO}t) &= \begin{cases} 1 & : \quad -\frac{\pi}{2} \leq \omega_{LO}t + 2k\pi < \frac{\pi}{2} \\ -1 & : \quad \frac{\pi}{2} \leq \omega_{LO}t + 2k\pi < \frac{3\pi}{2} \end{cases} \quad k \in \mathbb{N} && (3.12) \\ &= \frac{2}{\pi} \sum_{k \in \mathbb{O}} \frac{1}{k} e^{jk\omega_{LO}t} && (3.13) \\ i_z(t) &= i(t) \cdot sq(\omega_{LO}) && (3.14) \\ &= \frac{2I}{\pi} \sum_{k \in \mathbb{O}} \frac{1}{k} e^{j(k\omega_{LO}+\omega_{RF})t} && (3.15) \\ & \quad \forall k \in \mathbb{O} : \exists n \in \mathbb{Z} : k = 2n+1 \end{aligned}$$

The linear relationship in the frequency domain between current and voltage over the TIA load allows to calculate $v_z(t)$:

$$\begin{aligned} V_{zk} &= Z_{TIA}\Big(j(k\omega_{LO} + \omega_{RF})\Big) I_{zk} && (3.16) \\ &= \frac{2IZ_{TIA}\Big(j(k\omega_{LO} + \omega_{RF})\Big)}{k\pi} \quad k \in \mathbb{O} && (3.17) \\ & && (3.18) \end{aligned}$$

To find the impedance seen through the switches, it is sufficient to calculate $v_z(t)$ back to $v(t)$ by multiplying it with the square wave.

$$\begin{aligned} v(t) &= 2v_z(t) \cdot sq(\omega_{LO}t) && (3.19) \\ V_k &= \frac{8I}{\pi^2} \sum_{n \in \mathbb{O}} \frac{1}{(k-n)n} Z_{TIA}\Big(j\left((k-n)\,\omega_{LO} + \omega_{RF}\right)\Big) && (3.20) \end{aligned}$$

These final results reveal that the impedance around the fundamental mirror frequencies will have the most influence. When $k = 0$ both $n = -1$ (the wanted mixing term) as well as $n = 1$ (the mirror frequency) have equal influence on the impedance seen from the transconductors. To minimize the resistance seen by the transconductor, the impedance at all harmonics should be minimized. In practice, the high mirror frequency ($f_{RF} + f_{LO}$) will be the most important, since the higher harmonics will be severely reduced by the $\frac{1}{(k-n)n}$ factor in equation (3.20).

Design of the TIA

The transimpedance amplifier will offer a low impedance to the preceding stage and transform the incoming current to a voltage. The circuit will be

implemented as differential inverters with the sources of the NMOS transistors connected together to a current source. A simplified single-ended representation is shown in figure 3.25.

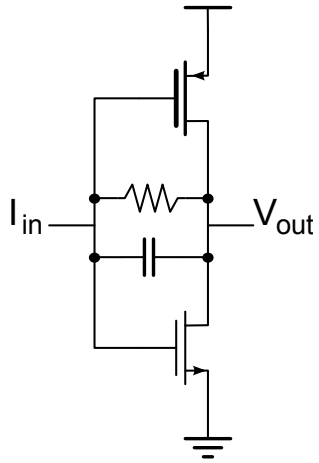


Figure 3.25: Simplified single-ended representation of the transimpedance amplifier acting as load for the mixer.

The important parameters of the TIA are :

- transimpedance,
- bandwidth,
- input impedance over frequency (most important at $f \pm f_{LO}$),
- input-referred noise current,
- and linearity.

The different parameters will be calculated in the following paragraphs.

The input impedance will be derived from figure 3.26.

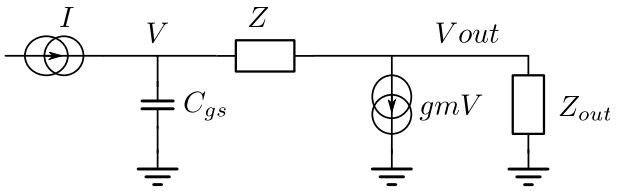


Figure 3.26: Small signal schematic of the TIA.

$$Z_{in} = \frac{\frac{Z+Z_{out}}{1+A}}{1+\frac{sC_{gs}(Z+Z_{out})}{1+A}} \tag{3.21}$$

$$\approx \frac{\frac{Z}{1+A}+\frac{1}{g_m}}{1+\frac{sC_{gs}}{g_m}} \tag{3.22}$$

$$A = g_m Z_{out} \tag{3.23}$$

$$Z_{out} = \frac{r_o}{1+sr_oC_{ds}} \tag{3.24}$$

$$Z = \frac{R}{1+sRC} \tag{3.25}$$

The resulting input impedance is the transimpedance divided by the loop gain in series with transconductance. As shown in equation (3.20), it is important to keep the input impedance low. To reduce the impedance at the high mirror frequency, the input pole of the amplifier should be located at a sufficiently high frequency while the bandwidth of the transimpedance should be limited to the baseband bandwidth.

The transimpedance will be determined from the small signal diagram shown in figure 3.26.

$$
\begin{aligned}
Z_{trans}(s) &= -\frac{ZA + Z_{out}}{1+A} - \frac{ZA + Z_{out}}{sC_{gs}\left(Z + Z_{out}\right)} && (3.26)\\
&\approx -Z + \frac{1}{g_m} - \frac{(1+A)\left(Z - \frac{1}{g_m}\right)}{sC_{gs}\left(Z + Z_{out}\right)} && (3.27)\\
&\approx \frac{Z - \frac{1}{g_m}}{1 + \frac{sC_{gs}(Z+Z_{out})}{1+A}} && (3.28)\\
&\approx \frac{Z - \frac{1}{g_m}}{1 + \frac{sC_{gs}}{g_m}} && (3.29)
\end{aligned}
$$

The DC-transconductance is, as expected, $R - 1/g_m$, which will approximately amount to R. The bandwidth will be determined by the pole formed by $1 + sR\left(C + \frac{C_{gs}}{1+A}\right)$ and degraded by the input impedance.

The noise current of the TIA consists of two noise sources: the feedback resistor and the transistor, which will create white and 1/f noise. To estimate the effect, the transfer function between the noise sources and the output voltage will be determined.

The equivalent feedback resistance noise circuit is shown in figure 3.27, yielding

$$
\begin{aligned}
\frac{V_{out}}{I_R} &= Z\frac{AZ + Z_{out}}{(1+A)\left(Z_{out} + Z\right)\left(1 + \frac{Z+Z_{out}}{1+A}sC_{gs}\right)} && (3.30)\\
&\approx Z\frac{1 + \frac{Z_{out}}{Z_{out}+Z}\frac{sC_{gs}}{g_m}}{1 + \frac{sC_{gs}}{g_n}} && (3.31)
\end{aligned}
$$

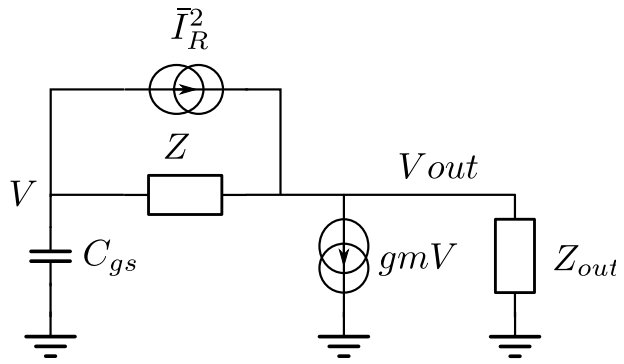


Figure 3.27: Small signal schematic of the TIA with a noise source in the feedback path.

The transfer function of the drain current noise to the output voltage is shown in figure 3.28

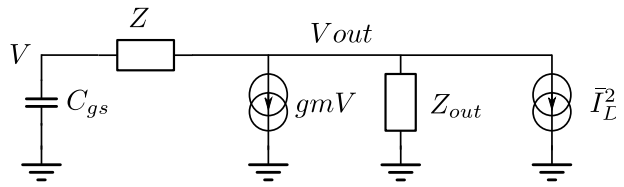


Figure 3.28: Small signal schematic of the TIA with a noisy transistor.

$$\frac{V_{out}}{I_D} = \frac{Z_{out}}{1+A}\frac{1+sC_{gs}Z}{1+sC_{gs}\frac{Z_{out}+Z}{1+A}} \tag{3.32}$$

$$= \frac{1}{g_m}\frac{1+sC_{gs}Z}{1+\frac{sC_{gs}}{g_m}} \tag{3.33}$$

The resulting voltage noise spectrum at the output and current spectrum at

the input is given by

$$\bar{V}_{out}^2 = \frac{\left(\frac{1}{gm}(1+sC_{gs}Z)\right)^2 \bar{I}_D^2 + \left(Z(1+\frac{Z_{out}}{Z+Z_{out}}\frac{sC_{gs}}{gm})\right)^2 \bar{I}_R^2}{\left(1+\frac{sC_{gs}}{gm}\right)^2} \tag{3.34}$$

$$\bar{I}_n^2 = \frac{\left(\frac{1}{gm}(1+sC_{gs}Z)\right)^2 \bar{I}_D^2 + \left(Z(1+\frac{Z_{out}}{Z+Z_{out}}\frac{sC_{gs}}{gm})\right)^2 \bar{I}_R^2}{(Z-\frac{1}{gm})^2} \tag{3.35}$$

$$\bar{I}_R^2 = \frac{4kT}{R} \tag{3.36}$$

$$\bar{I}_D^2 = 4kT\Gamma gm + \frac{K_F'}{WLf^{AF}} \tag{3.37}$$

Depending on the absolute values of the noise currents and the location of the poles, the cut-off frequency can be evaluated.

Linearity will be improved due to the feedback. To ensure that enough swing is available, the saturation voltage of the transistors should be kept sufficiently low.

Sizing of the circuit elements is done with the derived equations plotted in figure 3.29 on an IC-ID graph. The bandwidth and compression determine the optimal working point.

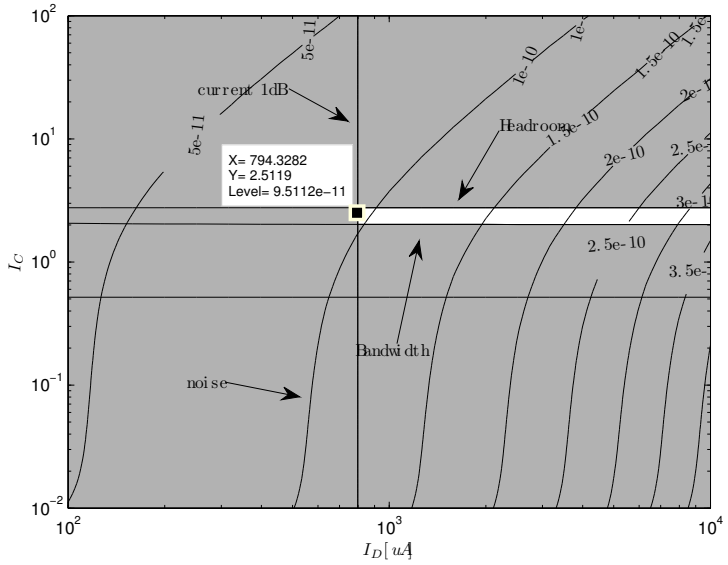


Figure 3.29: IC - ID graph with design constraints for the mixer TIAs.

Layout

The layout of the complete mixer is shown in figure 3.30. Special care was taken to ensure symmetry in the signal path to reduce I/Q phase and amplitude mismatch.

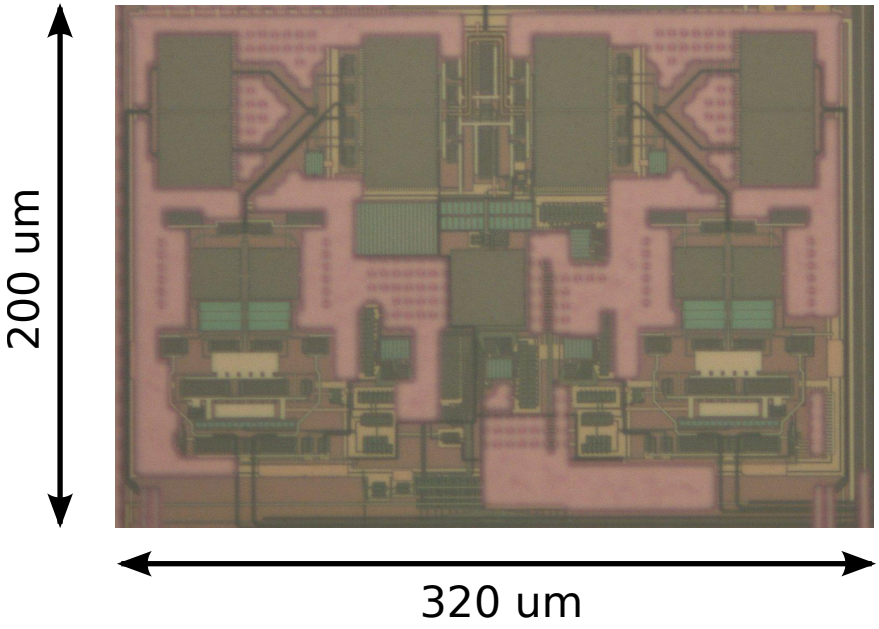


Figure 3.30: Micrograph of the mixer.

Conclusion

The mixer comprises a transconductor, a passive switching matrix and a TIA load. The different subblocks were designed in a systematic way, yielding a short design time. The complete mixer was laid out and simulated with extracted parasitics. The resulting gain is $12\ \mathrm{dB}$ with a noise figure of $6\ \mathrm{dB}$, realizing the specifications of table 3.1. The total current consumption of the I/Q mixer is $6.5\ \mathrm{mA}$.

3.4.5 Measurements

After characterizing the LNA, the LNA-mixer combination can be measured. After subtracting the LNA characteristics, the performance of the mixer is known. The procedures and results are described below.

Power consumption

In figure 3.31, a comparison between the simulated and measured current is shown. Increasing current push the current sourcing transistor of the mixers transconductance more towards its linear region, yielding greater matching errors and deviation from the simulated curve.

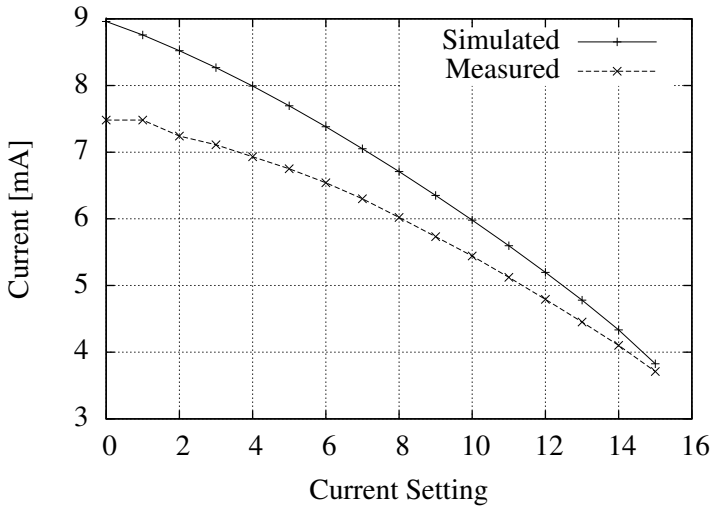


Figure 3.31: Current consumption Mixer.

Gain - Bandwidth

The gain and bandwidth of the mixer have been measured with a spectrum analyser. The gain is shown as function of the IF bandwidth in figure 3.32. The measured bandwidth is sufficient for the ranging application.

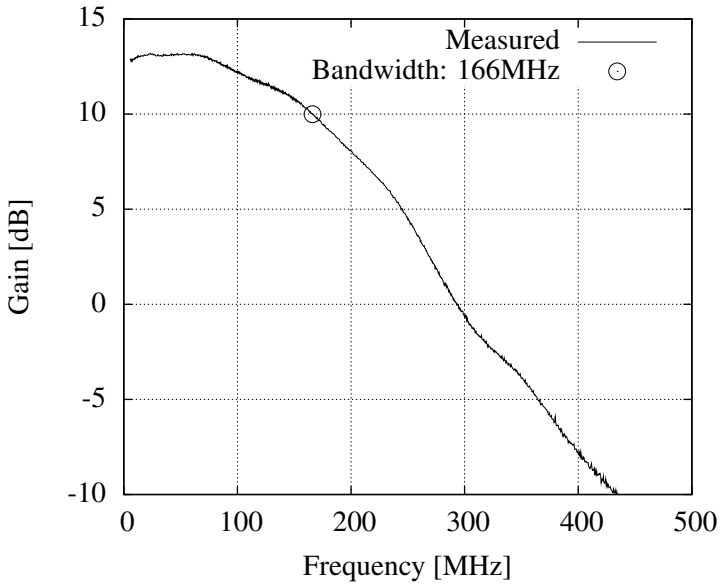


Figure 3.32: Mixer Gain and Bandwidth.

LO amplitude sensitivity

The amplitude of the LO signal has a strong impact on the conversion gain of the mixer. Since a low power LO driver stage demands minimum signal amplitude, the DC LO value should be set so maximum on/off resistance of the switches is ensured. The DC component of the signal can be varied to ensure optimum performance. The parameter which controls the DC value of the LO signal is swept and the resulting gain is normalized and shown in figure 3.33.

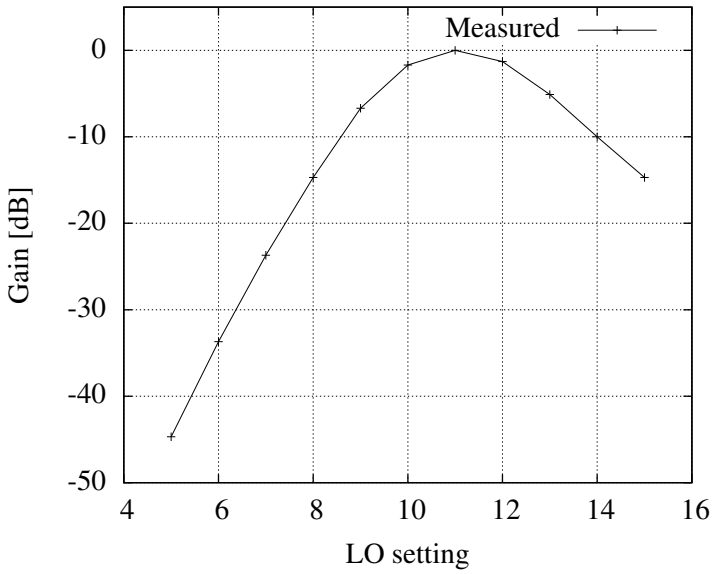


Figure 3.33: Mixer LO - Gain.

Noise figure

The receiver noise figure is measured using a known noise source. The total noise figure of the receiver is expressed in dB. Since the noise figure and gain of the LNA are known, the noise figure of the mixer can be calculated

back using Friis formula:

$$F_{tot} = F_{LNA} + \frac{F_{MIXER} - 1}{G_{LNA}} \tag{3.38}$$

$$F_{MIXER} = G_{LNA}(F_{tot} - F_{LNA}) + 1 \tag{3.39}$$

$$NF_{MIXER} = 10 \log \frac{F_{MIXER}}{10} \tag{3.40}$$

The high input loss of the LNA dominates the total noise figure and the noise figure of the mixer can not be measured. However the gain and current figures correspond well to the simulated ones, so, no important discrepancies are expected.

Linearity

The linearity of the mixer is verified by applying a 2 tone signal. The power of the resulting first and third order intermodulation terms are shown in figure 3.34. The input IIP3 point is found to be around -8 dBm, comparable with the specifications of table 3.1.

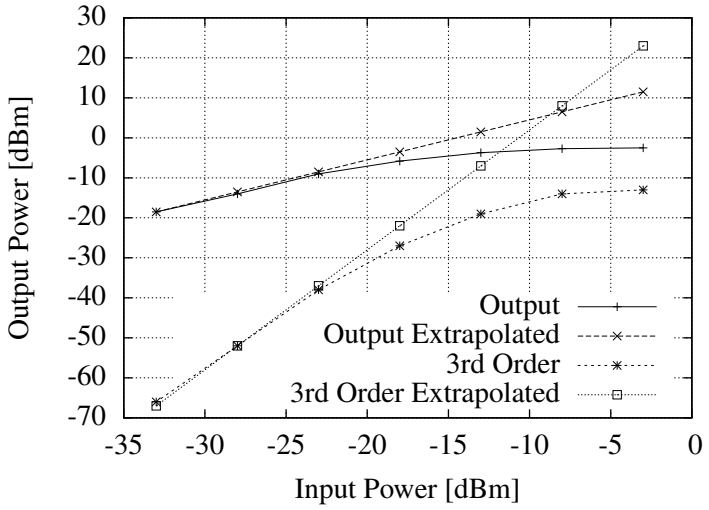


Figure 3.34: Mixer Linearity.

3.5 Integrated receiver

Notwithstanding that the measurements were impacted by additional parasitics, they provide a proof-of-concept of the receiver design, the architecture and the circuit techniques used.

By careful analysis, extensive use of the test modes and a FIB operation, it was possible to pinpoint improvements on the layout.

- The present power amplifier is AC coupled to the output, so we no longer need AC coupling to the LNA. Since it is shown that extra resistance at the input has a dramatic effect on the overall performance, the input capactors of the LNA were omitted.

- The conversion gain of the mixer is very sensitive towards the DC voltage of the LO signal. This sensitivity can be reduced by increasing the LO power and/or reducing the threshold voltage of the switches.

Making use of these insights, some design optimizations were performed and new silicon was produced. The improved measurement results are described below:

3.5.1 Input Matching

The input DC-blocking capacitors were removed from the original design. The resulting input resistance is shown in figure 3.35. It is clear that a much better matching is achieved ($S_{11} < -20$ over the ISM band).

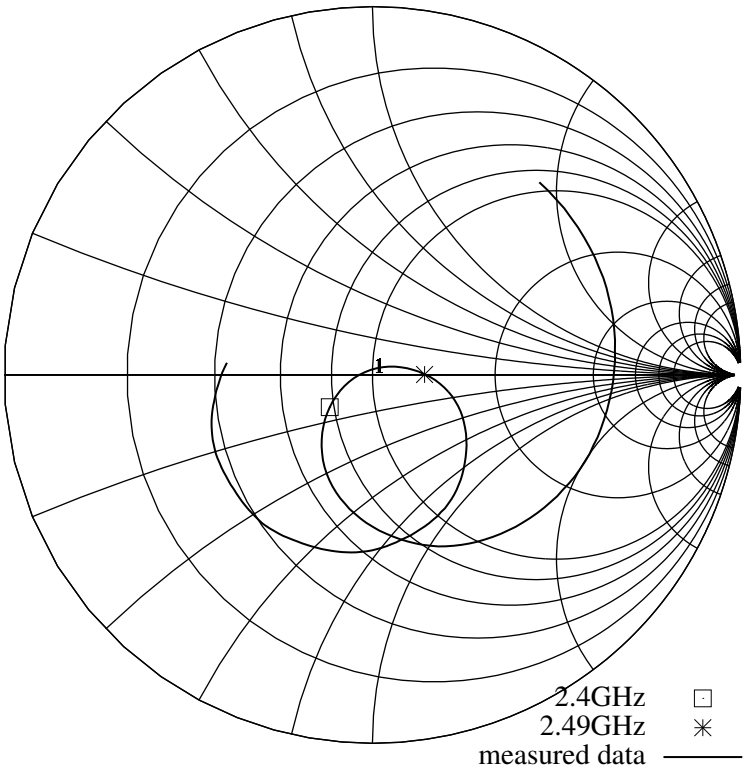


Figure 3.35: LNA input reflection coefficient.

3.5.2 Gain

As a result of better input matching, the gain of the receiver improved substantially. The sensitivity towards LO DC-amplitude was removed in the new design by biasing the gates of the LO switches a threshold voltage above the common mode input voltage of the TIAs. This threshold voltage is generated via a diode connected MOSFET. The measured combined gain of LNA and mixer is shown in figure 3.36. During these measurements the total current consumption of the receiver was $10\ \mathrm{mA}$ from a $1.2\ \mathrm{V}$ supply.

Looking at figure 3.36, an RF bandwidth of $260\ \mathrm{MHz}$ and a gain of $26\ \mathrm{dB}$ can be marked out. A result sufficient for the application but a little less than simulated ($29\ \mathrm{dB}$).

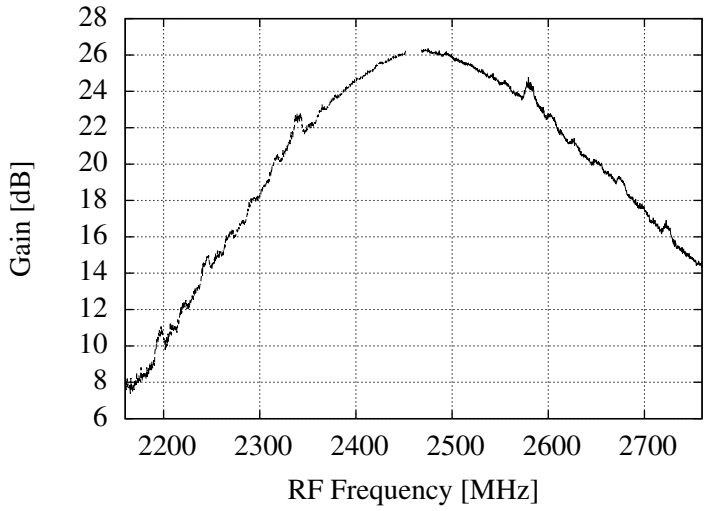


Figure 3.36: Receiver's Gain.

3.5.3 Noise

The single side band noise performance of the receiver is depicted in figure 3.37. A minimum noise figure of $7.5\ \mathrm{dB}$ was measured, $1.5\ \mathrm{dB}$ higher than simulated. The figure clearly shows the passband characteristic of the LNA and mixer since the noise measurements were performed at baseband after downmixing. As expected, the noise rises at with increasing frequency due to increased attenuation.

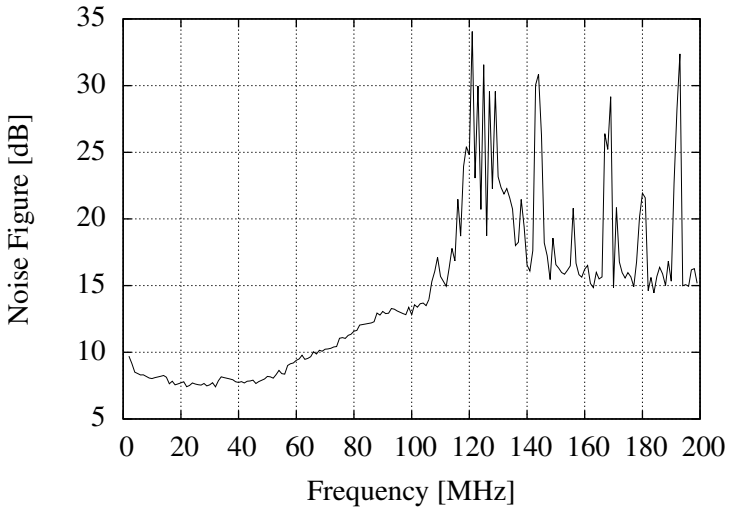


Figure 3.37: Receiver Noise Figure.

3.5.4 Linearity

The linearity in terms of IIP3 is shown in figure 3.38. The measurements are performed by appling a closely spaced two-tone signal. The total input power of the two tone signal is shown on the x-axes, the power of one 1st order term and one 3rd order signal is shown on the y-axes. An IIP3 point of $-12\ \mathrm{dBm}$ is measured at a gain of $26\ \mathrm{dB}$, which is comparable to the specifications of table 3.1.

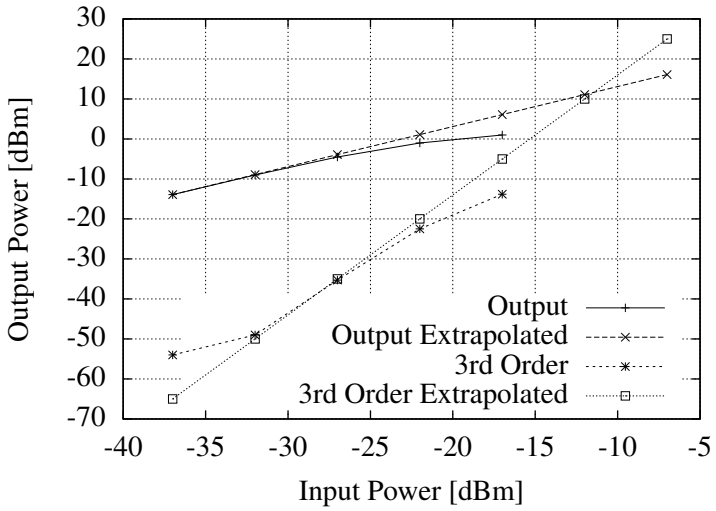


Figure 3.38: Receiver linearity measurement.

3.6 Conclusion

This chapter described the realization of a broadband, low noise, low power ranging receiver front-end. Two structural design procedures were described, resulting in a short implementation cycle of both LNA and mixer.

The LNA is co-designed with the on-chip PA. The output of the PA is reused in the matching network avoiding bulky inductors from the design. The switching nature of the PA made it possible to simplify a traditional transmit/receive switch to a simple pass gate in front of the LNA, achieving maximum integration.

The mixer design uses a TIA as load. This TIA reduces the voltage swing on the internal nodes and, hence, reduces the effect of non-linear output resistances and, thus, reduces the total distortion.

Via careful inspection of layout, and comparison of simulation and measurements, an inaccuracy in the models of the finger capacitors was found. After a second tape-out the discrepancies between the simulated and measured results were solved and the target specifications were met.

References

[1] T. Song, H.-S. Oh, S. Hong, and E. Yoon. A 2.4-GHz sub-mW CMOS receiver front-end for wireless sensors network. *IEEE Microwave and Wireless Components Letters*, 16(4):206 – 208, April 2006.

[2] J.-S. Syu, C. Meng, C.-Y. Lin, S.-C. Wong, G.-W. Huang, and W.-T. Liu. 2.4-GHz 8.5mW 3.7-dB NF 100-kHz 1/f corner direct-conversion receiver using double-balanced passive mixer. In *IEEE MTT-S International Microwave Symposium Digest*, pages 1 –4, June 2011.

[3] J. Wu, P. Jiang, D. Chen, and J. Zhou. A Dual-Band GNSS RF Front End With a Pseudo-Differential LNA. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58(3):134 –138, March 2011.

[4] K.S. Kumari and B. Bhuvan. Compact WiMAX Low Noise Amplifier Using Active Inductor. In *International Conference on Devices and Communications*, pages 1 –5, Feb. 2011.

[5] R. Fiorelli, A. Villegas, E. Peralias, D. Vazquez, and A. Rueda. 2.4-GHz single-ended input low-power low-voltage active front-end for ZigBee applications in 90 nm CMOS. In *20th European Conference on Circuit Theory and Design*, pages 829 –832, Aug. 2011.

[6] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello. A 0.13 μm CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback low noise amplifier. In *Symposium on VLSI Circuits. Digest of Technical Papers*, pages 406 – 409, June 2005.

[7] J.A.M. Jarvinen, J. Kaukovuori, J. Ryynanen, J. Jussila, K. Kivekas, and K.A.I. Halonen. 2.4-GHz receiver for sensor applications. In *Proceeding of the 30th European Solid-State Circuits Conference*, pages 91 – 94, Sept. 2004.

[8] T. H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*, volume 22. Cambridge University Press, 2004.

[9] Z. Li, G. Torfs, J. Bauwelinck, X. Yin, J. Vandewege, C. Van Praet, P. Spiessens, H. Tubbax, and F. Stubbe. A 2.45-GHz + 20-dBm Fast Switching Class-E Power Amplifier With 43% PAE and a 18-dB-Wide Power Range in 0.18- μm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, PP(99):1 –5, 2012.

[10] J.A. Garcia, E. Malaver, and L. Cabria. A zero-bias single-device balanced E-PHEMT mixer with conversion gain for RFID applications. In *IEEE MTT-S International Microwave Symposium Digest*, volume 2, pages 1311 – 1314 vol.2, June 2003.

[11] K. Yhland, N. Rorsman, and H. Zirath. A novel single device balanced resistive HEMT mixer. In *IEEE MTT-S International Microwave Symposium Digest*, pages 1411 –1414 vol.3, May 1995.

[12] E. Chan. Design of a 5-6 GHz single balanced Schottky diode mixer. In *Asia-Pacific Conference on Applied Electromagnetics*, pages 67 – 71, Aug. 2003.

[13] A. Maalik and Z. Mahmood. A Novel C-Band Single Diode Mixer with Ultra High LO/RF and LO/IF Isolation. In *International Conference on Electrical Engineering*, pages 1 –6, April 2007.

[14] C.-H. Lin, H.-Z. Liu, C.-K. Chu, H.-K. Huang, C.-C. Liu, C.-H. Chang, C.-L. Wu, C.-S. Chang, and Y.-H. Wang. A Ku/K-band PHEMT Diode Single-balanced Mixer. In *8th International Conference on Solid-State and Integrated Circuit Technology*, pages 884 – 886, Oct. 2006.

[15] X. Fan and E. Sanchez-Sinencio. 3-22GHz CMOS distributed single-balanced mixer. In *IEEE International SOC Conference. Proceedings*, pages 93 – 96, Sept. 2004.

[16] A. Helmy, K. Sharaf, A. Mhani, and H. Ragai. A low voltage single-balanced down-conversion transformer coupled mixer. In *IEEE 46th Midwest Symposium on Circuits and Systems*, volume 3, pages 1243 – 1246 Vol. 3, Dec. 2003.

[17] V. Vidojkovic, J. van der Tang, A. Leeuwenburgh, and A. van Roermund. Low voltage, low power folded-switching mixer with current-reuse in 0.18 μm CMOS. In *Proceedings of the 2004 International Symposium on Circuits and Systems*, volume 1, pages I – 569–72 Vol.1, May 2004.

[18] Z. Cheng, P. Zhou, J. Li, and S. Zhang. An Improved Current Bleeding Mixer Based on CMOS Technology. In *International Conference on Communications and Mobile Computing*, volume 3, pages 128 –131, April 2010.

[19] Z. Pan, P. Jiang, L. Zhang, and C. Mao. Low flicker noise and high linearity passive mixer in 0.18 μm CMOS for direct conversion receiver. In *Asia Pacific Conference on Postgraduate Research in Microelectronics Electronics*, pages 21 –24, Jan. 2009.

[20] D. M. Binkley. *Tradeoffs and Optimizations in Analog CMOS design*. Wiley & Sons, June 2008.

4 Baseband section

4.1 Introduction

In chapter 3, the RF front-end of a ranging transceiver was described. This front-end allows the reception of the broadband ranging signal and converts it to baseband with a zero-IF architecture. For distance measurements, this signal needs to be digitized to allow further digital signal processing. The typical approach is to use a high-speed ADC. Section 4.3 describes a state-of-the-art 4 bit flash ADC which was especially optimized for this application (high bandwidth, low SNR, low power). To maximize the performance of the ADC, proper signal conditioning is required. Signal components above the Nyquist frequency (which is half the sampling rate) need to be filtered out, since these would lead to aliasing. To accomplish this signal conditioning section 4.2 describes a novel, low-power steep baseband filter with programmable bandwidth.

4.2 Baseband Filter

4.2.1 Specifications

The RF front-end amplifies and down-converts the incoming RF signal. The specifications of the ranging system demand a high bandwidth around the 2.45 GHz ISM band, but close to this band other (undesired) signals,

such as UMTS carriers, tend to interfere with the ranging signal. To remove the interfering signals from the ranging signal a 125 MHz low pass filter is required with a suppression of 35 dB at 225 MHz[1]. To increase the link budget when the transceiver is in (narrowband) communication mode, thus when it is not sending ranging signals, a parallel filter with 20 MHz bandwidth is provided.

4.2.2 Topologies

A number of different active filter topologies exist. Figure 4.1 gives an overview of the realizable bandwidth and signal to noise and distortion ratio in a standard CMOS technology.

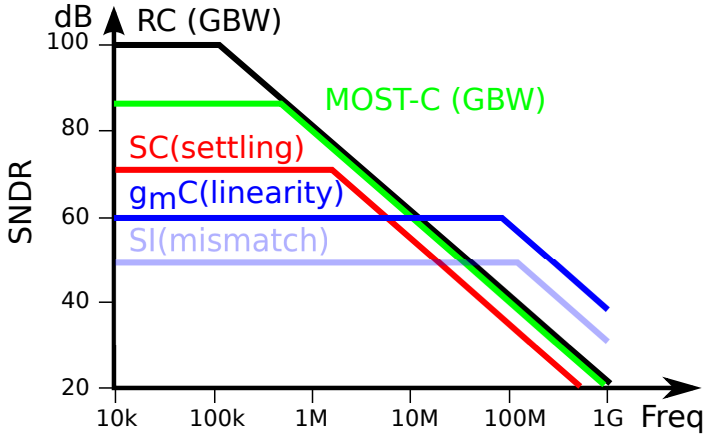


Figure 4.1: Comparison of different filter topologies (and their limitations) [1].

1. RC: This configuration is based on operational amplifiers with a resistive-capacitive feedback network. Very high signal to noise and distortion ratios can be realised at the lower frequencies due to the high loop gain. At higher frequencies the loop gain degrades as will the dynamic range. The filter is very difficult to tune due to the fixed resistors. It can be fine tuned discretely by using tunable resistor banks. The power consumption of the needed opamps is high. Realizations can be found in [2, 3].

[1] 35 dB suppression is needed to remove UMTS transmitters located in the proximity of the ranging receiver

2. MOST-C: To make the RC filter more flexible, the resistors can be replaced by Metal-Oxide-Semiconductor (MOS) transistors working in their linear region. The maximum signal to noise and distortion ratio will be lower due to non-linearities of MOS resistors. In [4] a realization is discussed.

3. SC: Switched capacitor filters are easily tuned, but have a low dynamic range due to clock injection and charge redistribution. At high frequencies this is even worse due to the short settling time constraints since the switching speed should be an order of magnitude higher than the signal's bandwidth. Examples can be found in [5, 6].

4. gmC: By using combinations of transconductor stages loaded with a capacitor, different filter topologies can be realized. These filter topologies rarely have a dynamic range larger than $60\ \mathrm{dB}$ due to the distortion generated by the transconductor stage. They can on the other hand offer a very high bandwidth, thanks to the simplicity of the building blocks. In [7, 8] some realizations are shown.

5. SI: Switched current filters nearly offer the same speed as gmC, but are limited by the mismatch of the current sources and clock injection. Some possible implementations are shown in [9, 10].

As a very high frequency response with a maximum dynamic range should be realized, different gmC filter topologies were studied.

Standard gmC topology

Filters with the highest dynamic range are realized with opamps, because the high open loop gain at low frequencies linearises the circuit. However, at higher frequencies, the loop gain degrades and the dynamic range of the filter reduces. To operate at higher frequencies, the complex opamps used in RC and switched capacitor filters are reduced to their bare essence: a transconductor, which is no more than a linearised differential pair. To cancel out even order harmonics a differential implementation is preferred.

Linearised Transconductors The easiest differential transconductor is a differential pair (figure 4.2). Its transconductance (g_m), noise ($v_{n,rms}$) and compression ($V_{INDIF1dB}$) in function of the inversion coefficient (IC

[11]), the drain current (I_D) and the technology parameters[2] are given by:

$$g_m = \frac{1 - e^{-\sqrt{IC}}}{nU_T\sqrt{IC}} I_D \tag{4.1}$$

$$v_{n,rms} = \sqrt{\frac{4kT \cdot n\Gamma}{g_m}} \tag{4.2}$$

$$V_{INDIF1dB} \approx 1.81 \cdot nU_T\sqrt{IC} \tag{4.3}$$

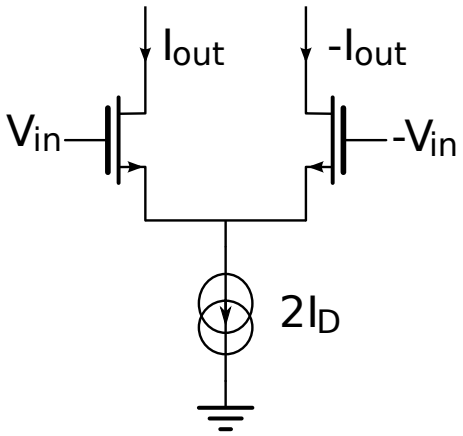


Figure 4.2: Differential pair as transconductor.

To increase the signal to noise and distortion ratio, feedback techniques can be applied:

- Source degeneration: Figure 4.3 shows a differential pair with source degeneration. The transconductance is degraded with a factor m. The distortion decreases linearly with R while the signal to noise ratio only decreases with the square-root of R. The resulting transconductance, noise and distortion are shown in equations (4.4)–(4.8). The

[2] Different technology constants:
U_T: thermal voltage; kT/q
n: substrate factor
Γ: Thermal-noise factor relative to g_m for operation in saturation
k: Boltzmann's constant; 1.3806 x 10^{-23} J/K
T: absolute temperature
q: elementary charge; 1.6022 x 10^{-19} C

equations reuse the results of equations (4.1)–(4.3) to ease comparison.

$$
\begin{aligned}
m &= 1 + R \cdot g_m && (4.4)\\
g_{m(eff)} &= \frac{g_m}{m} && (4.5)\\
v_{n,rms(eff)} &= \sqrt{4kT \cdot \left(\frac{n\Gamma}{g_m} + R\right)} && (4.6)\\
V_{INDIF1dB(eff)} &\approx m \cdot V_{INDIF1dB} && (4.7)\\
&\approx 1.81 \cdot R \cdot I_D + V_{INDIF1dB} && (4.8)
\end{aligned}
$$

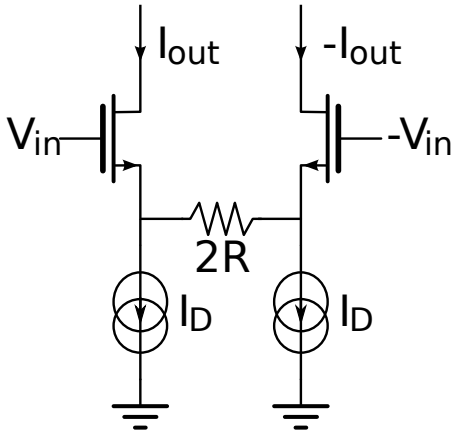


Figure 4.3: Differential pair with resistive source degradation.

- Gain boosting: by adding an amplifier (with gain A) around the transconductor (figure 4.4), the distortion and noise at lower frequencies can be reduced. Nevertheless, the resulting opamp will cost power. The resulting figures can be seen in equations (4.9)–(4.12).

$$m = \frac{1+(A+1)\cdot R\cdot g_m}{A} \tag{4.9}$$

$$g_{m(eff)} = \frac{g_m}{m} \xrightarrow{\lim} \frac{1}{R} \tag{4.10}$$

$$v_{n,rms(eff)} = \frac{1}{A\cdot m}\sqrt{4kT\cdot\left(\frac{n\Gamma}{g_m}+R\right)} \tag{4.11}$$

$$V_{INDIF1dB(eff)} \approx m\cdot V_{INDIF1dB} \tag{4.12}$$

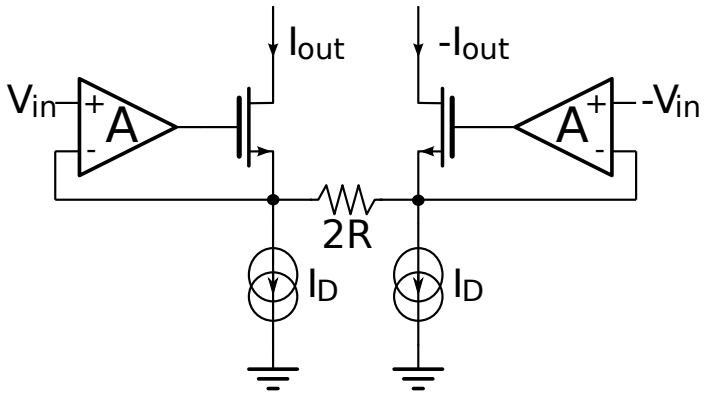


Figure 4.4: Differential pair with gain boosting.

Generic biquad stages By combining gm stages and capacitors a generic biquad (a polynomial with a second order nominator and denominator) stage can be formed. An example of such a biquad stage is shown in figure 4.5 with transfer-function given in equation (4.13). With a cascade of such stages any filter can be synthesized [12].

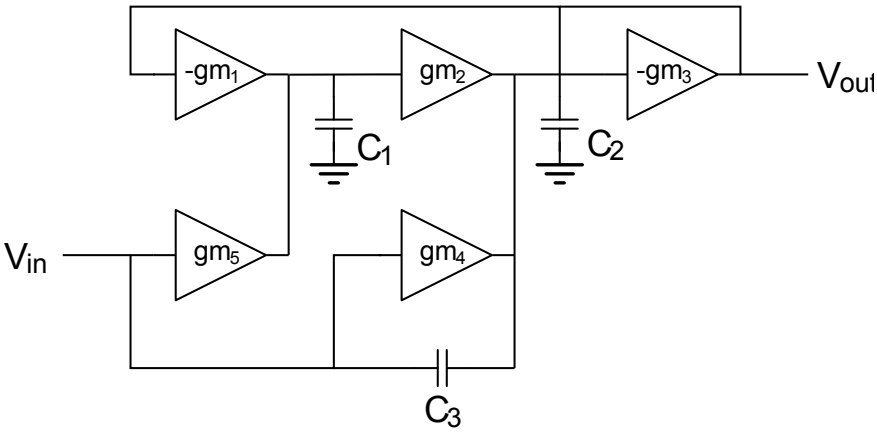


Figure 4.5: Generic Biquad stage.

$$V_{out} = K\frac{s^2 + a_1 \cdot s + a_0}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}V_{in} \tag{4.13}$$

$$K = \frac{C_3}{C_2 + C_3} \tag{4.14}$$

$$a_0 = \frac{gm_2 gm_5}{C_1 C_3} \tag{4.15}$$

$$a_1 = \frac{gm_4}{C_3} \tag{4.16}$$

$$\omega_0 = \sqrt{\frac{gm_1 gm_2}{C_1(C_2 + C_3)}} \tag{4.17}$$

$$Q = \sqrt{\frac{C_2 + C_3)}{C_1}}\frac{\sqrt{gm_1 gm_2}}{gm_3} \tag{4.18}$$

Source-Follower based filter

To linearise a differential pair, feedback needs to be applied. The linearisation techniques discussed above all degrade the noise and/or power performance of the original differential pair. To overcome this problem a source-follower (figure 4.6) configuration can be used. The transfer function of a source follower can be written as:

$$H(s) = \frac{1}{1 + \frac{g_{ds}+sC}{g_m}} \tag{4.19}$$

The transfer function can be rewritten to resemble the transfer function of a simple feedback system (eq. (4.20)). And as with every feedback system, its linearity increases with its open loop gain (eq. (4.21)). The linearity will increase with g_m and looking at eq. (4.22), one can see that the noise is inversely proportional with the square root of g_m. As a consequence, increasing g_m will both increase the linearity and reduce the noise floor.

$$H(s) = \frac{g_m}{sC + g_{ds}} \cdot \frac{1}{1 + \frac{g_m}{sC+g_{ds}}} \tag{4.20}$$

$$K = \frac{g_m}{sC + g_{ds}} \tag{4.21}$$

$$v_{n,rms} = \sqrt{\frac{kT \cdot n\Gamma}{g_m}} \tag{4.22}$$

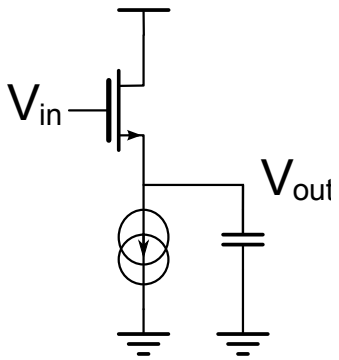


Figure 4.6: Source-Follower with capacitive load.

A source-follower can be used as a first order filter stage. To synthesize more complex filters, the source follower can be combined with a cross

coupled source follower as proposed in [13] and shown in figure 4.7. The filter is implemented differentially. The input transistors M_1 and M_2 act like normal source followers. Transistors M_3 and M_4 are a second set of source followers, following the crossed output of the input transistors. The transfer function of the filter cell is giving by eq. (4.23). The filter stage offers a high input and low output impedance which allows to cascade them to form complex all pole filters, in contrast with [14, 15].

$$H(s) = \frac{1}{s^2 \cdot \frac{C_1 C_2}{gm^2} + s \cdot \frac{C_1}{gm} + 1} \tag{4.23}$$

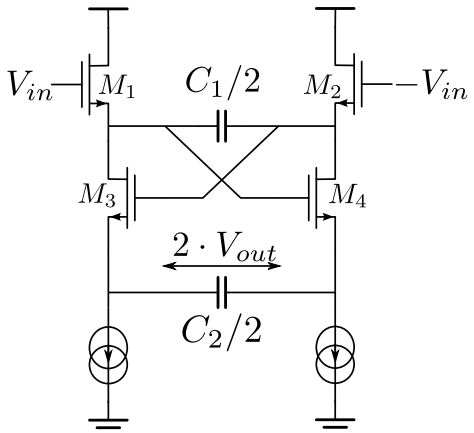


Figure 4.7: Source-Follower based filter.

The filter branch consists of 3 stacked transistors (M_1, M_3 and the current source). Assuming the common mode of the previous stage equals $V_{dd} - V_{sat}$ (where $V_{sat} = V_{GS} - V_{th}$), the maximum signal swing is given by:

$$\begin{aligned} V_{swing} &= V_{dd} - V_{sat} - V_{GS1} - V_{GS3} - V_{sat} && (4.24) \\ &= V_{dd} - 4 \cdot V_{sat} - 2 \cdot V_{th} && (4.25) \end{aligned}$$

For the $0.13\ \mu\mathrm{m}$ technology used for the RF front end, the typical 1.2 V supply voltage is insufficient to allow enough swing. When the filter architecture is folded [13] as shown in figure 4.8, the voltage swing can be increased.

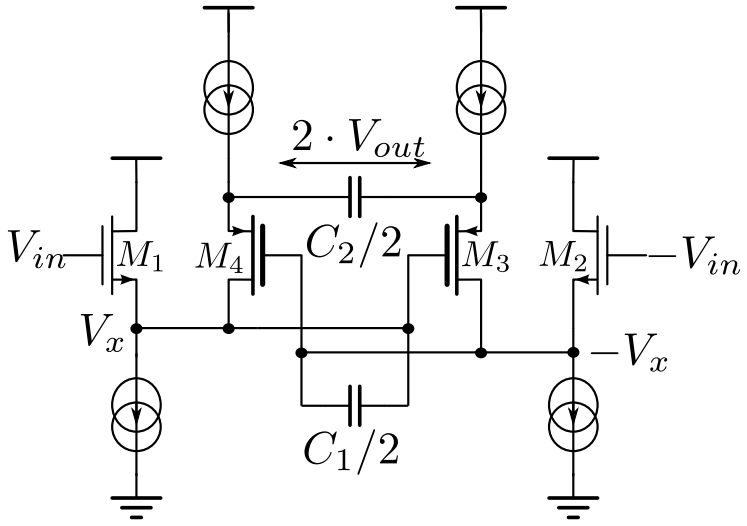


Figure 4.8: Folded Source-Follower based filter.

This will increase the maximum voltage swing to:

$$\begin{aligned} V_{swing} &= V_{dd} - V_{sat} - V_{GS1} - V_{sat} && (4.26)\\ &= V_{dd} - V_{sat} - V_{GS3} - V_{sat} && (4.27)\\ &= V_{dd} - 3 \cdot V_{sat} - V_{th} && (4.28) \end{aligned}$$

So, we gain $V_{sat} + V_{th}$. In a $0.13\ \mu\mathrm{m}$ technology, this will allow a differential peak-to-peak voltage swing of $800\ \mathrm{mV}$. The folded structure offers a second advantage: the output common mode voltage can be kept more or less equal to the input common mode voltage since the signal first undergoes a drop by V_{GS1} and then rises again by V_{GS3}. The linearity of the structure degrades when transistors M_3 and M_4 enter their linear region. This happens when the single ended signal swing exceeds the threshold voltage V_{th}.

Source-Follower based filter with extended linear range

The linear range of the structure is limited by the cross-coupling. Figure 4.9 shows our new solution to change the feedback structure. Instead of using transistors M_3 and M_4 to directly draw current out of C_1, the current is copied via the current mirror M_5 – M_7 and M_6 – M_8 respectively. In this way the biasing scheme is simplified since the current for M_1 and

M_2 is provided through the newly added current mirrors. Additionally, the cross-coupling used in figure 4.8 can be removed while keeping the current flowing through C_1 equal to $gm \cdot (V_{in} - V_{out})$, with gm equal to the transistors conductance. Hence, it becomes possible to use the filter in a single-ended configuration.

The small-signal linearity of the proposed filter architecture remains the same as the one of [13]. The non-linearity introduced by the current mirrors can be kept sufficiently small by increasing the length of the transistors and thus reducing the influence of channel length modulation to a minimum. A source-follower inherently shows high linearity because of the voltage feedback formed by $gm \cdot V_{GS}$, with V_{GS} equal to the transistors gate-source voltage. Again the effect of channel length modulation can be minimized by increasing the length of the transistors.

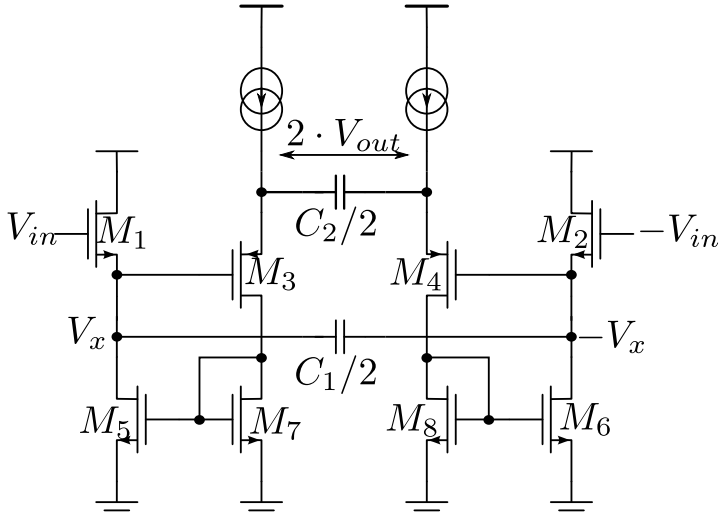


Figure 4.9: Folded Source-Follower based filter with extended linear range.

The main difference, though, occurs when considering large input signals. For in-band signals, M_1 and M_3 act as source followers. Transistor M_3 of figure 4.8 will enter the cut-off region due to the inverse relation of its drain and gate voltage, as depicted in figure 4.10. Removing the cross-coupling and adding a low impedance connection to the drain of M_3, as proposed in figure 4.9, ensures sufficient head-room over the transistor (see fig. 4.11). The proposed solution clearly eliminates the cut-off problem and guarantees linearity for larger input signals.

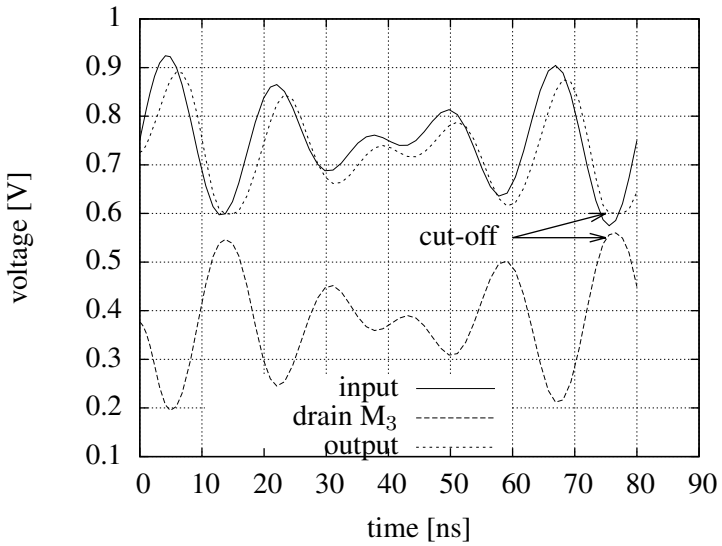


Figure 4.10: Waveforms of the circuit in figure 4.8.

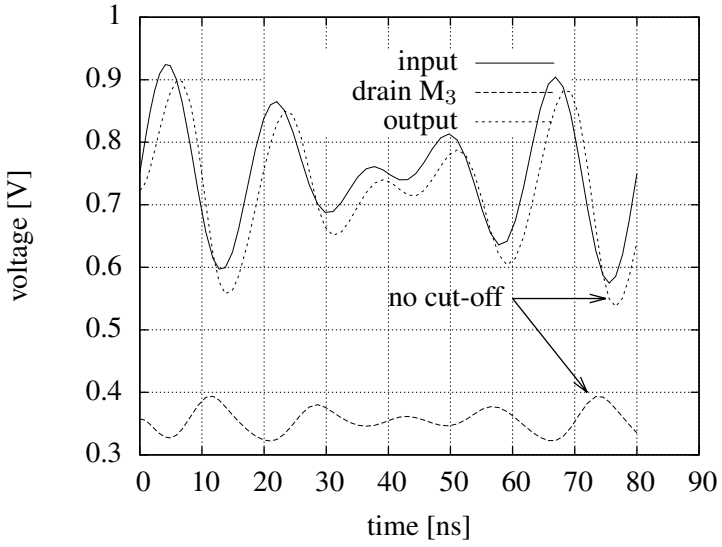


Figure 4.11: Waveforms of the circuit in figure 4.9.

Both the original source-follower based filter as described in [13] and the proposed filter have been implemented and simulated in the same $0.13\ \mu\mathrm{m}$ CMOS technology with a $1.2\ \mathrm{V}$ supply, thus allowing for performance comparison. Two $125\ \mathrm{MHz}$ filter stages, each consuming $40\ \mu\mathrm{A}$, were designed according to the architectures of figure 4.8 and figure 4.9 respectively. To allow for a fair comparison between both designs, the transistors have been sized and biased equally. A two tone input signal consisting of $50\ \mathrm{MHz}$ and $50.5\ \mathrm{MHz}$ has been applied and the deviation from the ideal linear and third order characteristic have been evaluated for different signal levels (see fig. 4.12 and 4.13). The curve at figure 4.12 reveals that the resulting 1-dB compression point is extended. Figure 4.13 shows that, in the proposed architecture, the point where strong non-linear effects occur and where the third order intermodulation starts deviating from its ideal characteristic is shifted to higher input powers. D'Amico's implementation [13] starts to show degradation when the output transistors reach cut off. The proposed circuit degrades more slowly up to the point where the current sources driving M_3 and M_4 are forced in to their linear region. As they provide the bias current for the output transistors as well as for the input transistors (through current mirrors M_5–M_7 and M_6–M_8), the current through the input transistors will be cut-off altogether. This happens when the (peak to peak) differential signal amplitude reaches $1.4\ \mathrm{V}$, extending the linear input range with 5dB (see fig. 4.12). This source follower based filter with extended dynamic range is published in [16].

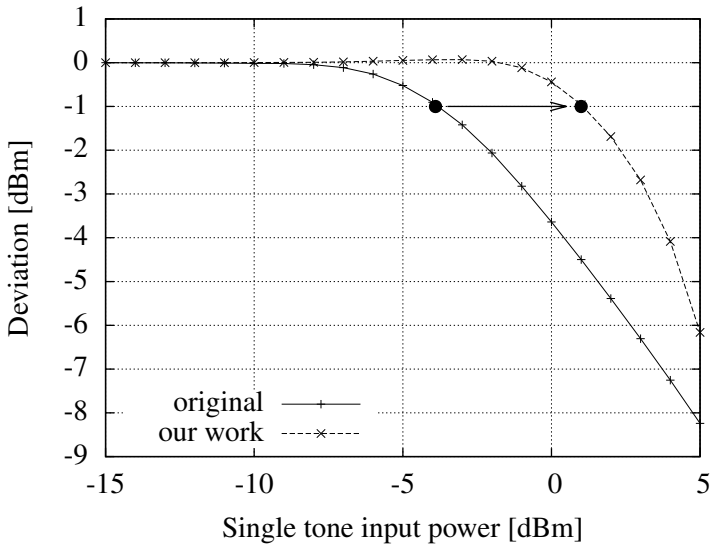


Figure 4.12: Deviation of the linear characteristic.

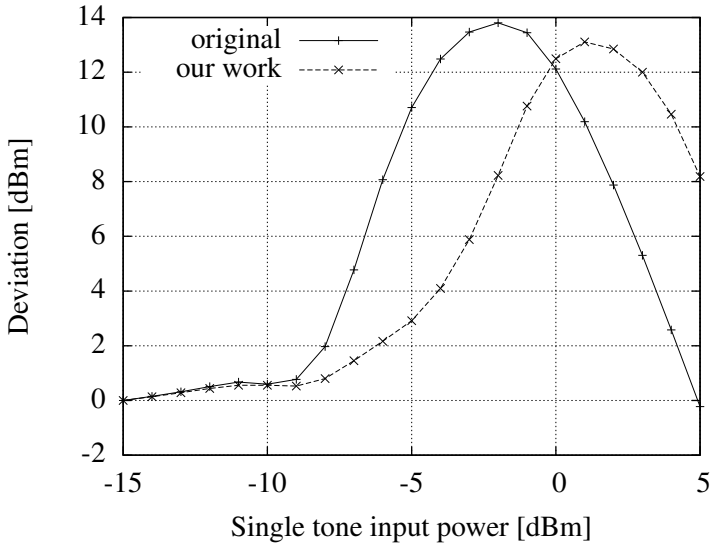


Figure 4.13: Deviation of the third order characteristic.

Source follower based filter with Gain

In CMOS processes where there is no triple well available, it is not possible to isolate the NMOS transistors from the substrate. As a consequence, the bulk effect will limit the gain of a source follower to typically 0.7. This problem can be overcome with the circuit proposed in figure 4.14. By matching the transconductance of M_3 and M_4 to the body transconductance of M_1 and M_2 the body effect can be canceled. By increasing the transconductance even further, some gain can be introduced in the filter and higher Q factors can be realized.

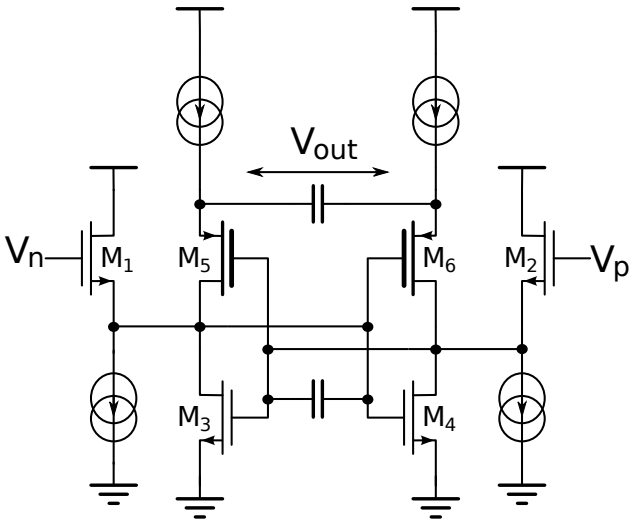


Figure 4.14: Source follower based filter with gain.

4.2.3 Implementation

The filter section shown in figure 4.14 has been used in a 125 MHz 10th order baseband filter. The resulting micrograph is shown in figure 4.15.

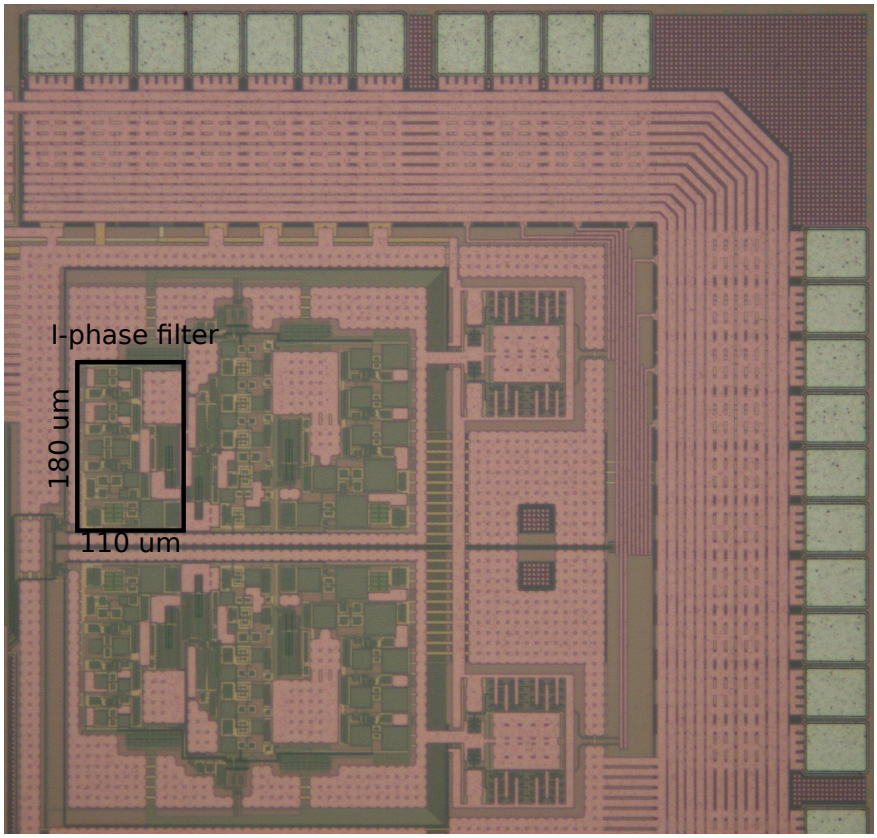


Figure 4.15: Micrograph of the I/Q baseband filter.

4.2.4 Measurements

The measured filter frequency response, obtained after tuning the input common mode voltage, is shown in figures 4.16 and 4.17. The resulting attenuation at $225\ \mathrm{MHz}$ is $35\ \mathrm{dB}$ which was the goal for the suppression of nearby UMTS transmitters. The linearity is evaluated in terms of the IIP3 and results in $17.9\ \mathrm{dBm}$. Some third order cancellation can be seen on Figure 4.17, where without cancellation the slope of HD3 should be 2, the cancellation mechanism eliminates the output 3rd order intermodulation (IM3) at a specific input voltage, resulting in a dip on the curve around $-23\ \mathrm{dBm}$ input power. The input referred noise is $187\ \mu\mathrm{V_{rms}}$. The filter consumes 2mW, supplied from a $1.2\ \mathrm{V}$ source. A commonly used Figure Of Merrit (FOM) used for comparison is defined as:

$$FOM = 10\log\frac{IMFDR_3 \cdot Bandwidth}{Power/pole} \tag{4.29}$$

$$IMFDR_3 = \left(\frac{IIP_3}{V_{noise}}\right)^{4/3} \tag{4.30}$$

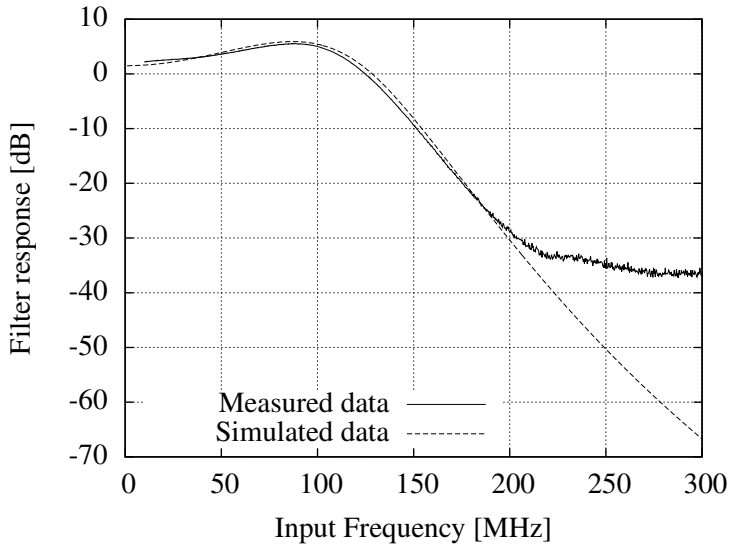


Figure 4.16: Frequency response of the implemented filters.

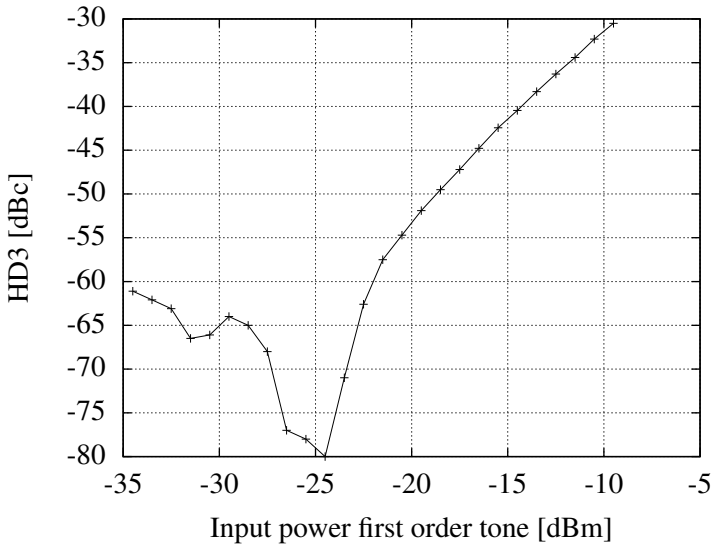


Figure 4.17: HD3 of the implemented filters.

The FOM of the filter with feedback around the input transistor is 173, which is comparable to the state of the art. A comparison with the state-of-the-art is given in table 4.1. Although [14] has a higher FOM, its linearity is lower, which is required by the application.

	This work	[13]	[14]
Bandwidth [MHz]	125	10	280
Power [mW]	2	4.1	0.12
Number of poles	10	4	6
Input noise [uVrms]	187	24	374
IIP3 [dBm]	17.9	17.5	11
FOM	173	164	176

Table 4.1: Filter comparison.

4.2.5 Integrated receiver

The designed filter is implemented together with the RF ranging front-end. The gain, linearity and noise of the complete receiver are measured. The total power consumption is $12\ \mathrm{mA}$ from a $1.2\ \mathrm{V}$ supply.

Gain

The overall receiver gain, measured from LNA input up to the outputs of the baseband filter, is shown in figure 4.18. The figure shows a gain of $28\ \mathrm{dB}$ at low frequencies, a $3\ \mathrm{dB}$ bandwidth of $130\ \mathrm{MHz}$ and, due to the gain peaking, $33\ \mathrm{dB}$ attenuation at $225\ \mathrm{MHz}$. Fulfilling the specifications of table 3.1.

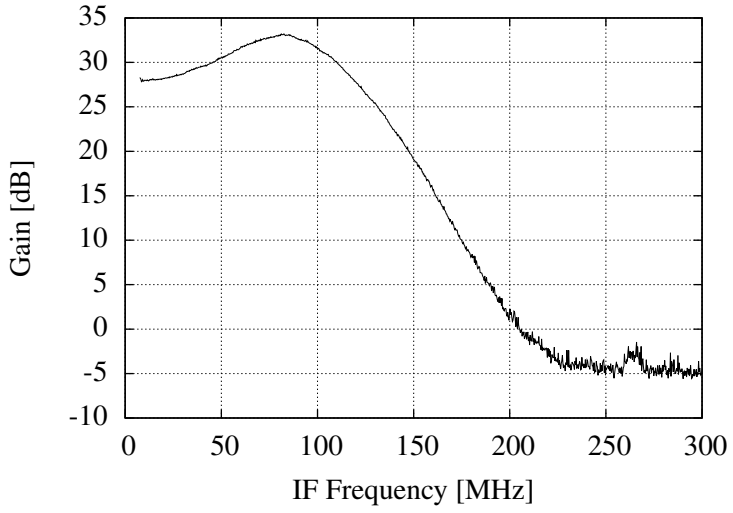


Figure 4.18: Total receiver's gain.

Noise

The receiver NF in function of frequency is shown in figure 4.19. The figure clearly shows the frequency characteristic of the filter and a minimum NF of 8 dB. Comparing with section 3.5.3 shows that the filter has only little influence (0.5 dB) on the total noise behaviour.

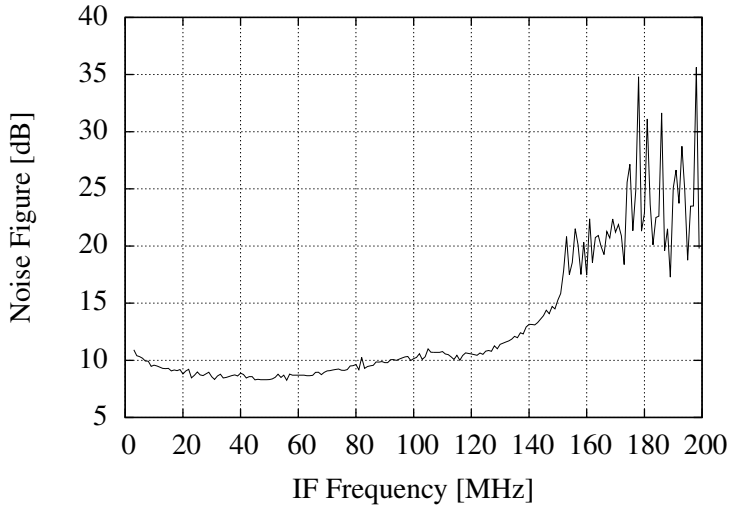


Figure 4.19: Total receiver NF as function of frequency.

Linearity

The overall receiver linearity is measured in terms of IIP3. Figure 4.20 shows the measured 1st and 3rd order intermodulation terms and the interpolation resulting in the linearity measurement. This measurement shows a -23 dB IIP3. By enabling the bypass mode of the LNA, this point can be extended to around 0 dB.

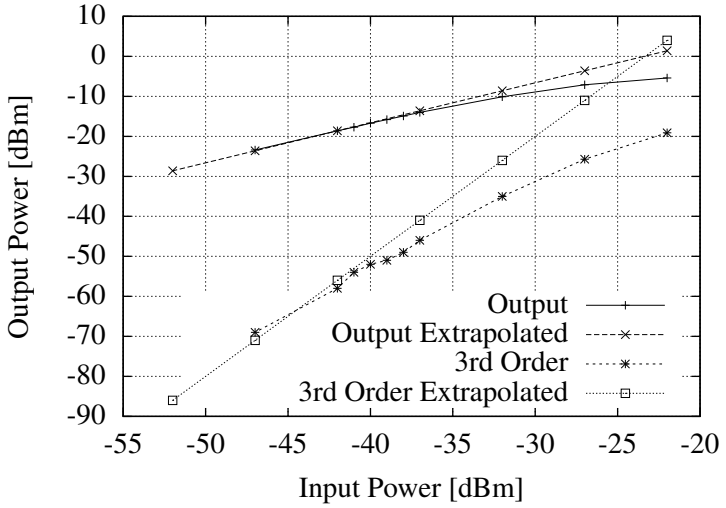


Figure 4.20: Receiver linearity.

4.3 Analog-to-Digital Converter

In most modern communication devices, the analog part serves as an interface towards the outside world, hence the term "analog front-end". The main functionality is implemented with digital logic since these building blocks gain the most out of CMOS scaling. To interface the analog signals to the digital part, typically an ADC is used.

As shown in chapter 2, an ADC is required with sampling rates up to $500\ \mathrm{MHz}$ but with only a limited resolution (4 bit). Typically such ADCs use a flash architecture. Figure 4.21 shows such a flash ADC converter. The input is compared to a reference ladder. This results in a thermometer code which can be converted to binary codes.

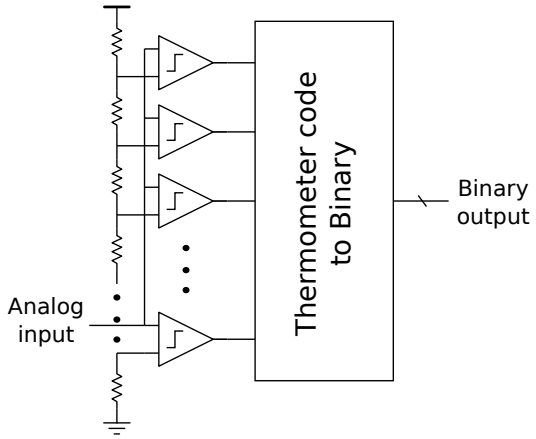


Figure 4.21: Flash ADC Architecture.

To reduce the power consumption, [17] proposes a comparator with an integrated threshold. This novel circuit designed and provided to us by IMEC is shown in figure 4.22. This circuit omits the use of a reference ladder and reduces the static power dissipation, yielding $10.6\ \mathrm{mW}$ of power consumption at $1\ \mathrm{Gsps}$ and 4 bit resolution. A down-side of this design is that comparator switching generates considerable kick-back noise into the ADC input, which necessitates the use of a low-impedance buffer for driving the ADC, and so the overall power reduction of this system is limited. Other comparators [18, 19] have been proposed with low kick-back noise. However, these approaches show a relatively high power consumption due to the need for a static reference ladder or due to a folded architecture. Combining the best of both worlds would yield a superior comparator: cascode

transistors to reduce the kick-back noise while maintaining the low power consumption and removing the need of a static reference ladder due to off-setting the input transistors.

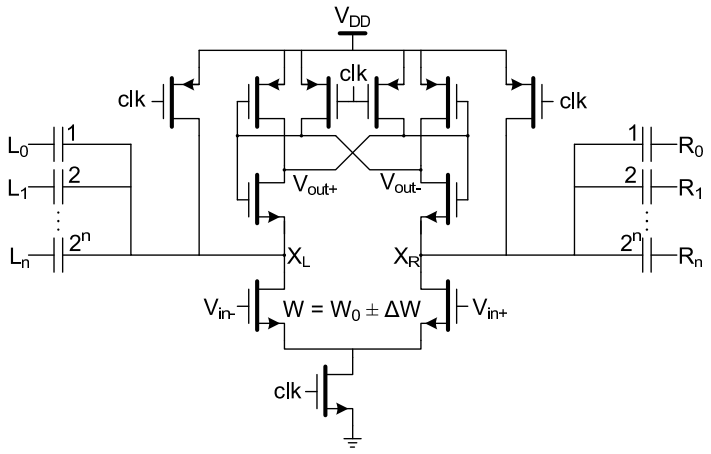


Figure 4.22: Comparator proposed by [17].

In [17] a comparator architecture for a low power, high speed ADC is presented. By using transistors with off-setted widths ($W_0 \pm \Delta W$) in the input differential pair, the need for reference voltages is omitted, reducing the power consumption. The resulting offset voltage can be expressed as a first-order approximation, eq. (4.31).

$$\Delta V_{th} = \frac{V_{GS} - V_{Tn}}{2} \frac{\Delta W}{W} \tag{4.31}$$

Due to process and mismatch variations a large variation in threshold voltage can be expected, compared to the Least Significant Bit (LSB) of the ADC. This requires calibration. An array of binary-scaled switchable capacitors connected to the drains of the input NMOS transistors can be used. The variation in voltage can be expressed as:

$$V_{OD} = \frac{V_{GS} - V_{Tn}}{2} \frac{\Delta C}{C}. \tag{4.32}$$

A downside of the comparators used in this circuit is the significant amount of kickback noise injected into the input nodes when the clock switches. This noise is caused by large voltage and current variations at the input

NMOS transistor pair when the comparator is switched on or off. These variations result in charge being pushed or pulled from to the input-nodes through the gate-drain and gate-source capacitances of the input pair.

These charges are converted into voltages over the output impedance of the driving stage. This results in a change of the input voltage at the very moment the comparator is switched on, the moment when it is most sensitive. Or even worse: the voltage change caused by the switching off of the comparator may not have disappeared before the next cycle, resulting in a memory effect making the state of the comparator depend on its previous state rather than solely on the actual input voltage. These effects reduce the accuracy of the ADC and increase the need for a low-impedance drive stage, consuming a considerable amount of power as the low impedance must be maintained up to and above the ADC clock frequency.

4.3.1 A reduced kickback noise comparator

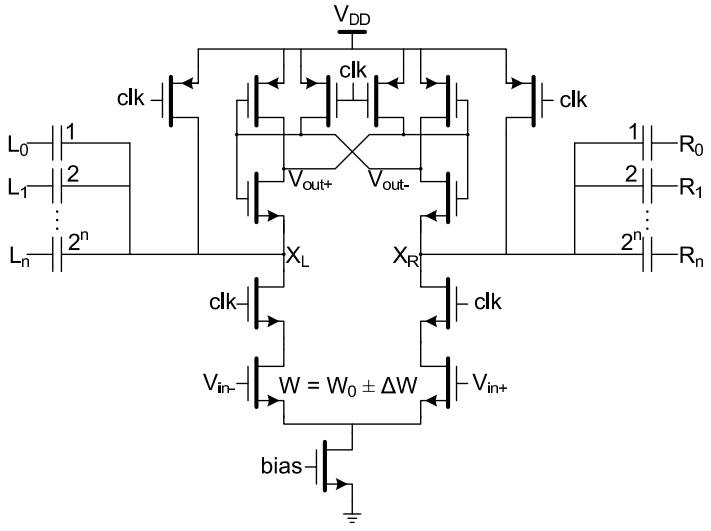


Figure 4.23: Comparator with reduced kickback noise.

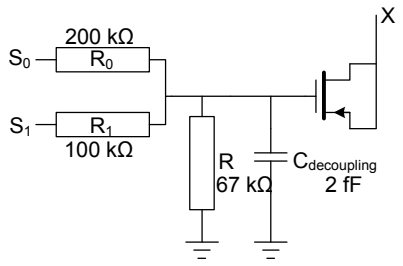


Figure 4.24: Variable PMOS capacitor.

To reduce the overall power consumption, including the driver, one needs to reduce the kick-back noise. A straightforward way to realize this is to add a source follower to the input transistors [19]. However, this not only adds static power consumption, but also increases the thermal noise. The proposed comparator shown in figure 4.23 is a better approach. It is less effective in terms of kick-back noise reduction compared to [19], but the reduction is significant, and it does not increase the input noise nor the power consumption. This architecture reuses the idea of offsetting the widths of the input NMOS transistors of the comparators to induce an offset voltage and eliminate the reference ladder, and combines it with cascode transistors [18] to isolate the input differential pair from the regenerative part, and reduce to the fast voltage swings across the input transistors. These cascodes separate the calibration capacitors from the drain-gate capacitors of the input differential pair, eliminating the large charge injections to the input nodes and improving the comparator sensitivity, effectively reducing the kick-back noise to clock feed-through.

4.3.2 PMOS capacitor

Thanks to the improved comparator sensitivity, a more accurate calibration can be applied. In [17] the switchable capacitors are implemented as pmos capacitors, so that the minimum calibration step is determined by the minimum size of a transistor. To reduce the minimum calibration step the circuit in figure 4.24 is proposed.

The operation of the device can be explained when looking at the different phases in the comparison. In the first phase – as the clock makes a transition from low to high – the lower transistors start sinking current out of the calibration capacitors which were charged to the supply voltage. As the

transistors can be replaced with their g_m, the voltage on X can be expressed as $v_X(t) = V_{DD}\exp(-t\ g_m/C)$. As soon as the voltage on one of the branches drops below the threshold voltage of the NMOS transistors of the regenerative part, the positive feedback kicks in and the comparator reaches a fixed state.

The capacitance of the calibration capacitors – implemented as PMOS transistors with drain and source connected to node X – can be changed by tuning the gate voltage. By crude approximation, one could say that if the gate-source voltage is higher than the threshold voltage (V_{Tp}), the capacitance is equal to the oxide capacitance (C_{ox}). If the gate-source voltage is lower than V_{Tp}, the channel in the PMOS is formed and its capacitance (C_{ch}) comes in series with C_{ox}, resulting in a total capacitance of $C_L = \frac{1}{1/C_{ox}+1/C_{ch}}$. This mechanism is used to change the total capacitance on node X in [17].

The smallest variation in capacitance is achieved when switching the channel of a minimum size pmos capacitor on and off. To make a smaller variation, the gate voltage (V_G) of such a minimum size capacitor can be set between the 2 logical values. When V_G is lower than $V_{DD} - V_{Tp} - V_{Tn}$ the channel is never pinched off; when V_G is larger than $V_{DD} - V_{Tp}$ the channel can never be formed. In between these states the capacitance at the starting of phase 1 of the comparison is equal to C_L but as soon as the voltage on node X drops below $V_G + V_{Tp}$ the capacitance is changed to C_{ox}. This results in an average capacitance between C_{ox} and C_L which has been simulated and modelled as in eq. (4.33).

By choosing the gate voltage such that a linear change in capacitance results, a more accurate calibration can be obtained. This results in a more accurate Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) increasing the performance of the ADC. In figure 4.24, four different voltages can be applied, but as can be seen, this technique can be generalized to even higher bit resolutions.

$$C(V) = \begin{cases} C_{ox} & : \quad V > V_{DD} - V_{Tp} \\ -\frac{C_{ox}/V_{Tn}}{C_{ch}/C_{ox}+1}(V_{DD} - V_{T_p} - V) + C_{ox} & : \quad V_{DD} - V_{Tp} - V_{Tn} < V < V_{DD} - V_{Tp} \\ \left(\frac{1}{C_{ox}} + \frac{1}{C_{ch}}\right)^{-1} & : \quad V < V_{DD} - V_{Tp} - V_{Tn} \end{cases} \tag{4.33}$$

	Proposed Comparator	[17]	[18]	[19]
Technology (CMOS)	$0.18\ \mu$m	$0.18\ \mu$m	90 nm	$0.18\ \mu$m
Common kick-back charge (aC/cycle)	235.91	309.53	182	-
Differential kick-back charge (aC/cycle)	11.99	92.51	-	-
Power Dissipation (μW)	106.5	138.7	27.9	202
Sampling frequency (GHz)	1	1	1	0.25
Input-referred Thermal Noise (1σ in mV)	0.66	0.5	-	-

Table 4.2: Comparison of the key figures.

4.3.3 Simulation results

The proposed comparator was simulated in a $0.18\ \mu\mathrm{m}$ CMOS technology[3] at $1.8\ \mathrm{V}$ supply and driven by a 1GHz clock. To measure the kick-back noise, the input gate voltage was measured over a $1\ \mathrm{k}\Omega$ resistor inserted between the input transistors (V_{in+}, V_{in-}) and the differential voltage source. Figures 4.25 and 4.26 show the differential and common-mode kick-back noise respectively from the proposed comparator and the reference design of [17]. The voltages are measured for a differential input signal of $100\ \mathrm{mV}$. This figure shows that the differential kickback at the sampling events (0, 1 and 2ns) is significantly reduced. The simulations show that the voltage swings at the drain and source of the input NMOS transistors are reduced (fig. 4.27 and 4.28 respectively). The main voltage swings now occur over the cascode transistors isolating kick-back charges from the inputs. Figure 4.28 also shows that the common-mode kick-back voltage is inverted compared to the original design as the drain capacitor of the input transistors is charged to ground instead of V_{DD}.

[3]The ADC was the first step in the proof of concept of an integrated SoC, as the fast 2-channel ADC of the PCB demonstrator was dominating the power consumption of the analog front-end. Later in the project, a lower technology node was chosen since this was beneficial to the PA and DSP design and the ADC redesign for $0.13\ \mu\mathrm{m}$ CMOS was done by Essensium.

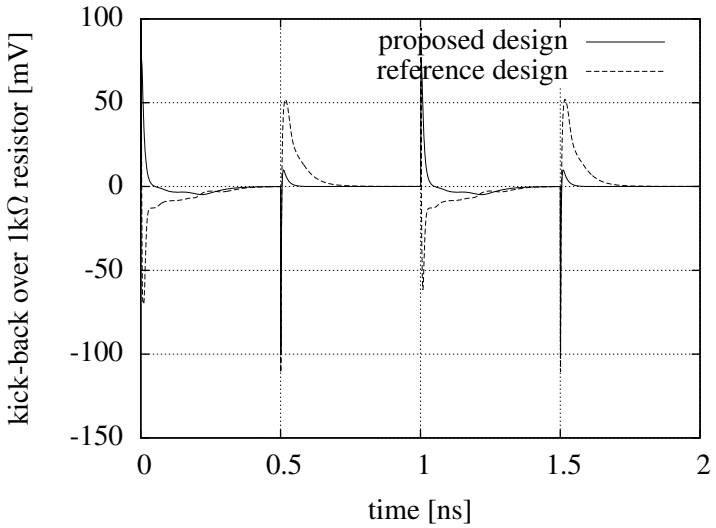


Figure 4.25: Common-mode voltage swing due to kick-back over a 1 kΩ resistor connected at the input gates.

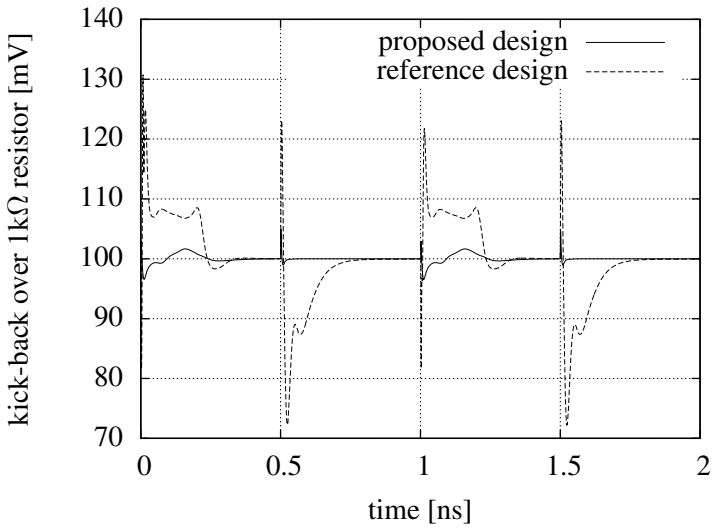


Figure 4.26: Differential voltage swing due to kick-back over a 1 kΩ resistor connected at the input gates.

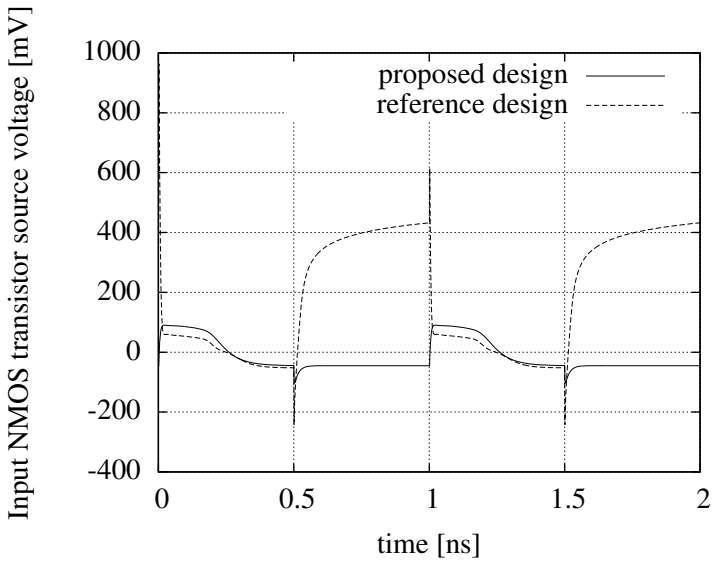


Figure 4.27: Voltage swings at the source node of the input transistors.

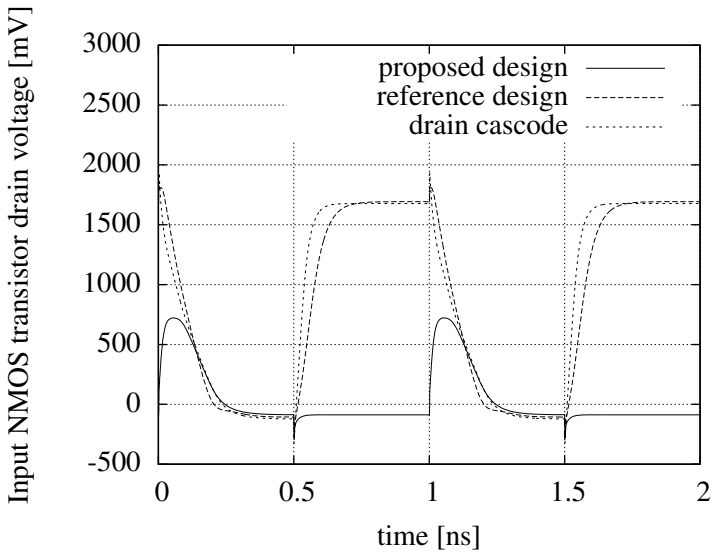


Figure 4.28: Voltage swings at the drain node of the input and cascode transistor.

In table 4.2 the resulting figures are compared. The differential kickback is

8 times smaller, whereas the power consumption is reduced by 25% compared with [17]. The kickback reduction relaxes the requirements on the output impedance of the preceding amplifier stage, resulting in an additional reduction of the overall power consumption. The input noise is still comparable to the reference design. For a 1GHz clock and 200 $\mathrm{mV_{pp}}$ input range, this input noise results in 3.8 Effective Number Of Bits (ENOB) for a 4 bit ADC design, or 5.2 ENOB for a 6 bit ADC design. The performance of [18] is comparable, keeping the technology scaling in mind. However, the stated power consumption does not yet include the power consumption of the reference ladder. The kickback of [19], though not mentioned, is lower than in the proposed design. However, this technique consumes two times more power at a much lower sampling frequency (250 MHz).

4.3.4 Implementation and measurements

The new comparator with reduced kick-back noise is implemented in a 4-bit ADC with 200 mVpp full scale input range, and has been fabricated in a 0.18 μm CMOS technology. The resulting die is shown in figure 4.29.

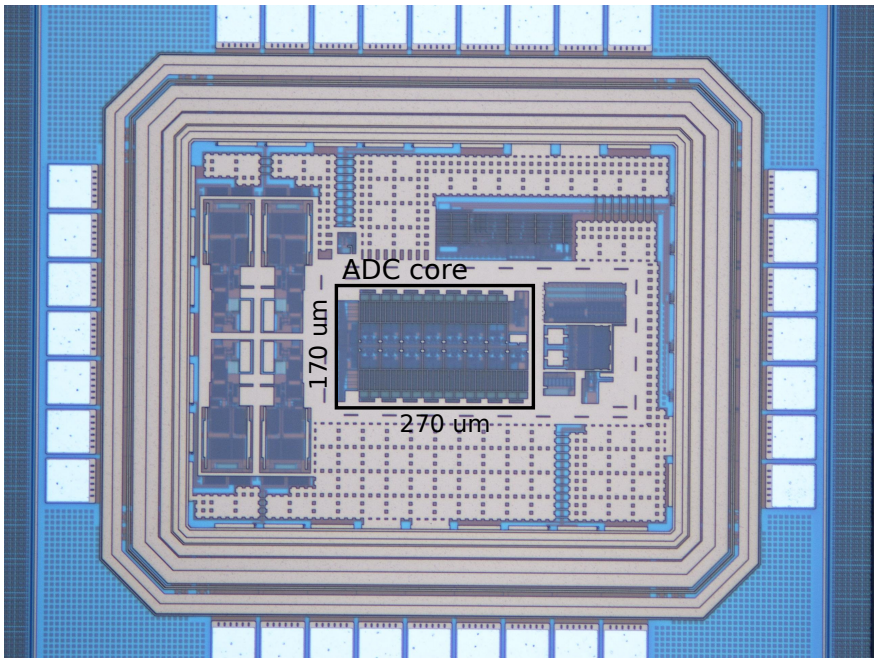
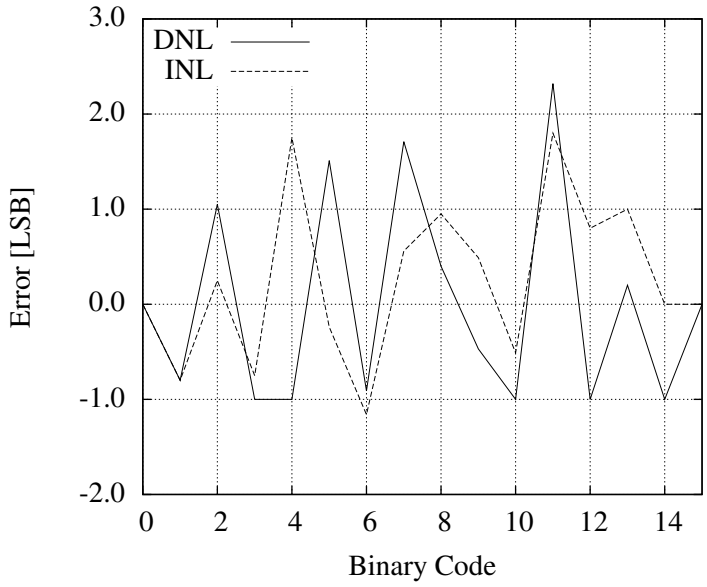


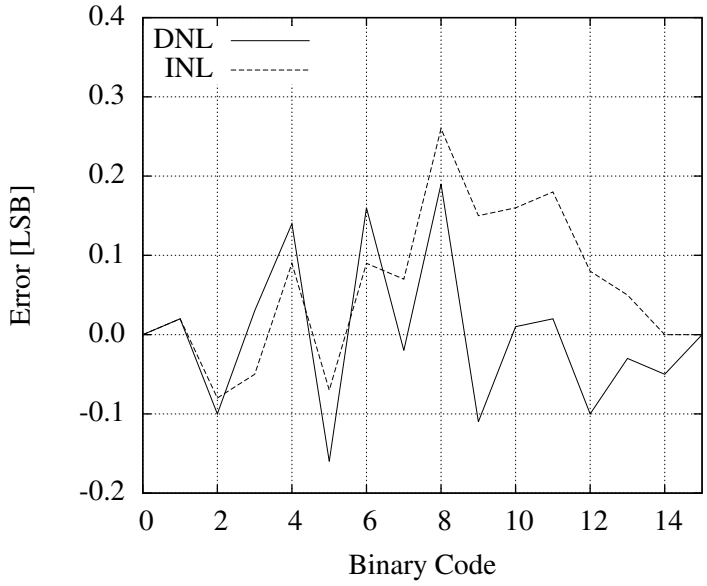
Figure 4.29: ADC die micrograph.

The differential input signal was applied to the chip through a balun and the output codes were sampled with a $10\ \mathrm{Gsps}$ digital oscilloscope and processed offline. The linearity was measured by applying a $10\ \mathrm{MHz}$ triangular wave. The resulting DNL and INL is shown in figure 4.30. Without calibration large variations and even missing codes can be observed. Due to process and mismatch errors, the threshold of the comparators can vary up to 2 LSB. To reduce these non-linearities, a resistor ladder, producing the threshold voltages of the different comparators, is added next to the ADC core. These voltages can be connected to the input of the ADC to allow calibration. The calibration logic is implemented off chip and will start by detuning all comparators. Next, it will apply the lowest threshold voltage and tune the first comparator so that half of the time the comparator triggers. The next step is to increment the applied input voltage and repeat the measurement for the subsequent comparators.

After all comparators are calibrated, the DNL is below 0.2 LSB and the INL below 0.25 LSB. The dynamic performance is analysed by applying a full scale 200 mVpp differential sine wave. The captured data is then fitted to an ideal sine wave, and with these parameters the Signal to Noise and Distortion Ratio (SNDR) and the ENOB was calculated. The resulting measurements for sample frequencies of $500\ \mathrm{MHz}$ and $700\ \mathrm{MHz}$ are shown in figure 4.31. The ENOB with a sample frequency of $500\ \mathrm{MHz}$ is 3.92 at the Nyquist frequency and 3.77 with a sample clock of $700\ \mathrm{MHz}$. Above $700\ \mathrm{MHz}$ the ENOB starts to degrade quickly due to the speed limitations of the Read-Only Memory (ROM)-based digital circuit which converts the thermometer code of the comparators to binary code. Adding a flip-flop in between the comparators and the ROM would solve this timing issue, extending the operating frequency with only a marginal increase of the power consumption. The measured power consumption is $4.30\ \mathrm{mW}$ at $500\ \mathrm{MHz}$ and $5.56\ \mathrm{mW}$ at $700\ \mathrm{MHz}$ from a $1.8\ \mathrm{V}$ supply. These figures include the 2-stage input buffer which consumes $1.13\ \mathrm{mW}$. Without the power consumption of the buffer, the FOM of the ADC core is respectively $0.42\ \mathrm{pJ}$ and $0.46\ \mathrm{pJ}$ per conversion step at $500\ \mathrm{MHz}$ and $700\ \mathrm{MHz}$. Including the power consumption of the buffer the FOM is still $0.57\ \mathrm{pJ}$ and $0.58\ \mathrm{pJ}$ per conversion step respectively. Table 4.3 compares these figures with the state of the art [17, 20–24]. To the author's knowledge, this design achieves the lowest FOM for flash ADCs in this technology node. The new ADC concepts were patented [25] as a continuation of the original ADC design (shown in figure 4.22) developed by IMEC [17]. The results were published in two journal papers [26, 27].



(a)



(b)

Figure 4.30: Differential and integral non-linearity before (a) and after (b) calibration at a sample rate of 700 MHz.

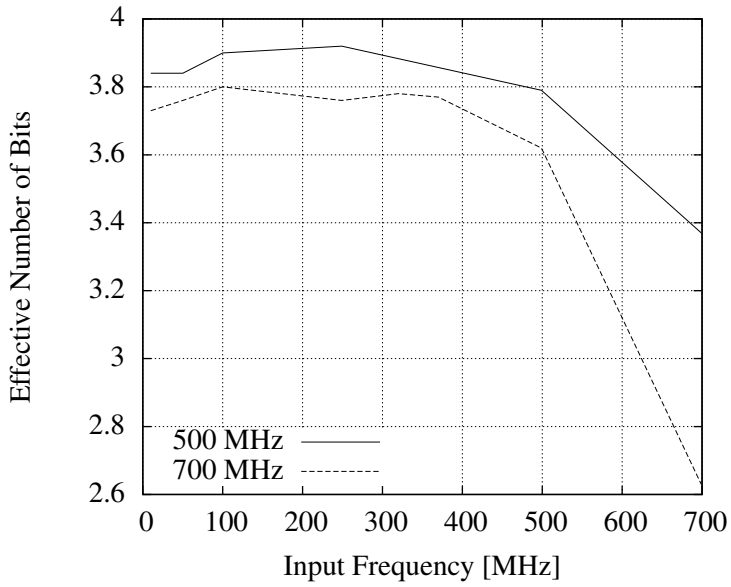


Figure 4.31: Effective number of bits versus input frequency at sample rates of 500 MHz and 700 MHz.

	Tech.	# of bits	DNL	INL	ENOB @ Nyquist	Fs (MHz)	Power (mW)	FOM (pJ/conv)
this work	0.18 μm	4	< 0.19	< 0.27	3.77	700	4.43	0.46
[17]	0.18 μm	4	< 0.25	< 0.17	3.8	500	5.2	0.73
					3.7	1000	10.6	0.81
[20]	0.18 μm	4	0.4	1.1	3.24	400	20	5.3
[21]	0.18 μm	4	0.04	0.06	3.61	2000	42	1.73
[22]	0.13 μm	6	< 0.49	< 0.42	4.69	1600	180	4.36
[23]	0.13 μm	6	< 0.6	< 0.4	5.6	600	90	3.09
					5.7	1200	160	2.56
[24]	0.13 μm	5	< 0.24	< 0.39	4.44	2000	120	3.07
					4.54	3200	120	4.30

Table 4.3: Comparison with state-of-the-art analog to digital converters.

References

[1] W. Sansen. *Analog Design Essentials*. Springer, 2006.

[2] E. De Backer, J. Bauwelinck, C. Melange, E. Matei, P. Ossieur, X.-Z. Qiu, J. Vandewege, and S. Horvath. 2.5 V 35 dBm IIP3 75 MHz sixth-order active RC filter. *Electronics Letters*, 44(7):466 –467, 2008.

[3] G. Moschytz. The design of active RC filters for the Analog Front End of IC communication systems. In *15th IEEE International Conference on Electronics, Circuits and Systems*, pages 19 –20, Sept. 2008.

[4] K. Tripetch and G. Khunead. Lowest power optimal dynamic range continuous time MOSFET-C filter in submicron CMOS technology compared with experimental measurement results. In *ICCAS-SICE*, pages 5500 –5504, Aug. 2009.

[5] L. Yue and J.I. Sewell. A comparison study of SC biquads in the realisation of SC filters. In *IEE Colloquium on Digital and Analogue Filters and Filtering Systems*, pages 101/1 –101/9, Nov. 1993.

[6] H. Yang, S. Cha, S. Lee, S. Lee, J. Lim, and J. Choi. A 1.2V Wide-Band SC Filters for Wireless Communication Receivers. In *IEEE Region 10 Conference*, pages 1 –4, Nov. 2006.

[7] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynanen, and K. Halonen. A 1.2V 240MHz CMOS Continuous-Time Low-Pass Filter for a UWB Radio Receiver. In *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pages 122 –591, Feb. 2007.

[8] R. Thirugnanam, Dong Sam Ha, Bong Hyuk Park, and S.S. Choi. Design of a tunable fully differential GHz range Gm-C lowpass filter in 0.18 μm CMOS for DS-CDMA UWB transceivers. In *IEEE International Symposium on Circuits and Systems. Proceedings*, pages 4 pp. –2380, 2006.

[9] J.L. Chan and S.S. Chung. Universal switched-current integrator blocks for SI filter design. In *Proceedings of the Asia and South Pacific Design Automation Conference*, pages 261 –264 vol.1, Jan. 1999.

[10] J.B. Hughes, I.C. Macbeth, and D.M. Pattullo. Developments in switched-current filter design. In *IEE Colloquium on Digital and Analogue Filters and Filtering Systems*, pages 11/1 –11/4, May 1990.

[11] D. M. Binkley. *Tradeoffs and Optimizations in Analog CMOS design*. Wiley & Sons, June 2008.

[12] B. Nauta. *Analog CMOS Filters For Very High Frequencies*. Kluwer Acaemic Publishers, 1964.

[13] S. D'Amico, M. Conta, and A. Baschirotto. A 4.1-mW 10-MHz Fourth-Order Source-Follower-Based Continuous-Time Filter With 79-dB DR. *IEEE Journal of Solid-State Circuits*, 41(12):2713 –2719, Dec. 2006.

[14] S. D'Amico, M. De Matteis, and A. Baschirotto. A 6th-Order 100 μA 280MHz Source-Follower-Based Single-loop Continuous-Time Filter. In *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pages 72 –596, Feb. 2008.

[15] A. Liscidini, A. Pirola, and R. Castello. A 1.25mW 75dB-SFDR CT filter with in-band noise reduction. In *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pages 336 –337,337a, Feb. 2009.

[16] G. Torfs, Z. Li, J. Bauwelinck, J. Vandewege, and P. Spiessens. A novel large input range source-follower based filter architecture. *IEICE Electronics Express*, 8(24):2025–2028, 2011.

[17] P. Nuzzo, G. Van der Plas, F. De Bernardinis, L. Van der Perre, B. Gyselinckx, and P. Terreni. A 10.6mW/0.8pJ power-scalable 1GS/s 4b ADC in 0.18μm CMOS with 5.8GHz ERBW. In *Proceedings of the 43rd annual Design Automation Conference*, DAC '06, pages 873–878, New York, NY, USA, 2006. ACM.

[18] T. Sundstrom and A. Alvandpour. A Kick-Back Reduced Comparator for a 4-6-Bit 3-GS/s Flash ADC in a 90nm CMOS Process. In *14th International Conference on Mixed Design of Integrated Circuits and Systems*, pages 195 –198, June 2007.

[19] G. Zhang, B. Wang, F. Liang, and Z. Shao. A low-kickback-noise and low-voltage latched comparator for high-speed folding and interpolating ADC. *IEICE Electronics Express*, 5(22):943–948, 2008.

[20] S. Banik, D. Gangopadhyay, and T.K. Bhattacharyya. A low power 1.8 V 4-bit 400-MHz flash ADC in 0.18 μm digital CMOS. In *19th International Conference on VLSI Design. Held jointly with 5th International Conference on Embedded Systems and Design*, page 6 pp., Jan. 2006.

[21] L. Wu, F. Huang, Y. Gao, Y. Wang, and J. Cheng. A 42 mW 2 GS/s 4-bit flash ADC in 0.18- μm CMOS. In *International Conference on Wireless Communications Signal Processing*, pages 1 –5, Nov. 2009.

[22] A. Ismail and M. Elmasry. A 6-Bit 1.6-GS/s Low-Power Wideband Flash ADC Converter in 0.13-μm CMOS Technology. *IEEE Journal of Solid-State Circuits*, 43(9):1982 –1990, Sept. 2008.

[23] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner. A 6-bit 1.2-GS/s low-power flash-ADC in 0.13-μm digital CMOS. *IEEE Journal of Solid-State Circuits*, 40(7):1499 – 1505, July 2005.

[24] Y.-Z. Lin, C.-W. Lin, and S.-J. Chang. A 5-bit 3.2-GS/s Flash ADC With a Digital Offset Calibration Scheme. *IEEE Transactions on Very Large Scale Integration Systems*, 18(3):509 –513, March 2010.

[25] G. Van der plas, P. Nuzzo, F. De Bernardinis, J. Bauwelinck, Z. Li, G. Torfs, J. Vandewege, and X. Yin. A/D Converter Comprising a Voltage Comparator Device. Continuation in part of WO2007088175, US7652600 (B2), granted on 26 Jan. 2010.

[26] G. Torfs, Z. Li, J. Bauwelinck, X. Yin, J. Vandewege, and G. Van Der Plas. A Low-Power Reduced Kick-Back Comparator with Improved Calibration for High-Speed Flash ADCs. *IEICE Transactions on Electronics*, E92C(10):1328–1330, OCT 2009.

[27] G. Torfs, Z. Li, J. Bauwelinck, X. Yin, G. Van der Plas, and J. Vandewege. Low-power 4-bit flash analogue to digital converter for ranging applications. *Electronics Letters*, 47(1):20–21, JAN 6 2011.

5 Antenna

5.1 Introduction

An important factor in a transceiver's link budget is the antenna efficiency. There is an enormous variety of antennas and choosing the right one is challenging. A few constraints will bias the choice of the favoured solution:

- The antenna should make use of PCB technology. This will allow a low cost and easy integration since it can be incorporated in the design of the transceiver PCB.
- It should be more or less omnidirectional. This will allow efficient and reliable ranging.

To find the right antenna, different shapes of PCB antennas are studied. Furthermore, different existing PCB substrate materials are evaluated to make a trade-off between cost and performance. Finally, an efficient method to optimize and co-design the antenna and the transceiver is proposed.

5.2 Exploration of various antenna types

When looking into different kinds of antennas, one can distinguish two fundamentally different types of operation: electric and magnetic antennas. To choose the optimum antenna it is important to notice the different effects

those two working mechanisms will have. Therefore, the two antenna types will be described separately and different properties of the antennas (like bandwidth, size, impedance, radiation pattern) will be discussed. Due to the desired omnidirectional property only a limited amount of shapes are available. [1, 2]

5.2.1 Dipole and monopole antennas

An electric dipole is an antenna where ideally the current is distributed linearly over the radiating element. This will result in a typical solution of Maxwell's equations: the fields propagate in Transverse Magnetic (TM) mode, i.e. there is no magnetic field component in the direction of propagation.

Different variations of an electric dipole antenna have been studied with the goal to minimize the required area on a PCB: $\lambda/2$ dipole, $\lambda/4$ monopole and inverted F-antenna.

$\lambda/2$ Dipole antenna

A half-wavelength dipole antenna consists of a piece of metal with length around half a wave length on the substrate. This piece of metal commonly split in 2 halves is then driven differentially, inducing a current distribution which is maximum at its feed points and zero on its ends. A possible implementation including a distributed balun is shown in figure 5.1. Its impedance can be estimated from a thin wire model, where in the ideal case 73 Ω can be expected at resonance.

Increasing the wire diameter will result in a reduction of the resonance frequency, giving rise to the need of shortening the dipole, and lowering its input resistance. This way a $50\ \Omega$ match can be achieved. Further on, the broader the wire diameter, the slower the slope of the reactance over frequency, resulting in a more broadband antenna. A plus for the application.

The antenna should be kept away from nearby metal. Nearby metal will result in capacitive loading of the antenna, reducing the efficiency. The radiation pattern of a dipole looks like a donut, it has nods in the direction of the dipole arms but is fairly omnidirectional.

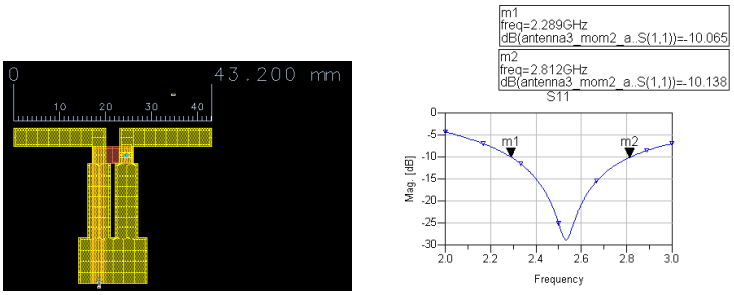


Figure 5.1: Layout and simulation results of a dipole antenna.

$\lambda/4$ Monopole antenna

A monopole uses a conductive ground plane as a mirror, to act as a dipole antenna. A possible implementation is shown in figure 5.2. This results in the same electrical characteristics, 36.5 Ω of input impedance (half of the 73 Ω differential impedance of a dipole). As a low impedance ground plane is required, a large area on the PCB needs to be reserved to accommodate it. A common way to overcome this problem is by folding the antenna, resulting in a capacitive top load which needs to be compensated. A standard way to compensate this is by using an inverted F-antenna.

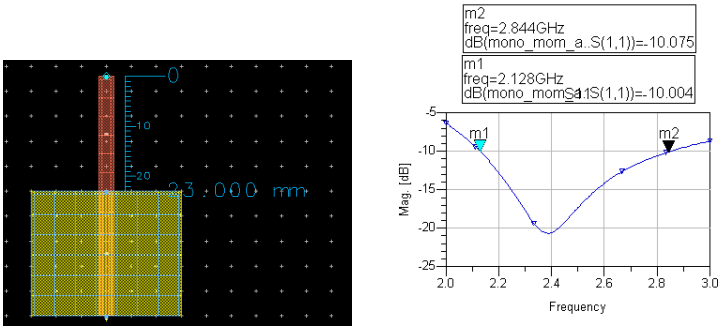


Figure 5.2: Layout and simulation results of a monopole antenna.

Inverted F-antenna

An inverted F-antenna is a monopole antenna which is folded towards the ground plane. The capacitive top-load which appears this way, is compensated by adding an inductive stub at the knee of the antenna. Figure 5.3 shows an implementation of this antenna.

The problem with this type of antenna is the capacitive load which is very sensitive to the varying environment, for example the proximity of the human body, making the antenna very sensitive to detuning.

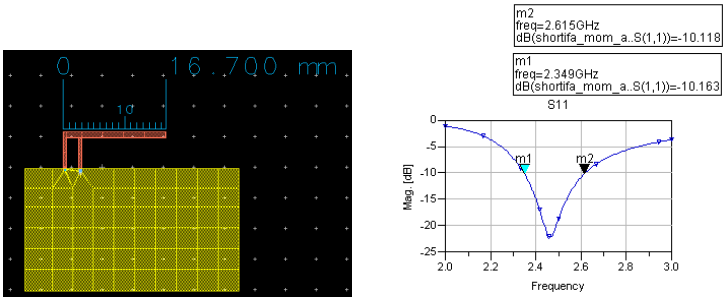


Figure 5.3: Layout and simulation results of an inverted F antenna.

5.2.2 Loop antennas

A loop antenna can be seen as the dual of an electric dipole: as a magnetic dipole. The circular current will generate a linear flux distribution. Dual to the electric dipole antenna, solving Maxwell's equations will yield a Transverse Electric (TE) mode, i.e. there will be no electric field component in the direction of propagation.

Both a $\lambda/2$ Loop antenna as a full wave loop antenna are discussed.

$\lambda/2$ Loop antenna

A half-wave loop antenna is a piece of conductor bent in a closed curve, this can be a circle, rectangle, triangle, ..., opened at one end to have 2 terminals. In literature and experiments, a circular thin wire antenna is most often discussed because of the simple associated mathematics. A loop antenna's resistance and reactance rises with its length and reaches a maximum when its length is equal to half a wavelength. To eliminate its inductive reactance and make it resonant, the antenna can be loaded with a capacitance, forming a LC-tank structure. The voltage and current distribution vary over the antenna structure, from a maximum voltage, minimum current over the resonant capacitor to a zero voltage and maximum current at the opposite point.

This offers the ability to very easily match impedance: choosing the right feed point on the antenna can give any desired resistance ranging from 0Ω

to the maximum resistance located over the resonating capacitance. Resulting in a structure which can be seen as a tap on the coil of the LC-tank circuit. Figure 5.4 shows such a tapped $\lambda/2$ loop antenna.

The Q-factor of this structure, its ability to store energy and not radiate it into space, needs to be kept low to achieve sufficient bandwidth. This quality factor depends on the ratio of loop-radius over conductor width, the larger this ratio, the higher the Q-factor.

The shape of the loop will influence the efficiency of the radiator. The larger the encircled area, the more magnetic flux will pass through it. This results in an optimum circular geometry. However, this is not the most practical layout from a manufacturing perspective, a compromise needs to be found.

Due to its magnetic nature, changes in the environment will have little effect on the radiation properties, as most materials have a permeability equal to one.

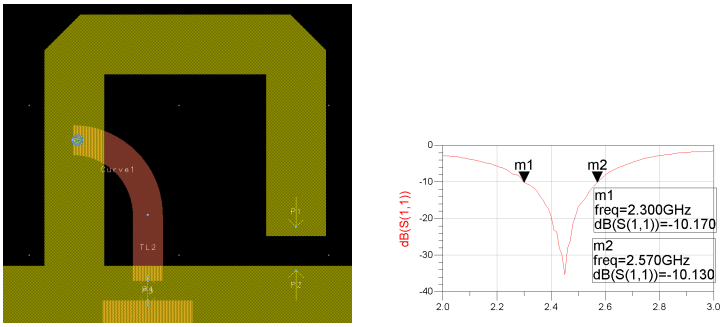


Figure 5.4: Layout and simulation results of a $\lambda/2$ loop antenna.

λ Loop antenna

A full wave loop is a closed curve, resonating at the radiating frequency. Any two points on the circumference can be chosen as feed-points. This gives the ability to drive the antenna differentially at any given impedance, going from zero when the to feed-points are located together or to a maximum value, depending on the Q-factor of the resonator, when the feed-points are on opposite sites. In between the feed-points a virtual ground point appears which can be connected to any wanted reference, for example to superpose a DC voltage on the feed-points, e.g. to supply the output stage of the PA.

The surface area of a full wave loop is four times the surface area of a half wave loop, but it has a differential nature and removes the capacitor from

the design. Figure 5.5 shows an implementation of a λ loop antenna with matching stubs.

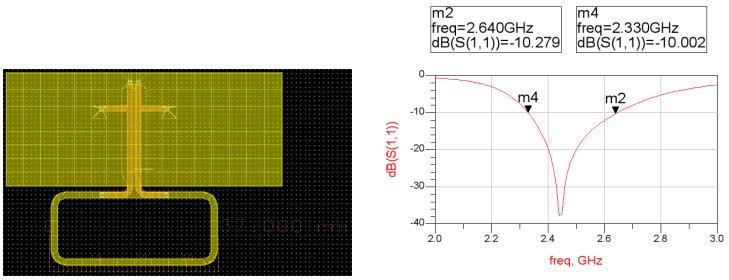


Figure 5.5: Layout and simulation results of a λ loop antenna.

5.2.3 Conclusion

Different types of antennas have been described with each offering advantages and showing disadvantages. A global conclusion is that the higher the desired efficiency, the more area is required. Existing techniques to reduce the area have been studied, such as folding to an inverted F-antenna, but they always result in a loss of efficiency.

When comparing electric and magnetic antennas, an important remark is the robustness of magnetic antennas to environmental factors. For example in small portable devices, the change of the surrounding dielectric environment (e.g. proximity to the human body) will influence the impedance of electric antennas, resulting in a more difficult PA-design as the stability should be guaranteed on all these possible impedance levels. As the properties of the magnetic antenna mainly depend on the magnetic properties of the surroundings, less influence can be expected, reducing the demands on the integrated designs.

5.3 Available substrates for on-board antennas

The cheapest and most common used substrate material is FR4. It is widely available, low cost and can be handled by different PCB manufacturers. So, if it is possible to make an antenna which is compliant with the specifications, FR4 is the preferred material.

The downside of FR4 is the changing dielectric constant over temperature and its relatively high loss tangent. Other materials are available that have very good temperature and mechanical stability and offer a wide range

of dielectric constants, however, at higher cost. An overview of typical PCB materials with their associated dielectric constant and loss tangent are shown in table 5.1.

As long as the surroundings are quite mild, i.e. room temperature, normal humidity, pressure, ... FR4 can be used. If the surroundings change too much, other materials will need to be considered.

Substrate name	ϵ_r	tan δ
FR4 [3]	4.3	0.018
RO3003 [4]	3	0.0013
RO3006 [4]	6.15	0.0020
RO3010 [4]	10.2	0.0023
RO5870 [5]	2.33	0.0012
RO5880 [5]	2.2	0.0009

Table 5.1: Different substrates with their key figures.

Depending on the kind of antenna used, the dielectric constant and the loss tangent will have more or less effect on the performance.

5.4 Derivation of an efficient co-design methodology

Since Electro-Magnetic (EM) field simulations and the RF circuit simulations are performed in two different tools (ADS Momentum and Cadence/Spectre), an intelligent co-optimization strategy needs to be found.

In first instance, the antenna can be matched to different impedances, so choosing the desired impedance will mostly depend on the figure needed for optimal efficiency of the PA. The current/voltage relationship will have to be chosen to reach the desired output power. To maximize efficiency, the voltage will be maximized (with respect to the breakdown voltages of the devices) at the output nodes to reduce the effect of ohmic losses.

Most efficient PA topologies use output matching networks to suppress/reflect harmonics on their output nodes, to shape the waveforms to realize a current-voltage relationship on the active device where drain current and drain-source voltage are mostly separated in time, realizing a minimum of loss. Matching networks, implemented on chip, take a lot of area (due to the use of inductors) and will be of poor quality (due to the limited Q-factors

realizable on chip). Incorporating this network in the matching network of the antenna will result in a much better performance.

After fixing the output impedance of the PA at the different harmonic frequencies (fundamental + the effect of the output matching), the antenna can be designed to meet these impedances over the desired bandwidth. This can be done by changing the antenna structure itself or by adapting the matching network towards the antenna, but the design-work is limited to the antenna itself without iterating over the PA design.

As a final step, the antenna s-parameters can be exported from ADS Momentum, imported in Cadence schematics and simulated with Spectre. In this way the effect of the antenna impedance on the PA behavior can be evaluated.

While importing the S-parameters in Cadence special care has to be taken towards the DC behavior of the antenna. The DC behavior is not included in the s-parameters and will be an extrapolation of the low frequency behavior. This is not always correct. It is advisable to use an ideal bias-T in the simulation bench to overcome this problem.

5.5 Antenna Implementation and Measurements

The antenna prototype was made on a $1.55\ \mathrm{mm}$ FR4 substrate with an in house milling machine. The resulting antenna is shown in figure 5.6.

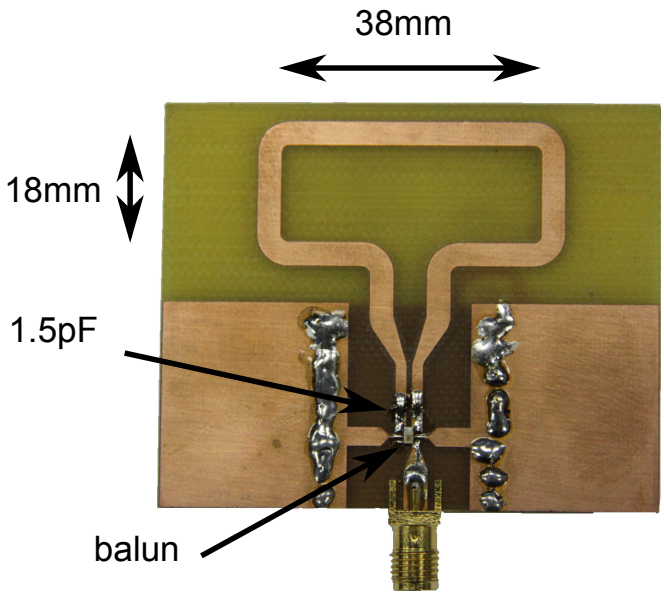


Figure 5.6: Picture of the fabricated antenna.

5.5.1 Impedance Matching

The ideal antenna would be immediately matched to the differential LNA and the differential PA of that ranging tranceiver. In chapter 3 it is described how a transmit/receive switch can be omitted and the interconnection with the transceiver will be $100\ \Omega$ differential. It was possible to realize this impedance simply by adding two $1.5\ \mathrm{pF}$ capacitors in series with the antenna, limiting the overall component count.

This impedance is difficult to interconnect with standard single-ended $50\ \Omega$ test equipment. To facilitate this interconnection, a balun with an impedance ratio of 2 is inserted. This results in a 50Ω interconnect.

The antenna input matching has been measured with a vector network analyser. The resulting S_{11} parameter is shown in figure 5.7. The realized $-10\ \mathrm{dB}$ bandwidth (corresponding to a S_{21} bandwidth of -3 dB) is $200\ \mathrm{MHz}$.

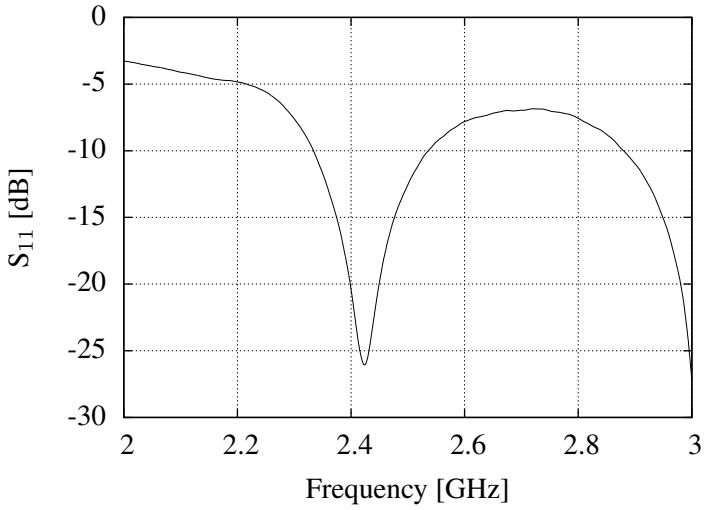


Figure 5.7: Measured S_{11}.

5.5.2 Radiation Patern

The radiation pattern has been measured in an anechoic chamber. The resulting radiation pattern is shown in figure 5.8. The ground plane clearly has a large shielding effect. The half plane omnidirectionality makes is sufficient for most ranging applications, for basestations as well as mobile

nodes. Basestations are most effective when placed on corners of the ranging area. On mobile nodes the antenna can be placed such that minimum radiation is absorbed by the carrier. If the antenna is positioned well it can realize a gain of 3 dB, gain that isn't needed in the RF front-end, and thus, offering power and noise reduction.

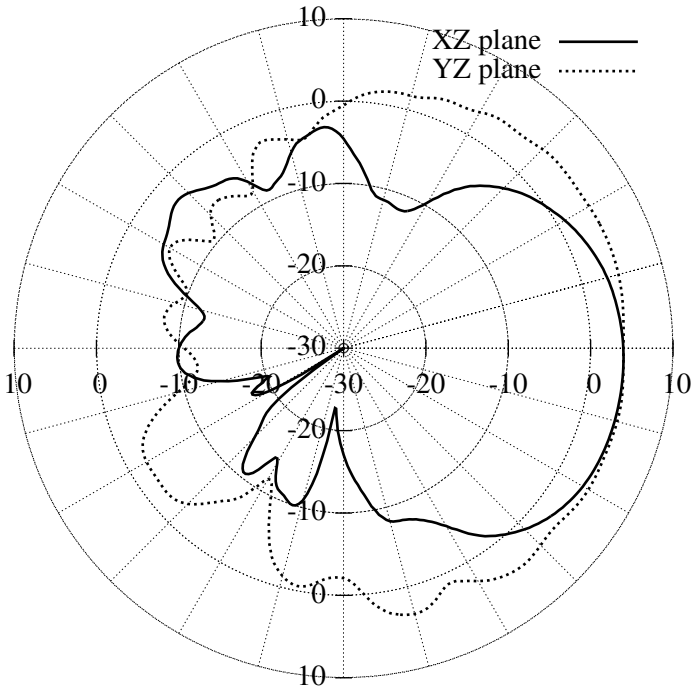


Figure 5.8: Measured Radiation pattern.

5.6 Conclusion

After considering a wide range of antennas, the most suitable antenna type is a differential λ loop magnetic antenna on FR4. It can be made sufficiently broadband to transmit and receive the ranging signal, while area and efficiency are interchangeable. This antenna benefits from its magnetic properties, reducing the influence of disturbances in its near field. Furthermore, it is easily implemented for a differential system, and the need for on- or off-chip baluns is removed (so lower loss).

Furthermore, we have developed a practical design methodology to optimize the PA together with the antenna.

Taking all consideration into account, an antenna meeting the requirements for the application, i.e. $200\ \mathrm{MHz}$ bandwidth with an optimized impedance for both PA and LNA taking only limited space on the PCB, is implemented. If a commercial single ended $50\ \Omega$ antenna is used, the PA/LNA can be connected by making use of a 1:2 balun. The insertion loss of such a balun will degrade the link budget by 1dB.

References

[1] R.C. Johnson, R.C. Johnson, and H. Jasik. *Antenna engineering handbook*. McGraw-Hill series in electrical and computer engineering. McGraw-Hill, 1993.

[2] Freescale Semiconductor. Application Note AN2731, Compact Integrated Antennas. June 2006.

[3] Wikipedia – FR4. http://en.wikipedia.org/wiki/FR-4.

[4] Rogers Corporation – RO3000 Laminate Datasheet. http://www.rogerscorp.com/acm/products/15/RO3000-and-RO3200-series-High-Frequency-Laminates-PTFE-Ceramic.aspx.

[5] Rogers Corporation – RT/duroid 5870/5880 Datasheet. http://www.rogerscorp.com/acm/products/10/RT-duroid-5870-5880-5880LZ-High-Frequency-Laminates.aspx.

6 Conclusion

6.1 Summary of the results

The main focus of the research described in this dissertation lies on low power ranging applications. Since wireless sensor networks are emerging everywhere, location awareness becomes more and more important to realize flexible ad-hoc networks. If mobile sensor nodes gather data, not only this data but information concerning their location is equally important. Furthermore, location information per se can become the sensor nodes main source of information, enabling all kind of tracking applications.

To enable location awareness, an accurate ranging system is needed. Chapter 2 describes different ranging systems. Most of them have low resolution due to bandwidth limitations, or a reduced range due to the high frequencies used. By combining the best of the two, i.e. a lower frequency (2.4 GHz ISM band) while keeping a high bandwidth (250 MHz at RF) to make it multipath resistant, an outperforming ranging system can be obtained. Such a robust system was first built with commercial, of-the-shelf components and shows sub-meter accuracy over up to 500 meter. The work resulted in 3 publications [1–3].

This ranging system was further developed by Essensium, and was deployed in the port of Antwerp where it was demonstrated to work between rows of containers (which give rise to severe multipath reflections) and in

the neighborhood of strong electro motors which drive the cranes and straddle carriers.

Based on the results obtained from the PCB demonstrator, specifications were derived to incorporate the ranging functionality in a system-on-a-chip. This full custom design included the ranging front-end (described in this dissertation), a power amplifier (developed by my colleague Zhisheng Li) and the digital processing (developed by Essensium) to calulate the distance out of the ranging event.

The following chapters of this dissertation mainly focus on the ranging front-end. Chapter 3 presents two different design methodologies to design a low noise amplifier and a mixer. This results in a $10\ \mathrm{mW}$ ranging front-end with a noise figure of less than $7.5\ \mathrm{dB}$, a gain of $28\ \mathrm{dB}$ and a RF bandwidth over $250\ \mathrm{MHz}$. The noise figure and gain are sufficient for a range of more than hunderd meter. The bandwidth ensures submeter accuracy and the power consumption enables low power, battery operated applications.

Chapter 4 presents the design of a lowpass filter used to remove unwanted interference before the following 4-bit analog to digital convertor. By using an improved second order stage, the power consumption, noise and linearity are scaled to an optimum. The implemented 10th order filter has a bandwidth of $130\ \mathrm{MHz}$ ensuring submeter ranging accuracy, and an attenuation of $33\ \mathrm{dB}$ at $225\ \mathrm{MHz}$ to block out nearby UMTS transceivers, further increasing the robustness of the ranging system. This novel filter architecture is published in [4].

Following the baseband filters, an ADC is used to convert the incoming ranging packet to the digital domain. The proof-of-concept PCB showed that the ADC was the most power consumping building block of the receive chain. To reduce the overall power consumption of the receiver dramaticaly, a state-of-the-art ADC was implemented. This ADC comprises a novel comparator design. By reducing the kick-back noise of the comparator, the need for a low impedance driver was no longer needed, and a more accurate calibration was made possible. These features made it possible to design a best-in-class ADC. This work resulted in two publications [5, 6].

Finally, chapter 5 analyzes possible PCB antennas to use in combination with the SoC. The most promising is selected and produced.

The combination of all these building blocks provides a complete ranging receiver front-end, from the antenna to the digital domain and shows the possibility to implement a compact and low cost ranging TRx with submeter accuracy indoors. Such an integrated system opens a new range of

applications in person and asset tracking systems, from automated museum guides to the tracking of firemen in hostile situation, from warehouse automation to tracking hospital equipment.

6.2 Future Work

When different ranging nodes, employing the techniques described in this dissertation, are combined, a complete locationing system can be devised. The quality of such a system can be expressed with a few main parameters: range, accuracy, power consumption and acquisition speed. Each of these parameters can be optimized.

The range is mostly dependent on transmit power, receiver NF and gain. Power amplifiers and low noise amplifiers are still hot topic in literature and new techniques will be also beneficial to ranging systems.

To reduce the power consumption of the ranging system, every building block can be further optimized. With as ultimate goal a device with such a low power consumption that the needed energy can be harvested from the environment, making it completely battery independent. To realize this, further downscaling of the CMOS SoC will be beneficial. It is straightforward that the digital processing will gain tremendously from a lower technology node, but other components will also gain from smaller parasitic capacitances. Further, on the system level, additional power savings can be found. By increasing the mesh density of the different nodes, less transmit power is needed, reducing the need for high power PAs and thus reducing the power consumption of a single device.

To increase the accuracy of a ranging system, correlation methods can be used. Currently the DSP uses threshold detection of the ranging pulse. To increase the accuracy, the shape of the pulse can be taken into account and will give a more accurate indication of the actual arival time. An other approach to extend the accuracy is by combining different location methodes as a set of applications can't be covered by soly one ranging technology. Locationing in hospital settings is such an example. Due to the narrow hallways and small chambers, it is very difficult to determine the room of the tracking device with 100% confidence. Tracking devices near a 10 cm thick wall can be on either side of it. A possible solution to increase the accuracy is integrating the proposed ranging system with a gating system that detects passing of doors via RFID tags. To increase the integration, different locationing techniques can be combined, offering a wide scale of solutions and making it possible to combine the results and information

delivered by these different techniques.

References

[1] X. Yin, J. Bauwelinck, G. Torfs, P. Demuytere, J. Vandewege, H. Tubbax, J. Wouters, P. Debacker, J. Olbrechts, P. Spiessens, F. Stubbe, and J. Danneels. Embedded ranging system in ISM band. *Electronics Letters*, 44(17):1043–1044, AUG 14 2008.

[2] H. Tubbax, J. Wouters, J. Olbrechts, P. Debacker, P. Spiessens, F. Stubbe, J. Danneels, J. Bauwelinck, X. Yin, G. Torfs, and J. Vandewege. A Novel Ranging Technique for 2.4GHz ISM Band. In *The IASTED International Conference on Sensor Networks*, Sept.-Oct. 2008.

[3] H. Tubbax, J. Wouters, J. Olbrechts, P. Debacker, P. Spiessens, F. Stubbe, J. Danneels, J. Bauwelinck, Xin Yin, G. Torfs, and J. Vandewege. A novel positioning technique for 2.4GHz ISM band. In *IEEE Radio and Wireless Symposium*, pages 667–70, 2009.

[4] G. Torfs, Z. Li, J. Bauwelinck, J. Vandewege, and P. Spiessens. A novel large input range source-follower based filter architecture. *IEICE Electronics Express*, 8(24):2025–2028, 2011.

[5] G. Torfs, Z. Li, J. Bauwelinck, X. Yin, J. Vandewege, and G. Van Der Plas. A Low-Power Reduced Kick-Back Comparator with Improved Calibration for High-Speed Flash ADCs. *IEICE Transactions on Electronics*, E92C(10):1328–1330, OCT 2009.

[6] G. Torfs, Z. Li, J. Bauwelinck, X. Yin, G. Van der Plas, and J. Vandewege. Low-power 4-bit flash analogue to digital converter for ranging applications. *Electronics Letters*, 47(1):20–21, JAN 6 2011.