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P. Woestyn, P. Rombouts, X. Xing and G. Gielen

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A selectable-bandwidth 3.5 mW, 0.03 mm^2 self-oscillating Sigma Delta modulator with 71 dB dynamic range at 5 MHz and 65 dB at 10 MHz bandwidth

Pierre Woestyn · Pieter Rombouts · Xinpeng Xing · Georges Gielen

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Abstract In this paper we present a dual-mode third-order continuous time $\Sigma\Delta$ modulator that combines noise-shaping and pulse-width-modulation (PWM). In our 0.18 µm CMOS prototype chip the clock frequency equals 1 GHz, but the PWM carrier is only around 125 MHz. By adjusting the loop filter, the ADC bandwidth can be set to 5 or 10 MHz. In the 5 MHz mode the peak SNDR equals 64dB and the dynamic range 71dB. In the 10 MHz mode the peak SNDR equals 58dB and the DR 65dB. This performance is achieved at an attractively low silicon area of 0.03 mm^2 and a power consumption of 3.5 mW.

1 Introduction

Recently it has been demonstrated that combining time-encoding techniques with $\Sigma\Delta$ modulation provides various interesting features to implement analog-to-digital converters in today's deep submicron technology [1–7]. The main advantage compared to more traditional continuous-time (CT) Sigma Delta ($\Sigma\Delta$) modulators [8], is that the power hungry flash converter is avoided and instead replaced by some explicit or implicit pulse width modulation (PWM) mechanism. Additionally, the multi-bit feedback DAC can be avoided and replaced by a trivial single-bit DAC.

The basic idea is illustrated in Fig. 1 for the case of a 3-bit continuous-time modulator clocked at a frequency f_{s1}. According to the theory of [1], the corresponding PWM $\Sigma\Delta$ modulator should have a carrier frequency f_c of $f_{s1}/2$. Since 3-bit quantization corresponds to 8 PWM-levels, the clock frequency f_{s2} of the PWM $\Sigma\Delta$ modulator should be 8 times higher than the carrier frequency f_C and hence 4 times higher than the original clock frequency [1].

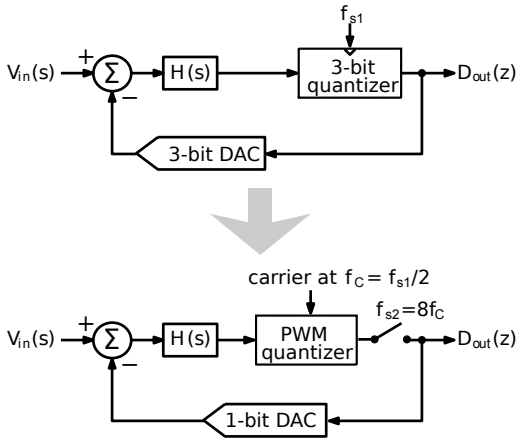

Fig. 1 Illustration of the equivalence between a conventional multi-bit CT $\Sigma\Delta$ modulator (top) and a PWM $\Sigma\Delta$ modulator (bottom).

In our circuit, the clock frequency is set to 1 GHz and the carrier frequency is around 125 MHz. As such our implemented modulator is approximately equivalent to a 3-bit modulator sampled at 250 MHz. However the circuit complexity and silicon area are greatly reduced. Compared to prior work [5], the presented circuit has considerably higher performance due to the incorporation of several innovations. First, we used a third-order loop filter instead of a second-order one. Moreover, the loop filter can be set in 2 modes (i.e. a 5 MHz and a 10 MHz bandwidth mode). In addition to this, we greatly improved the opamps by employing a feedfor-

Pierre Woestyn · Pieter Rombouts
Dept. ELIS, Ghent University (UGent), Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium

Xinpeng Xing · Georges Gielen
Department of Elektrotechniek, ESAT-MICAS, Katholieke Universiteit of Leuven, 3001 Leuven, Belgium

ward structure instead of a conventional Miller compensated structure. In such an opamp the excess poles are compensated by zeros and the resulting dominant pole originates from the capacitive load at the output node. In this way, no power hungry pole-splitting compensation is required. The rest of this paper is structured as follows: Section 2 reviews delay-based self-oscillation, Section 3 describes the system architecture. Circuit details, including the opamp design, are given in Section 4 and the experimental results are discussed in Section 5. Finally, conclusions are presented in Section 6.

2 Delay-based self-oscillating PWM $\Sigma\Delta$ modulator

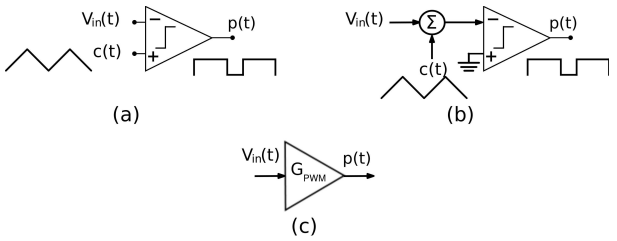

Fig. 2 (a) and (b) Conventional pulse width modulator and (c) its linearized low-frequency model.

Fig. 2(a) shows the conventional basic pulse width modulator, which can be used as the PWM quantizer in the structure of Fig. 1. Here an external triangular carrier $c(t)$ is combined with a comparator. This structure is known to provide a perfectly linear PWM. If the carrier waveform is not triangular (but e.g. sinusoidal), then this structure still performs pulse width modulation, but now the modulation becomes somewhat nonlinear. Obviously this structure is equivalent with the structure of Fig. 2(b), where the sum of the input signal V_{in} and the carrier are applied to the comparator. It is well known that when considering only low-frequency signal components, this system can be modeled by the linearized equivalent system shown in Fig. 2(c) [9].

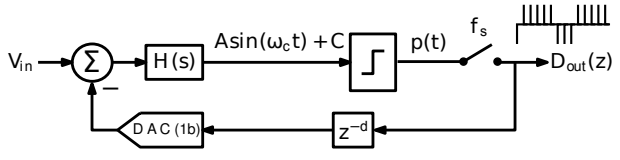

Fig. 3 Basic structure of a delay-based self-oscillating PWM.

Fig. 3 shows the basic structure of a delay-based self-oscillating $\Sigma\Delta$ modulator. It consists of a feedback loop with a continuous time loop filter, a comparator with a zero-order-hold 1-bit feedback DAC and a well-controlled digital delay consisting of d clock cycles in the loop. The loop filter consists of at least one integrator, and hence its DC gain can be assumed to be infinity.

The idea of this structure is to let the system itself generate the carrier $c(t)$ for the PWM. In this way, the input of the comparator will automatically consist of a contribution from the carrier and from the input signal V_{in}. To understand the basic mechanism, let us first assume that the input signal V_{in} is zero. In this case, we want that the output of the loop consists of a stable and well-controlled self-oscillation. In [1], it was shown that a stable self-oscillation will occur at the frequency f_c where the phase shift of the overall loop gain equals 180°. Obviously part of this phase shift will occur in the loop filter while the rest of the phase shift occurs due to the delay in the loop. A particularly simple case occurs when the loop filter is a single integrator, which always contributes a 90° phase shift. In this case, the self-oscillation occurs at the frequency f_c where the loop delay gives rise to the remaining 90° phase shift, which leads to:

$$f_c = \frac{f_s}{4(d+\frac{1}{2})} \tag{1}$$

This equation uses the factor $(d+\frac{1}{2})$ and not just d because the zero-order-hold DAC-pulse also gives half a clock cycle delay, which was neglected in other work [1].

When the input signal V_{in} is non-zero, the self-oscillation will remain and will be superimposed on signal components that are related to the input signal. This is shown in Fig. 3 where the input of the comparator consists of a low-frequency component (the term C) related to the input signal and a relatively high-frequency component related to the self-oscillation (the term $A\sin(\omega_c t)$). This self-oscillation component serves as the carrier for the pulse width modulation in our system.

The pulse width modulated comparator output signal $p(t)$ is then sampled at a very high clock frequency f_s (1 GHz in our case). It is important to realize that the pulse width modulation itself does not introduce quantization noise. The quantization noise originates from the sampling. Due to the sampling the associated waveform can only change at a clock edge and hence the exact transition time stamp is quantized. Fig. 4 illustrates how this mechanism introduces a quantization noise component Q. As is common, we approximate this noise by white noise and its variance can be shown to equal [5]:

$$\sigma_Q^2 = 4\frac{1}{12}\frac{2f_c}{f_s} = \frac{2}{3}\frac{f_c}{f_s} \tag{2}$$

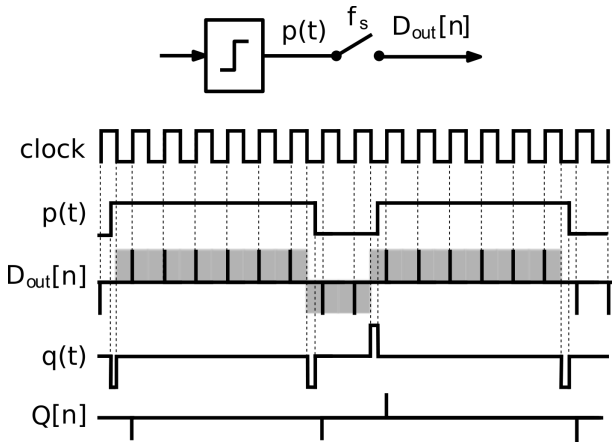

Fig. 4 Sampling induced quantization in a PWM.

Combining this, leads to the linearized system diagram of Fig. 5, which can readily be analyzed.

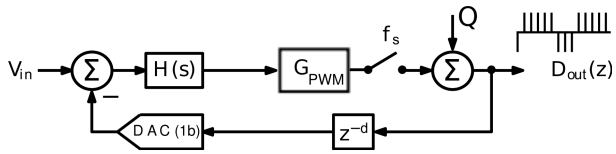

Fig. 5 Linearized delay-based self-oscillating PWM.

3 System design

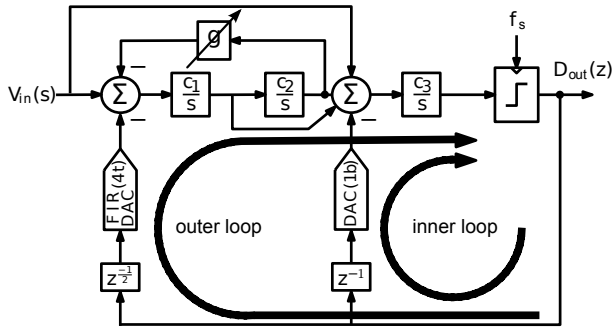

Fig. 6 Block diagram of the self-oscillating $\Sigma\Delta$ modulator.

For our third-order circuit we worked with a 1 GHz clock frequency, which is the maximum we could reliably achieve in the used technology (0.18 µm CMOS). Fig. 6 shows the block diagram of our circuit. Two feedback loops can be distinguished. The inner loop is of first order and is designed to dominate at high frequency. For this purpose the coefficient c_3 is set higher than the coefficients c_1 and c_2. The purpose of this inner loop is to accurately set the self-oscillation. For this purpose 1 explicit clock cycle delay is added. According to Eq. (1) this leads to a self-oscillation at $f_s/6$. But due to some additional gate delay and some additional phase shift (contributed by the outer loop) the actual self-oscillation occurs at $f_s/8 = 125MHz$. The outer loop consists of a third-order loop filter which dominates at lower frequencies (i.e. in the signal band). There is also a local feedback coefficient g for optimized noise shaping. This local feedback coefficient can be set to 2 values corresponding to a 5 MHz and a 10 MHz bandwidth respectively. The outer loop does not need delay, but here we have introduced half a clock cycle delay as well, to relax the settling of the comparator. Also, a uniform 4-tap finite-impulse-response (FIR) DAC is included here.

This filter serves two purposes. First it reduces the jitter sensitivity. Additionally, it reduces the magnitude of the signal that has to be processed by the first integrator in the loop. Finally, a feed-in path from the input is also present to reduce the output swing of the second integrator. With this topology the signal magnitude to be processed by the first two integrators is minimized. The resulting system parameters are shown in table 1.

Table 1 Self-oscillating $\Sigma\Delta$ modulator system parameters

Parameter	value
c_1	2π 25 MHz
c_2	2π 15 MHz
c_3	2π 45 MHz
g	$\frac{1}{6}$ or $\frac{1}{24}$
f_s	1 GHz
f_b	10 MHz or 5 MHz

4 Circuit design

The designed circuit is an RC-active implementation of the system of Fig. 6. The top-level schematic is shown in Fig. 7. The programmable local feedback (corresponding to the g-coefficient in Fig. 6) is implemented with a programmable resistor R_{FB}. The other main building blocks are the switched resistor FIRDAC (detailed in the figure), the flipflops in the FIRDAC and the opamp. The flipflops are custom designed to obtain controlled and matched rise and fall times.

The integrators are formed with active-RC voltage feedback opamps. These opamps should have both a high DC gain and a large output swing, which cannot easily be achieved with a single-stage topology. This way, we used a 2-stage opamp. However to obtain a power efficient design, we avoided power hungry com-

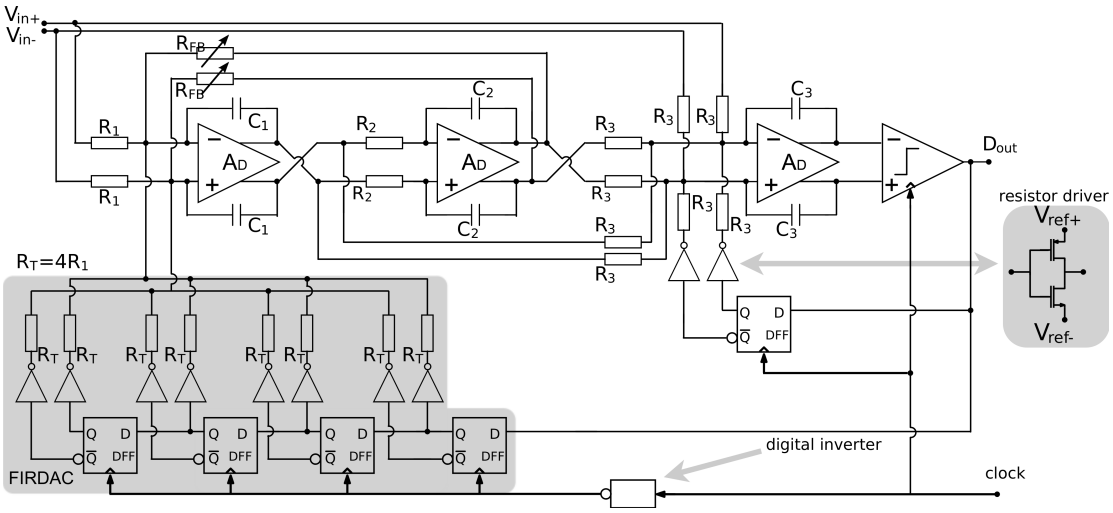

Fig. 7 Top-level schematic of the RC-active implementation of the proposed modulator.

pensation techniques such as Miller compensation. Instead we used a feedforward compensated opamp [10].

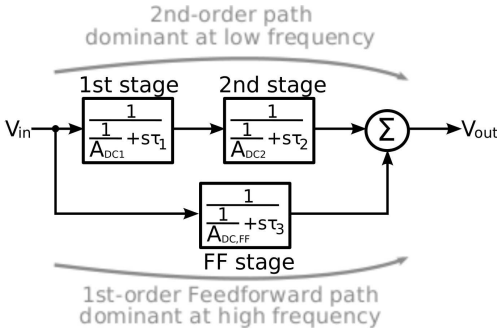

Fig. 8 High-level view of a two-stage operational amplifier with a compensating feedforward stage.

A signal flow diagram of the opamp is shown in Fig. 8. It consists of 3 stages that each have a single pole. Stage 1 and stage 2 are cascaded and sized to dominate at low frequencies. In addition to this, a feedforward stage is added that is sized to dominate at high frequency. The resulting opamp has a DC gain of the order of $A_{DC1}A_{DC2}$ and a unity gain frequency (UGF) of about $\frac{1}{2\pi\tau_3}$.

This is further clarified in Fig. 9 which shows the Bode plot of the overall opamp's transfer function together with its two components. It is clear that the opamp behavior above the corner frequency $f_c = \frac{1}{2\pi\tau_c}$ is of 1st order. Here we have:

$$\tau_c \approx \frac{\tau_1\tau_2}{\tau_3} \tag{3}$$

To obtain sufficient phase margin, it is needed that f_C is well below the opamp's unity gain frequency.

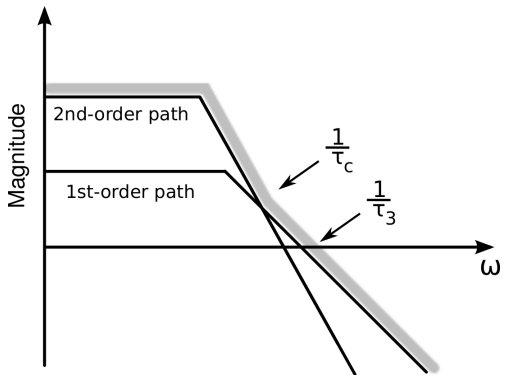

Fig. 9 Magnitude Bode plot of the feedforward opamp's transfer function.

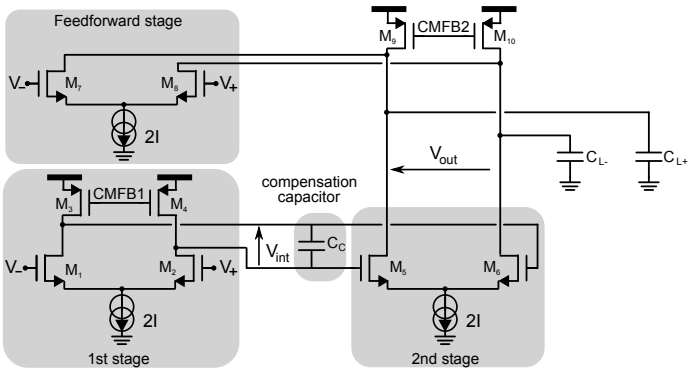

Fig. 10 Circuit implementation of the integrator opamp.

Figure 10 shows the circuit implementation of the opamp. It consists of two input differential pairs and one additional cascaded stage. By inspection of the circuit it is clear that, the circuit's dynamical behavior can be described by the diagram of Fig. 8, and that:

$$\tau_1 = \frac{C_{int}}{g_{m1}}, \quad \tau_2 = \frac{C_L}{g_{m5}}, \quad \tau_3 = \frac{C_L}{g_{m7}}, \tag{4}$$

where C_{int} corresponds to the total capacitance at the internal nodes (drains of M_1 and M_2) and C_L to the load capacitance. To obtain sufficient phase margin we set the corner frequency f_c to one third of the unity gain frequency. To achieve this we had to set τ_1 to a sufficiently large value. This cannot be achieved by simply setting g_{m1} to a small value, because the magnitude of g_{m1} has a lower limit, to avoid that the noise contribution of transistors M_1 and M_2 becomes to large. Therefore an explicit compensation capacitor C_C is added to the internal node, to set τ_1 to the desired (relatively large) value. It is clear that the opamp has no parasitic high frequency poles, which greatly enhances the power efficiency. Note that this compensation strategy has the side-effect that the closed-loop transfer function will have a doublet at f_c. This is undesirable in switched capacitor applications because it gives rise to a slow settling component in the step response [10]. However this is not an important issue in a continuous-time sigma delta modulator. The resulting opamp has a DC gain of 42 dB, a phase margin of 78°, and a unity gain frequency of 1.4 GHz.

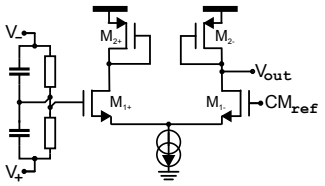

Fig. 11 Common-mode feedback circuit for the integrator opamp.

The opamp also has 2 independent common-mode feedback control loops to set the common mode level at the internal and output nodes. Each common-mode feedback circuit consists of a simple differential pair loaded with diode-connected PMOS transistors, which drive the nodes CMFB1 and CMFB2, respectively (see Fig. 11). A voltage divider is used to sense the common mode voltage. This is implemented as a parallel combination of a resistor and a capacitor. The resistor is sized quite large, not to affect the stage's gain.

5 Experimental results

Fig. 12 shows a micro photograph as well as the floor plan details of the prototype circuit fabricated in a single-poly, six-metal 0.18 µm digital CMOS process. The circuit fits in a rectangle of less than 0.03 mm^2. This includes all the analog circuits, the clock drivers, and a 4-bit shift register. This shift register is used to bring out the single-bit 1 GHz data stream off-chip as

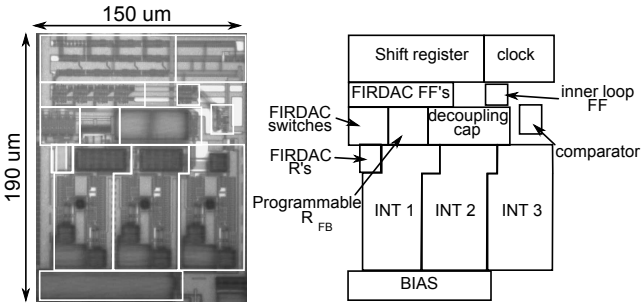

Fig. 12 Micro photograph (left) and floorplan details (right) of the 0.18 µm CMOS prototype.

4 parallel bits at 250 MHz. There is some layout overhead, since a set of roughly rectangular blocks of unequal sized are merged to form a larger block, which inevitably results in some empty area. In our prototype this empty area is partially filled with power supply decoupling capacitance. From the floor plan it is clear that the comparator as well as the FIRDAC take only a minor fraction of the silicon area. This compares favorably to very recently published multi-bit continuous-time $\Sigma\Delta$ modulators [11, 12] where the combination of the multi-bit DAC and multi-bit quantizer takes about half the silicon area.

The total power consumption (excluding the LVDS buffers) is only 3.5 mW from a 1.8 V supply voltage for f_s equal to 1 GHz. About 3 mW of this is consumed in the pure analog blocks (opamp + bias) while about 0.5 mW goes to the digital blocks (FIRDAC flipflops, clock and switch drivers and output shift register). The power consumption of the comparator is negligible (about 50 μW).

Measured output spectra for -2 dBfs input signals are shown in fig. 13. A full scale input corresponds to a sine wave with an amplitude of 1.8 V (i.e. the supply voltages are used as reference voltages in the DAC). A signal frequency of 1 MHz is chosen, such that the 5th harmonic still falls in the signal band in the 5 MHz mode. The top plot corresponds to the 10 MHz mode, while the bottom plot corresponds to the 5 MHz mode. The extended noise shaping for the 10 MHz mode can clearly be observed. Also the peaking of the spectrum at the PWM-carrier frequency (around 125 MHz) is clearly visible.

The distortion is dominated by the 5th harmonic in both cases. In the 10 MHz mode the SNDR equals 58dB and the SNR equals 61dB. In the 5 MHz mode the SNDR equals 64dB and the SNR 69dB. Similar performance was maintained for varying input frequencies (as long as the 5th harmonic still falls in the passband).

Full transistor level SPICE simulations for the circumstances of Fig. 13, predicted a lower distortion for

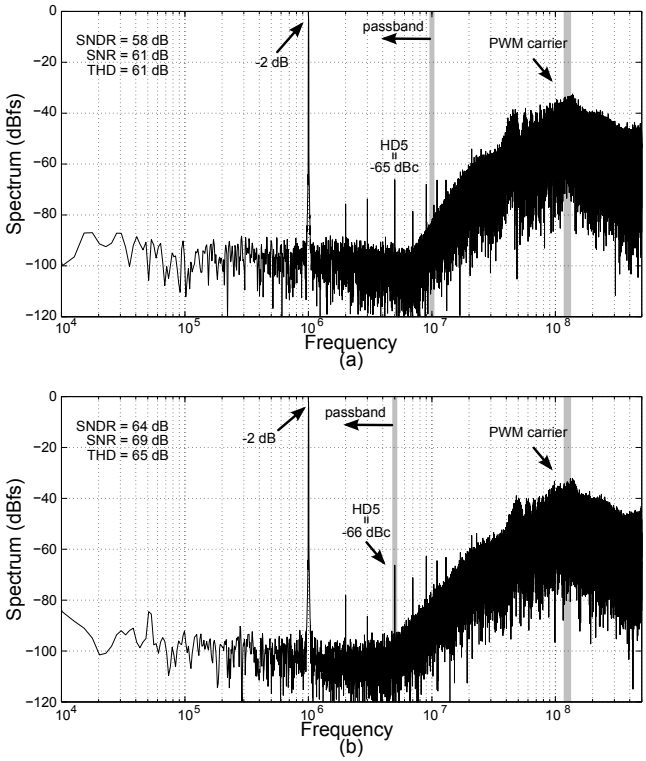

Fig. 13 Measured output spectrum for a 1 MHz, -2 dBfs input signal for the case of (a) 10 MHz bandwidth and (b) 5 MHz bandwidth.

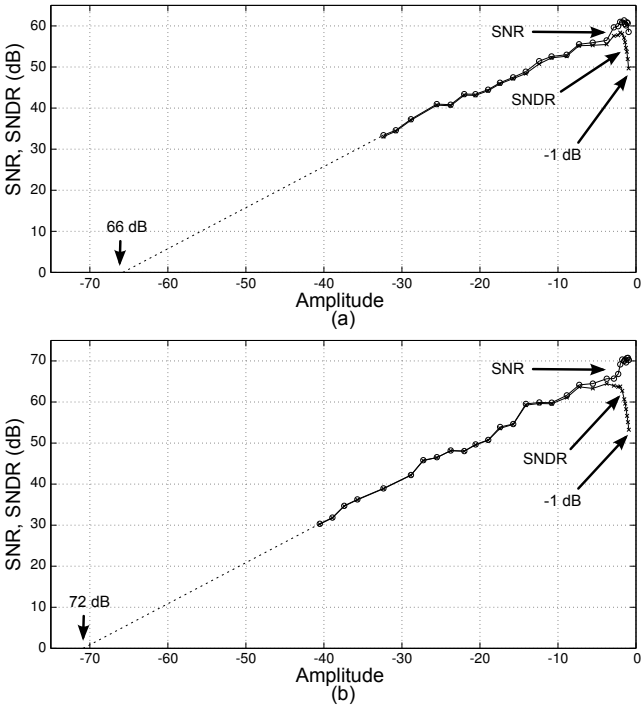

Fig. 14 SNR and SNDR vs. input amplitude measured with a 1 MHz input signal (a) for the 10 MHz mode and (b) for the 5 MHz mode.

Table 2 Prototype performance summary

Technology	0.18µm CMOS
Clock frequency	1 GHz
Bandwidth	5 MHz or 10 MHz
Power consumption	3.5 mW
Dynamic range (DR)	71 dB in 5MHz; 65 dB in 10MHz
Peak SNR	70 dB in 5MHz; 61 dB in 10MHz
Peak SNDR	64 dB in 5MHz; 58 dB in 10MHz
FOM (from DR)	124 fJ per conversion step
FOM (from SNDR)	278 fJ per conversion step
Converter Area	0.03 mm^2

our circuit: i.e. a THD of 84dB in 5 MHz mode and 72 dB in 10 MHz mode. The difference between the measured and simulated distortion is not yet fully understood.

The same measurements were repeated for varying input amplitudes and the corresponding SNR and SNDR plots are shown in fig. 14. From the plots the peak SNR, SNDR and dynamic range (DR) can be obtained for both modes. These values are summarized in table 2. For the 10 MHz mode about 11-bit performance is obtained and for the 5 MHz mode about 12-bit performance. To quickly assess the merit of an ADC design Walden's Figure of Merit (FOM = $\frac{P}{2f_b 2^B}$) is frequently used [13]. This FOM turns out to be identical for both modes. It should be noted that the interpretation of this FOM is not obvious, since it can be shown that this FOM favors low resolution designs [14]. Therefore, this number is only added for illustrative purposes.

Evaluating the linearity of an oversampling converter with single sine wave testing is typically somewhat optimistic. This is due to the fact that the linearity tends to decrease with increasing signal frequency. But if an oversampling converter is tested with a high-frequency input signal, the harmonics fall out of the signal band and are not taken into account. To avoid this problem the high-frequency linearity can be assessed with a 2-tone experiment, where both tones have a frequency close to the passband edge. This way, the intermodulation products are also near the passband edge and form an indication of the high-frequency nonlinearity. The result of such measurements is shown in Fig. 15. It is clear that the linearity performance is adequately preserved.

An additional strong feature of the presented architecture is that the limit cycle is derived from the digital delay in the loop and hence scales well with the clock frequency. As a result the performance is preserved over a large clock frequency range. This is illustrated in Fig. 16, where the peak SNDR is plotted vs. the clock frequency. The plot clearly illustrates the robustness of the proposed scheme. Note that no integrator time constant tuning or trimming was used. It is

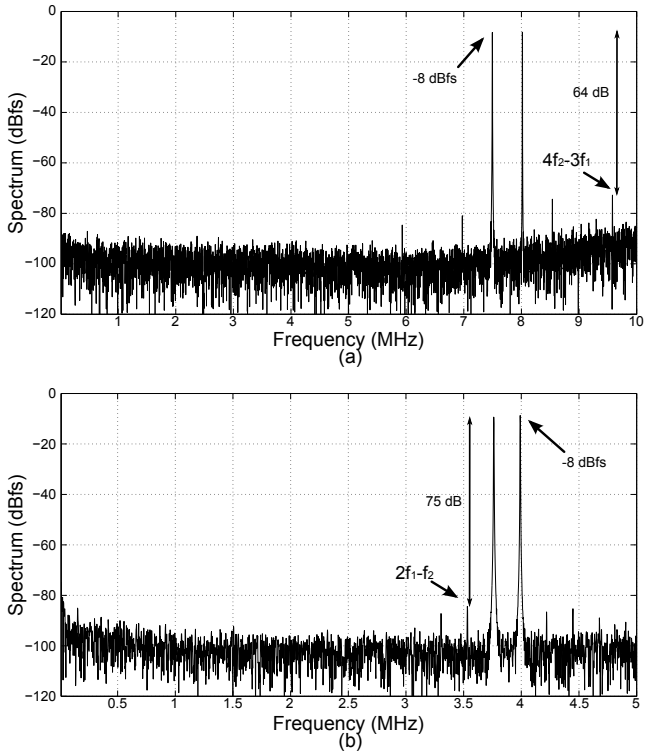

Fig. 15 Measured two-tone signal spectra for the case of (a) 10 MHz bandwidth and (b) 5 MHz bandwidth.

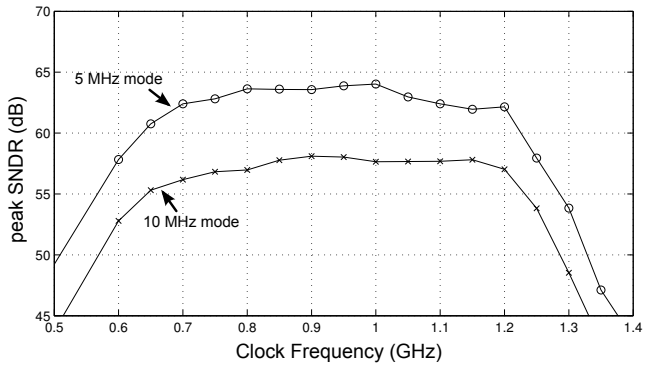

Fig. 16 Measured peak SNDR vs. the sampling clock frequency.

clear that the measured robustness of this pulse width modulation scheme is very good especially compared to comparable conventional continuous-time sigma delta modulators where the time constants must be tuned with an accuracy of the order of a few percents relative to the clock frequency [15].

For low clock frequencies, the performance goes down because the limit cycle comes too close to the signal band and because of overloading problems in the opamps. For high frequencies the performance drops due to settling issues in the opamps and the flipflops of the FIR-DAC.

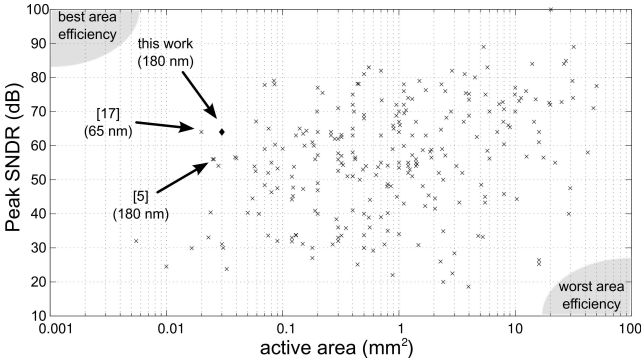

Fig. 17 Area vs. peak SNDR comparison scatter plot based on Murmann's ISSCC and VLSI-symposium data-set [16].

The area of our circuit is compared to other published ADC's from Murmann's data-set [16] in Fig. 17, which shows a scatter plot of the area vs. the peak SNDR. In the comparison only designs with a bandwidth above 1 MHz are taken into account. Also [5] is added to the plot. From the plot, it is clear that our circuit is one of the best designs in terms of silicon area efficiency. It turns out that there is only 1 design [17] that has a slightly better area efficiency than our work. This design [17] is also based on a novel time-encoding technique (different than our work). However, unlike our design, it achieves its linearity only after digital calibration (not included in the silicon area), while our circuit achieves its linearity 'as is'. Moreover [17] is fabricated in 65nm technology (3 technology nodes ahead of our circuit) and hence has a significant technology scaling advantage over our circuit.

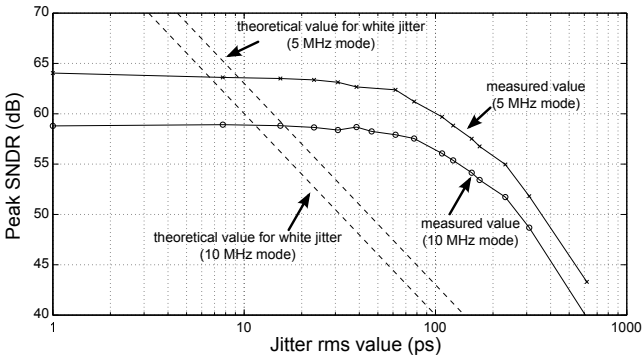

Fig. 18 Measured peak SNDR vs. jitter effective value for a jitter bandwidth of approximately 50 MHz. Also the theoretically calculated value for the case of jitter with a white spectrum (eq. (8) of [5]) is shown.

To test the jitter sensitivity, we modulated our pulse generator (Agilent 81134A) through its delay control input with an external noise source. In our measurement setup the bandwidth of the noise is approximately 50 MHz. Then we varied the jitter rms value and deter-

mined the corresponding peak SNDR. The corresponding measurement result is shown in Fig. 18. It is clear that the performance is maintained up to more than 30 ps-rms jitter. In addition we calculated the theoretical peak SNDR for the case of white jitter eq. (8) of [5] (also shown on the plot). It is clear that the (theoretical) case of white jitter corresponds to a considerably worse situation than the band limited jitter that we have in our measurement setup. Still, even in this case we expect that our circuits can function properly with up to 10 ps-rms of jitter.

6 Conclusion

A dual-mode third-order self-oscillating $\Sigma\Delta$ modulator fabricated in a 0.18 µm CMOS process was presented. The modulator achieves a dynamic range (DR) of 71 dB and 65 dB for a signal bandwidth of 5 MHz and 10 MHz respectively. This corresponds to 12-bit resolution for the 5 MHz mode and 11-bit for the 10 MHz mode. The power consumption of the modulator is 3.5 mW. Moreover this performance is maintained over a wide clock frequency range. The main advantage of this circuit is its simplicity, which translates to a silicon area of only 0.03 mm^2 (excluding decimation filter). This is among the smallest reported until today.

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