Low-Power, Low-Penalty, Flip-Chip Integrated, 10Gb/s Ring-Based 1V CMOS Photonics Transmitter

Michal Rakowski[1], Marianna Pantouvaki[1], Hui Yu[2], Wim Bogaerts[2], Kristin de Meyer[1, 4], Michiel Steyaert[4], Bradley Snyder[3], Peter O'Brien[3], Julien Ryckaert[1], Philippe Absil[1], Joris Van Campenhout[1]

1. imec, Leuven, Belgium
2. Ghent University - imec, Ghent, Belgium.
3. Tyndall National Institute - University College Cork, Cork, Ireland.
4. ESAT-MICAS, K.U. Leuven, Leuven, Belgium.
Author e-mail address: jvcampen@imec.be

Abstract: Modulation with 7.5dB transmitter penalty is demonstrated from a novel 1.5Vpp differential CMOS driver flip-chip integrated with a Si ring modulator, consuming 350fJ/bit from a single 1V supply at bit rates up to 10Gb/s.

OCIS codes: (200.4650) Optical Interconnects; (130.4110) Modulators; (230.2090) Electro-optical Devices

1. Introduction

Ring-based CMOS Si photonics transmitters have been proposed to implement power-efficient optical links to meet the stringent power and bandwidth density requirements that exist for chip-level I/O in future CMOS nodes [1,2]. In this paper, we report on the performance of a CMOS Si photonics transmitter based on a novel CMOS differential drive circuit flip-chip integrated with a depletion-type Si ring modulator. The driver circuit operates from a single 1V supply and is specifically designed to modulate the differential voltage between the anode and cathode of the ring-modulator diode from a forward 0.5V to a reverse -1V, thereby maximizing the extinction ratio (ER) and minimizing the insertion loss (IL) of the Si ring modulator while avoiding the slow carrier dynamics associated with carrier injection. With a 1.5Vpp differential drive swing, a transmitter penalty (TP) as low as 7.5dB has been obtained, which is about 1.5dB lower than for a (single-ended) 1Vpp swing. Using an on-chip programmable pattern generator (PPG), wide open eye diagrams are obtained at 4Gb/s for 340fJ/bit power dissipation, while open eye diagrams are obtained at 10Gb/s using an external PPG. Along with low transmitter power consumption, low TP is key to reduce the overall power of optical links, as a poor TP will either result in higher required laser optical power or higher required receiver sensitivities, both resulting in increased power dissipation.

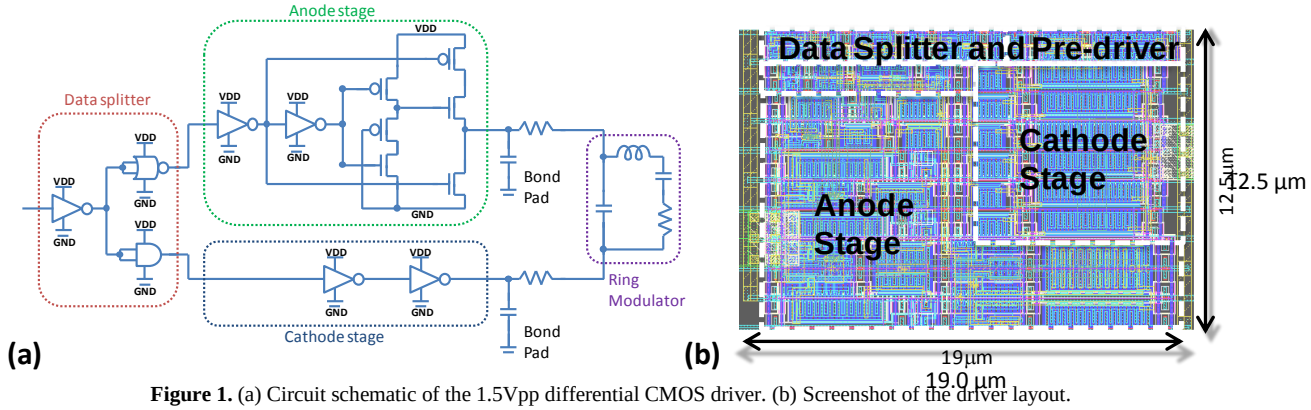

Figure 1. (a) Circuit schematic of the 1.5Vpp differential CMOS driver. (b) Screenshot of the driver layout.

2. Packaged CMOS photonics transmitter: description and fabrication

The CMOS modulator driver schematic can be found in Fig. 1a. The differential drive circuit consists of two dedicated stages: the cathode stage modulates the voltage on the cathode of the modulator p-n diode between 0V and 1V, while the anode stage modulates the anode voltage between 0.5V and 0V, resulting in a differential swing over the p-n diode of 1.5Vpp between +0.5V and -1V. To reduce power consumption, a data splitter is implemented in front of the two output stages. The circuit is sized to drive a nominal capacitive load up to 350fF, at speeds up to 10Gb/s. The driver footprint is 238µm^2, as shown in Fig 1b. The driver has been implemented in 40nm foundry CMOS, along with an on-chip 512-bit PPG, and a 100MHZ-13GHz programmable clock generator based on a phase-locked loop (PLL). Four ring modulator drivers are connected to the on-chip PPG, whereas two additional, stand-alone driver circuits can be driven with external data. The drivers can be configured to either deliver a 1.5Vpp or a 1.0Vpp differential swing, by enabling or disabling their anode stage. The 4-driver array is wired to a dedicated

power supply, such that its power consumption can be accurately measured. All CMOS blocks are controlled by a Network-on-Chip. A microscope image of the CMOS chip, which is about 4mm^2 in size, is shown in Fig 2b. Further details on the CMOS driver and test chip can be found in [3].

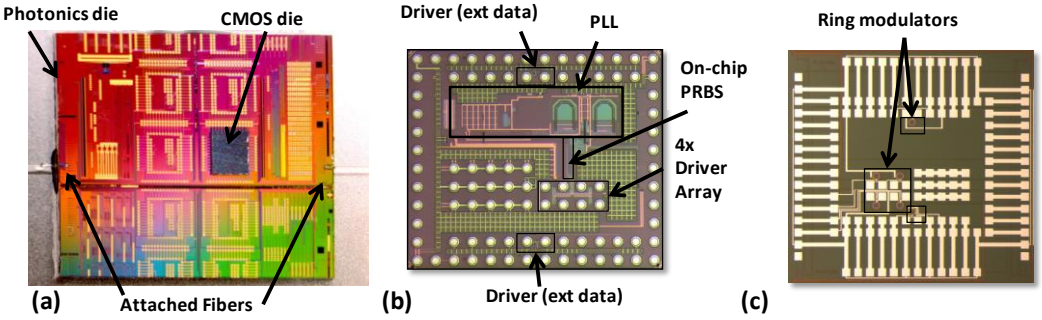

Figure 2. (a) Top view of the CMOS Photonics transmitter, showing the Si Photonics die with attached angled-facet SMF fibers and flip-chipped CMOS driver chip. (b) Microscope image showing the various blocks implemented in the CMOS chip. (c) Flip-chip site on the Si photonics die showing the ring modulators and bond pads.

Fig. 2a shows a top view of the packaged CMOS photonics transmitter. A co-designed Si photonics die containing the Si ring modulators has been fabricated in imec's 200mm pilot line using a subset of 130nm CMOS processing modules. The depletion-type ring modulators have a radius of 40µm, an optical Q factor of 13000, and represent a ~140fF capacitive load to the drivers. The photonics chip is about 1cm^2 in size, and contains grating couplers located at the edge of the chip for surface-normal optical coupling to fiber. For the experiment with integrated PPG, fibers were permanently attached to one of the 4 internally driven ring modulators on the Si photonics chip using a planar fiber-packaging method as described in [4] (Tyndall National Institute, Ireland). Details on the fabrication and performance of the ring modulators can be found in [5].

A conventional flip-chip technique with solder bumps on a 150µm pitch has been used to integrate the CMOS driver chip onto the Si photonics die. The bond-pad capacitance is estimated to be in the range between 100fF-150fF. After flip-chipping, the CMOS die can be electrically contacted through redistribution Cu lines implemented on the Si photonics carrier die, as shown in Fig. 2c.

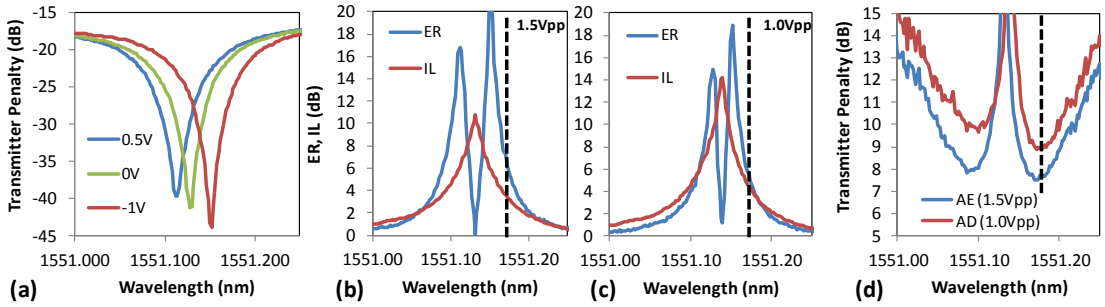

Figure 3. Static transmitter performance. (a) Ring transmission spectra measured for various differential voltages applied by the CMOS driver. Extinction ratio (ER) and insertion loss (IL) for 1.5Vpp differential swing (b) and 1.0Vpp differential swing (c). (d) Transmitter penalty (TP) estimated from static the transmission spectra in (a), for 1.5Vpp and 1.0Vpp driver swing

3. Transmitter performance

First, the static performance was measured of the driver with external data input. The driver's power supply was brought to 1V and static optical transmission spectra were recorded with 0-bit and 1-bit voltage levels at the data input pad. The resulting spectra are shown in Fig. 3a. For a 0-bit with the anode stage disabled (AD), the resonance wavelength is apparent at a wavelength of 1551.152nm. For a 1-bit level, and keeping AD, the resonance wavelength is blue-shifted by 22pm to 1551.13pm When the anode stage is enabled (AE) while keeping a 1-bit input level, the ring spectrum shifts a further 8pm to 1551.112nm. These resonance shifts are very similar to the shifts measured on ring modulators before flip-chip integration when varying the diode voltage between -1V, 0V and 0.5V, validating the static performance of the driver circuit.

From the obtained transmissions spectra, the static ER and IL spectra can be derived. Both are shown for 1.5Vpp (AE) in Fig. 3b and for 1.0Vpp (AD) in Fig 3c. In addition, the transmitter penalty TP, defined as TP = $10\log_{10}$ [(P_1-P_0)/($2P_{in}$)] can be calculated and is shown in Fig 3d. For 1.5Vpp, the TP is as low as 7.5dB at the optimum modulation wavelength, while for 1.0Vpp, the lowest TP is about1.5dB worse at 9dB.

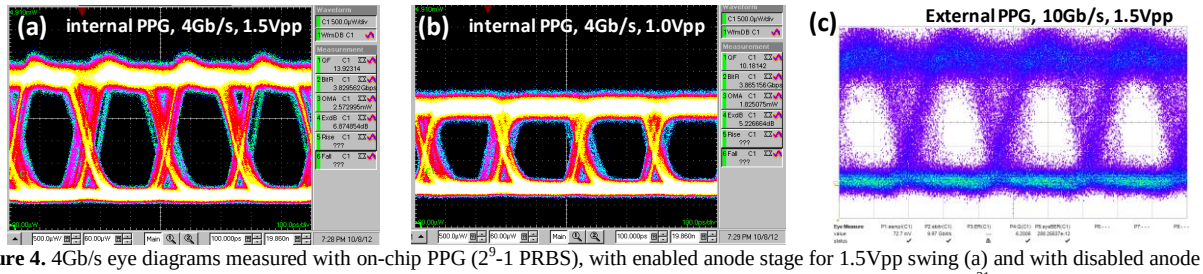

Figure 4. 4Gb/s eye diagrams measured with on-chip PPG (2^9-1 PRBS), with enabled anode stage for 1.5Vpp swing (a) and with disabled anode stage for 1.0Vpp swing (Driver V_{DD} = 1.0V) (b). (c) Preliminary 10Gb/s eye diagrams measured with external PPG (2^{31}-1 PRBS).

Next, the dynamic performance of the transmitter was measured, using one of the transmitters wired to the on-chip PPG. The 512-bit PPG was programmed to deliver a 2^9-1 PRBS data pattern and the PLL was configured to deliver a 4GHz clock signal to the PPG. The power supply of the driver array was kept at 1V. An external laser was tuned to the optimal modulation wavelength, and the modulated light was coupled into the output fiber, amplified by an erbium-doped fiber amplifier (EDFA), filtered and analyzed on a sampling scope with a 30GHz optical module. External amplification was required to compensate for the ~20dB fiber-to-fiber insertion loss, of which 10dB was due to fiber-chip-fiber coupling and 10dB due to optical loss in the 2cm long on-chip waveguide (including 2 waveguide crossings). Eye diagrams were recorded at 4Gb/s for 1.5Vpp (AE) and 1Vpp (AD), and are shown in Fig. 4a, and 4b respectively. Wide open eyes were obtained for both cases, although the AE eye has a larger dynamic ER of 6.9dB and a higher optical modulation amplitude (OMA) of 2.6mW versus ER=5.2dB and OMA =1.8mW for the 1Vpp swing (under identical incoming laser power and EDFA gain). For the AE condition, the power of a single driver was 1.35mW (340fJ/bit), while it was 0.8mW (200fJ/bit) for AD. The performance is summarized in table 1. From the difference in OMA between the AE and AD eyes, the relative difference in TP between AE and AD drive conditions can be calculated to be 1.6dB, in good agreement with the estimation provided by the static measurements. Horizontal eye closure arising from a timing issue prevented us from driving the transmitter at higher speeds. The cause for this excessive jitter is currently being investigated. However, the rise and fall times of the individual traces suggest that the transmitter is intrinsically capable of speeds substantially higher than 4Gb/s. This is confirmed by a preliminary 10Gb/s eye diagram obtained for a ring transmitter with data provided by an external PPG, as shown in Fig. 4c (recorded on a test setup with higher receiver noise).

Table 1 Summary of dynamic modulation performance at 4Gb/s

@4Gb/s, PRBS09, VDD=1V	**Anode Enabled**	**Anode Disabled**	**Difference**	**unit**
Driver swing	1.5	1.0	0.5	Vpp
Driver power	1.35	0.8	0.55	mW
	340	200	140	fJ/bit
ER	6.9	5.2	1.7	dB
OMA	2.6	1.8	0.8	mW
TP (static estimation in Fig 3d)	7.5	9	-1.5	dB

At the optical link level, the higher transmitter power required to obtain the 1.5dB reduction of the TP has to be compared with the power required to either increase the receiver sensitivity or the laser optical power by the same amount. In currently demonstrated Si optical links, link power is dominated by the laser (wall-plug) power, suggesting that the TP reduction will be helpful to lower overall link power consumption. By using smaller ring modulators and micro-bump integration [1], the power overhead for 1.5Vpp swing will be further reduced. Obviously, reducing the optical loss of the other components in the optical link will be equally important.

In summary, a flip-chip packaged CMOS ring-based photonic transmitter with a novel 1.5Vpp differential CMOS driver powered by a single 1V supply has been shown to exhibit a transmitter penalty as low as 7.5dB at 4Gb/s, a 1.5dB improvement over the single-ended 1.0Vpp drive condition. Power consumption was as low as 340fJ/bit. Open eye diagrams were obtained up to 10Gb/s.

This work was supported by imec's Core Partner Program. B.S. and P.O. acknowledge support from Science Foundation Ireland (07/SRC/i1173).

4. References

[1] X. Zheng, et al., "Ultra-efficient 10Gb/s hybrid integrated silicon photonic transmitter and receiver," Opt. Express 19, 5172-5186, 2011.
[2] J. S. Orcutt, et al., "Open foundry platform for high-performance electronic-photonic integration," Opt. Express 20, 12222-12232, 2012.
[3] M. Rakowski et al, " Low-Power, 10-Gbps 1.5-Vpp Differential CMOS Driver for a Silicon Electro-Optic Ring Modulator," in *Custom Integrated Circuits Conference (CICC)*, (IEEE, 2012)
[4] B. Snyder and P. O'Brien, "Planar Fiber Packaging Method for Silicon Photonic Integrated Circuits," in Optical Fiber Communication/National Fiber Optic Engineers Conference (OFC/NFOEC), 2012
[5] M. Pantouvaki et al, "Lateral versus Interdigitated Diode Design for 10 Gb/s Low-Voltage Low-Loss Silicon Ring Modulators," IEEE Optical Interconnects Conference, 2012.