Synthesis and characterization of copper, polyimide and TIPS-pentacene layers for the development of a solution processed fibrous transistor

B. Van Genabet,[1] A. Schwarz,[1,a] E. Bruneel,[2] L. Rambausek,[1] I. Van Driessche,[2] and L. Van Langenhove[1]

[1]*Ghent University, Department of Textiles, Technologiepark 907, 9052 Zwijnaarde, Belgium*
[2]*Ghent University, Department of inorganic and physical chemistry, Ghent University, Krijgslaan 281, 9000 Ghent, Belgium*

A study was performed for the development of a flexible organic field effect transistor starting from a polyester fibre as substrate material. Focus of subsequent layer deposition was on low temperature soluble processes to allow upscaling. Gate layer consists out of a pyrrole polymerization and copper coating step. Polyimide dielectric layer was deposited using dipcoating. Gold electrodes were vacuum evaporated and patterned via mask fibre shadowing. The active layer consisted of a soluble p-type TIPS-pentacene organic semiconductor. Different deposition techniques have been examined. Considerable progress in development of a transistor has been made. *Copyright 2011 Author(s). This article is distributed under a Creative Commons Attribution 3.0 Unported License.* [doi:10.1063/1.3656743]

I. INTRODUCTION

Development of fibrous flexible transistors is required for fabrication of fully integrated flexible electronics. Acting as electrical switches, fibrous transistors would enable to make electrical circuits directly on fabric level using CAD/CAM weaving systems.[1] Furthermore, transistors could also be used as sensor devices, as they are sensitive towards external stimuli such as chemicals, heat and radiation. These influences can alter the charge carrier mobility, which can be measured as a difference in source-drain current. Furthermore, due to their flexibility the ratio between channel width and channel length (W/L ratio) in the transistor could vary enabling functionality as motion sensors.

Another area of application is to be found in the medical field for monitoring, permanent treatment and rehabilitation via electrostimulation.[2] Fibrous transistors integrated on the fabric level could act as switches that activate or disable actuators. They can be used in logical circuits to alter the behaviour of the clothing depending on ambient conditions. It would be possible to measure the temperature of the wearer and activate a heating or cooling system accordingly without decreasing the wearers' comfort by large electronic devices.

The goal of our research is to build an organic field transistor directly on a fibrous polyester (PES) substrate as a cost-effective and flexible base.

In this paper, we described and discuss the solution-based methods that were investigated for application of the gate electrode, dielectric and semiconductive layer. The focus is also put on material choice and obtained layer properties. Above that, we briefly report on the source and drain electrode deposition, for which gold was used. The fibrous transistor set-up is illustrated in Figure 1.

[a]Corresponding author: phone: + 32 9 264 5408; Fax: + 32 9 264 5831; E-mail: Anne.Schwarz@UGent.be
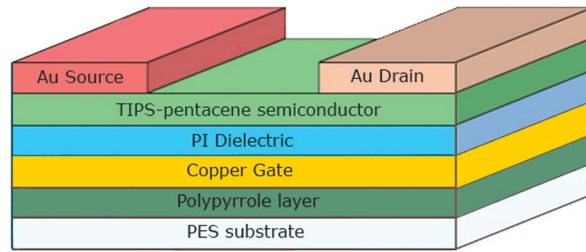
FIG. 1. Schematic representation of bottom gate - top-contact architecture of fibrous organic field effect transistor

II. MATERIALS AND METHODS

PES filaments with diameters ranging from 150 - 888 μm served as substrate material. They were supplied by Teijin.

In a previous study,[3] we already reported that a bottom-gate, top-contact configuration was preferred, as it allows an easier interconnection in textile applications.

A. Gate electrode

Prior to the coating of a polypyrrole (PPy) layer on the PES substrate material, it underwent an extensive washing in a 2 M sodium hydroxide (NaOH) solution at 80 °C for 30 to avoid delamination. The PPy layer formation was based on a polymerization reaction. For that purpose a 0.04 M pyrrole (Py) solution was prepared. An activation solution was prepared in an equal volume containing 0.093 M ferric chloride ($FeCl_3$) as an activator and 0.013 M benzoic sulphonic acid (BSA) as an anionic doping stabilizing agent.[4] Mixing both solutions initiated the reaction. The reaction mechanism of the polypyrrole layer formation is described in[5] and a study on the optimized chemical's concentrations is as reported in.[6] The reaction proceeded at 4 °C, because at higher temperature too many side-branches are formed disrupting the continuous film formation. At lower temperature, in turn, the reaction speed is too slow.[6]

PPy acted as a host material for the deposition of the copper gate layer. Sensitization and activation with a tin-chloride ($SnCl_2$) - palladium-chloride ($PdCl_2$) solution was required. Chemisorption of the palladium (Pd) atoms is favoured on the nitrogen-centra (N-centra) in the polypyrrole chains, because of their high affinity for metal.[7] Tin (Sn) was required to initiate palladium (Pd) chemisorption,[6] but had to be removed in an acceleration step using a 1w% hydrochloric acid (HCl) solution during two minutes. Hence, the chemisorbed Pd-centra acting as a catalyst for the copper (Cu) deposition were exposed. The copper layer was deposited using electroless plating reduction reaction according to.[6]

Copper sulphate and formaldehyde at a respective concentration of 0.04 M and 0.167 M were ideal concentrations for the redox reaction of which the mechanism can be found in Eq. (1). The minimal required pH to activate the formaldehyde half-cell equation was found to be 12.[7] The ideal pH for the reaction had to be determined.

$$Cu^{2+} + 2HCHO + 4OH^- \leftrightarrow Cu^0 + H_2 + 2H_2O + 2HCOO^- \tag{1}$$
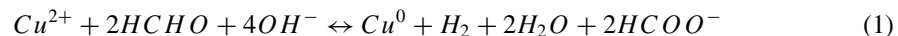
Electrical characterization of the obtained copper layer was done using four-point measurement with flat alligator clamps. Distance between voltage probes was set to 2.5 cm. The resistivity was determined using Pouillet's law as given in Eq. (2). In this equation R is the measured resistance in Ω, ρ is the resistivity in Ω.m, l is the length of the electrode and A is the area for charge transport.

$$R = \frac{\rho l}{A} \tag{2}$$

B. Dielectric layer

The dielectric layer, which will be at the interface with the organic semiconductor, has to fulfil a wide range of requirements. It needs to be isolating to minimize gate leakage, while maintaining

minimum thickness and maximum dielectric constant to exhibit an as high as possible capacitance. A higher capacitance is required to maximize the drain-source current in a transistor with minimal gate voltage, as follows from Eq. (3) and (4) used to calculate the drain-source current I_{DS} in linear and saturation regime, respectively. In these equations, μ_{FE} is the field effect mobility, C_{ox} is the capacitance of the dielectric, V_{GS} and V_{DS} are the gate-source and drain-source voltage, respectively, V_T is the threshold voltage. As the transistor will be in close contact to humans, low working voltages are indispensable. Furthermore, a minimal roughness is required in order to reduce inhomogenities that might act as charge traps decreasing the transistor performance. Polyimide (PI) was chosen as the dielectric material because of good biocompatibility, solution processability, water and common solvent stability, a relatively good dielectric constant and good isolating properties. Dimethylformaldehyde (DMF) and N-methyl-2-pyrrolidone (NMP) were used as solvents. To remove any impurities, samples were pretreated in methanol, followed by extensive drying. The polymeric film was deposited using dipcoating and finally the dielectric layer was formed by evaporating the solvent. The effect of drying conditions on film morphology and electrical properties was examined.

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3}$$

$$I_{DS} = \mu C_{ox} \frac{W}{2L} [V_{GS} - V_T]^2 \tag{4}$$

C. Semiconductive layer

Two types of organic semiconductors can be distinguished, polymeric and small organic molecules. With the latter the highest field effect mobilities have been achieved.[8] Pentacene-based thin film transistors have been reported with mobilities as high as 3cm^2/V.s,[9,10] which is higher than that of amorphous silicon ranging from 0.1-1cm^2/V.s.[8] The main disadvantage is the poor solubility of pentacene molecules in organic solvents at room temperature[11] and therefore the more expensive high-vacuum vapour deposition is mainly used for deposition of pentacene.[12] A lot of research has been focussed on development of soluble organic semiconductors that would allow low-cost solution processing techniques. This has been achieved using permanently functionalized linearly-fused chromophores. Incorporation of substituent in the central positions of chromophores can strongly improve the solubility, while at the same time improving the π-orbital overlap. The substituents take advantage of both steric and π-stacking interactions to induce these chromophores to self-assemble into arrays with strong intermolecular electronic coupling which yields uniform fields with significant long-range crystalline order.[13] Because of its versatile solution processability and high charge carrier mobility, 6,13-bis(Triisopropylsilylethynyl)pentacene (TIPS-pentacene) has been the most intensively investigated compound of all examined soluble small organic semiconductors.[10,14,15] Due to its molecular structure, as illustrated in Figure 2, TIPS-pentacene molecules will form cofacial 2D π-stacked structure with a π-face separation of 3.43 Å and π-overlap of 7.73Å^2.[13,16] This structure leads to relatively high field effect mobilities, generally in the order of 10^{-1} cm^2/V.s with the highest reported field effect mobility for TIPS-pentacene drop casted from a 2w% toluene solution of 1.8 cm^2/V.s.[14,15]

Boiling point and aromaticity are important properties of the solvent for solution processing. Aromatic solvents will solvate the π-conjugated part of the molecule, rather than the substituents as is the case for non-aromatic solvents.[17] Slower solvent evaporation rate encouraged by high boiling point solvents facilitates the growth of highly ordered films and has a positive effect on film morphology.[15,18] In this study, dodecane, tetraline and toluene were explored as solvents.

D. Source and drain electrodes

Electrodes were deposited using vacuum evaporation, both for bottom and gate configuration. The used material was gold, because the work function of this metal (5.1 eV) corresponds very well with the work function of TIPS-pentacene of 5.3 eV.[19] This reduces contact resistance for charge
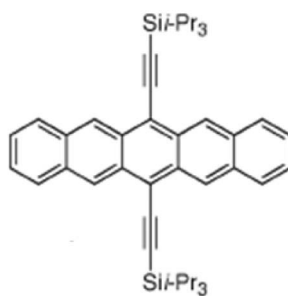
FIG. 2. Molecular structure of TIPS-pentacene

injection. Different masking approaches have been attempted. Fibre masking was preferred because of its applicability in common textile processes.[2] In a metal plate with a thickness of 100 μm a rectangular hole of 600 μm x 1.5 cm was cut using laser ablation. Masking of the channel was done using a filament with diameter of 150 μm.

E. Characterization methods

The layer thicknesses of the various layers were determined using resin embedding and analyzing the cross-section using optical microscopy. The layers' morphologies were analyzed using optical microscopy, scanning electron microscopy (SEM), focussed ion beam (FIB) and atomic force microscopy (AFM).

To evaluate the applicability of the dielectric layer in a thin film transistor, leak current and dielectric measurements were performed. For the former, a gold electrode was sputtered on the dielectric layer. The measurement was done by measuring the current leakage through the dielectric layer at an increasing voltage between the gate copper contact and the gold deposited contact.

Measuring the dielectric properties of an insulating layer were achieved by depositing electrodes directly on the insulating film and by contacting an impedance analyser at these electrodes.

To measure the transistor behaviour on the fibre three contacts have been made. The first circuit made a contact between the gate and the source, the second one between drain and source. The source was therefore at the same potential for both circuits and was grounded and is used as a reference point for the voltage measurements. Two DC sources were needed to generate a VGS voltage to attract the charge carriers towards the dielectric semiconductor interface generating a channel for charge conduction and one to generate the V_{DS} voltage to allow charge to flow from charge to drain. One Ampèremeter was used to monitor leak currents. Another Ampèremeter was applied to measure the drain-source current I_{DS} across the channel layer. The devices used could measure up to an accuracy of 10^{-14} A and could sweep voltages automatically up to -1000 V.

III. RESULTS AND DISCUSSION

A. Gate electrode

The ideal reaction time of the pyrrole polymerization was determined at 180 minutes. If the reaction time was shorter, a thinner and lighter polypyrrole layer was obtained. The subsequent copper coating had a higher resistance and lower reproducibility. A longer reaction time was avoided because of the increased risk of delamination. It was observed that the good polypyrrole layer lead to a decrease of surface inhomogenities arising from the substrate material. Polypyrrole coating was tested on PES fibres with a diameter ranging from 150 to 888 μm. It is concluded that a good polypyrrole layer had been obtained independent of the fibre diameter.

The electroless copper plating proceeded at a solutions pH of 13 for six minutes. As the copper plating reaction is autocatalytic, copper layers are deposited on top of each other, which increases the risk of gas bubbles entrapment at longer deposition times. This would lead to undesired layer delamination.
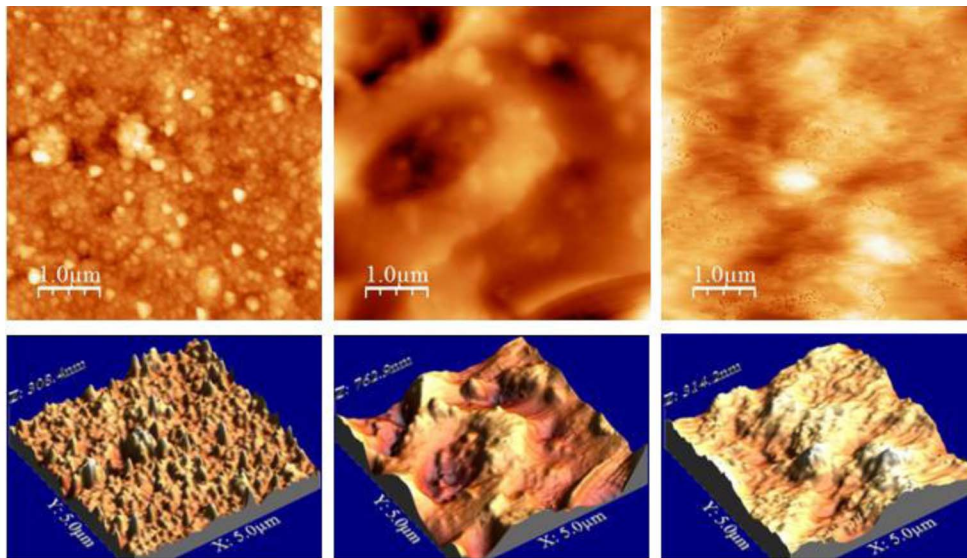
FIG. 3. AFM analysis of the untreated copper layer (left); 15w% PI/DMF-coated sample at 12.5 mm min^{-1} (middle) and 12.5w% PI/NMP-coated sample at 50 mm min^{-1} (right) with the corresponding 3D representations

Assuming a concentric layer model where current only flows through the copper layer resulted in an estimation of $6.5.10^{-7}$ Ω.m for the resistivity. As the resistivity of pure copper is $1.72.10^{-8}$ Ω.m, this increase in resistivity was attributed to impurities and inhomogenities in the copper layer as well as the observation that there is a very close interaction between the copper layer and the polypyrrole layer. It appeared that the copper and polypyrrole layer formed a close hybrid.

Stability of the copper layer was tested over a period of 28 days in ambient conditions. No significant increase in resistance was observed. A stable copper layer had been obtained. AFM analysis revealed that the copper layer had a roughness of 45 ± 1 nm (Figure 3).

B. Dielectric layer

The dielectric PI layer was deposited using DMF-based solutions varying in concentrations from 7.5 to 17.5w%. The layer's thickness appeared to increase with increasing solvent concentration and dip coating withdrawal rate. The leak current decreased with increasing thickness. During drying in ambient conditions a whitening of the dielectric layer was observed. The surface was characterized by a cellular morphology (Figure 4, left photograph) with a roughness in the order of 107 ± 2 nm (Figure 3). Using NMP as a solvent resulted in a transparent film when ambient relative humidity was below 25%. Coating from 12.5w% PI/NMP solution with withdrawal rate of 50 mm min^{-1} and drying at relative humidity resulted in a decreased roughness of 34 ± 5 nm (Figure 3). When the relative humidity was increased, also a whitening of the NMP-based film was observed. This was associated with appearance of a cellular surface morphology. Both NMP and DMF are good solvents for water, which is not a solvent for PI. As follows from the ternary phase diagram of the PI/NMP/water system at low water concentration the mixture stays in the homogeneous region. When the water concentration exceeds a certain threshold value, a phase separation in a polymer rich and polymer lean phase occurs, which is associated with a deterioration of the surface morphology. This phenomenon is described in literature as vapour induced phase separation.[20,21] It was observed that the demixation time of the DMF-based sample to induce vapour induced phase separation was much lower. This indicated the sensitivity of the DMF/PI system towards water is much higher compared to NMP. Drying the samples in an oven at 60 °C ensured a very homogenous layer morphology (Figure 4, right photograph). PI layers produced either in a 15w% NMP or DMF-based solution and a withdrawal rat of at 50 mm min^{-1} had a roughness of 0.375 ± 0.007 nm.
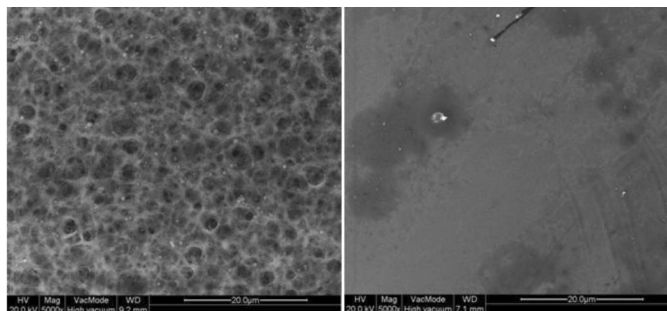
FIG. 4. SEM analysis 15w% PI/DMF solution coated sample at withdrawal rate of 50 mm min^{-1} and dried in ambient conditions (left) and in oven at 60 °C (right)
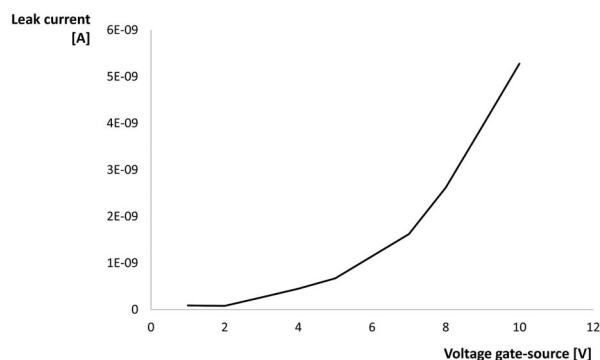

FIG. 5. Leak current for samples coated from a solution containing 15w% PI/NMP at a withdrawal rate of 50 mm/min

Drying conditions had furthermore an important effect on the other parameters of the dielectric layer. Drying at high relative humidity resulted in an increased porosity of the dielectric layer. This resulted in an increased layer thickness and hence in a reduced capacitance and a lower dielectric constant. The reduction in the capacitance was approximately with a factor 10 and was more pronounced when using DMF as a solvent. The leak current also decreased as a result of the porosities and increased thickness. Thin, dense transparent films obtained from a 15w% PI/DMF solution at a withdrawal rate of 50 mm min^{-1} that were dried in an oven at 60 °C resulted in a dielectric layer with the best parameters. The layer was characterized by an estimated capacitance of 31.15 nF cm^{-2}, a thickness of 550 nm and a leak current in the order of 10^{-10} A, when a gold evaporated contact was applied with an area of 74 mm^2, as illustrated in Figure 5. Samples coated at 75 mm min^{-1} from the same solution were used for further experiments because a thickness of 770 nm ensure there was no gate leakage. If dielectric layer thickness was increased more, so did the risk for gate leakage due to the appearance of cracks in the dielectric layer.

C. Semiconductive layer

Pure dodecane, tetralin and toluene were used as solvents with respective boiling points of 216 °C, 207 °C and 110.63 °C. Dodecane had a bad solubility of TIPS-pentacene and was saturated at a concentration below 2w%. Toluene and tetralin are both excellent solvents. Bottleneck at this stage of the research was the deposition of the semiconductive layer on the cylindrical substrate. Wettability of the dielectric layer was tested on a flat substrate. A PI layer that dried in an oven at ambient conditions showed a good wetting of the used solvents. The wetting of the solvents on a PI layer that dried in ambient conditions and underwent a whitening of the film was worse, although they had a better hydrophilicity due to the surface roughness. It was demonstrated the TIPS-pentacene morphology depends strongly on the used solvent by dropcasting on a glass substrate. Using a mixture of 25vol% dodecane and 75vol% toluene lead to larger crystals due to Marangoni
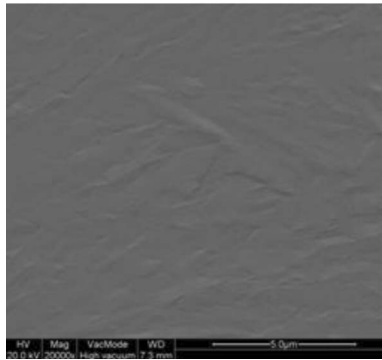
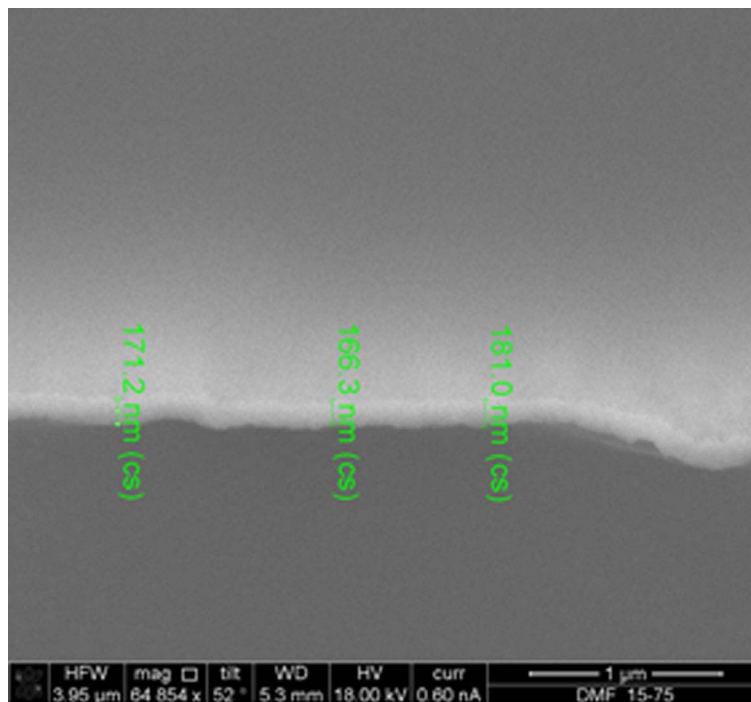FIG. 6. TIPS-pentacene semiconductive layer dipcoated from 2w% toluene solution at 100 mm min[-1]

FIG. 7. FIB cross-section of sample coated with TIPS-penatcene from 2w% toluene solution at 100 mm min[-1]

flow.[10] A homogeneous and crystalline film was obtained from 2w% toluene and 1w% tetralin solution although they both exhibited a ring like behaviour on the periphery known as the "coffee stain" effect. TIPS-pentacene was first deposited using dipcoating. The most homogeneous result was obtained when dipcoating from 2w% TIPS-pentacene/toluene solution at 100 mm min[-1], as illustrated in Figure 6. Thickness was estimated around 170 nm using a FIB cross-section (Figure 7). In order to investigate the transistor properties, the gate voltage was swept from 0 to -100 V, as depicted in Figure 8. It was confirmed that the gate leakage with the used dielectric layer was neglectable. The measured current between the drain and the source was constant over the entire range of V_{GS}, so no transistor effect was observed. The increased current upon increasing V_{DS} could be either the resistance of the semiconductive layer or channel leakage.

Drop casting the solution using a bottom contact configuration was attempted from the different solutions. The resulting semiconductive layer had a poor morphology and it was hard to position the semiconductive layer exactly on top of the channel. Furthermore the wettability on the gold electrodes as well as the dielectric layer was very poor. This was caused by the cylindrical structure,
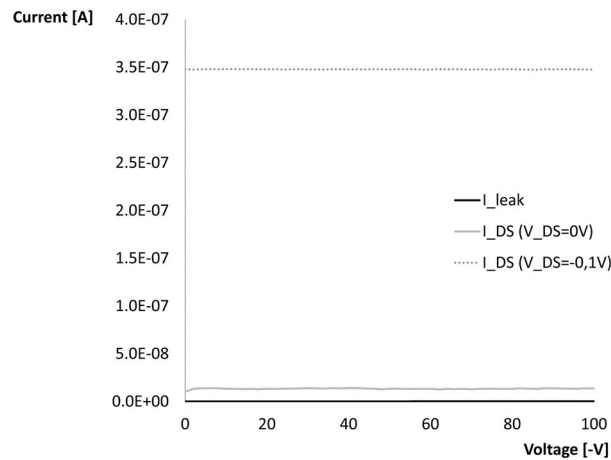
FIG. 8. I-V characteristic of TIPS pentacene deposited from 2w% toluene solution at 100 mm/min using top contacted fibre masking with a resulting channel of 73.1 μm

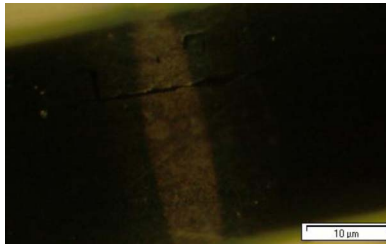FIG. 9. Wettability of the PI dielectric layer before (left) and after (right) corona treatment

FIG. 10. Channel length of 73.1 μm using masking fibre of 150 μm

which made wetting harder than on a flat substrate. It was observed that droplets rolled to the backside of the fibre after a drop had been deposited. As illustrated in Figure 9 wetting was strongly improved using corona treatment. Nevertheless no good semiconductive layer had been obtained. It was attempted to deposit the semiconductive layer directly on the dielectric layer using dropcasting to improve positioning of the channel. During mask application there was a delamination of the semiconductive layer.

D. Source and drain electrodes

Using a fibrous channel mask with a diameter of 150 μm resulted in a channel length of 73.1 μm as illustrated in Figure 10. The channel is smaller than the mask diameter, because the cylindrical masking fibre only makes contact with a relatively small area of the substrate fibre, due to the applied pressure. Using masking fibres with a smaller diameter resulted in a smaller channel length, but the reproducibility to obtain a channel without leakage decreased. Using masking fibres of 150 μm was therefore preferred.

IV. CONCLUSION

The paper describes the synthesis of thin film layers deposited on a PES filament to form a thin film transistor. The main conclusions are:

- A stable DC conductive copper layer had been obtained. Increasing fibre diameter significantly improved reproducibility and conductivity. A fibre diameter of 888 μm was selected for further experiments.
- Deposition of a dielectric layer using dipcoating from either DMF or NMP resulted in a good morphology when dried at 60 °C in dry conditions. Best results were obtained when coating from 15w% PI/DMF solution at 50 mm min^{-1}.
- Gold source and drain electrodes were successfully evaporated and a channel of 73.1 μm was obtained using masking with a fibre of 150 μm.
- TIPS-pentacene was chosen as a semiconductor. Deposition of the semiconductive layer is a major bottleneck in the current research.

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