This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

Multi-Channel 25 Gbit/s Low-Power Driver and Transimpedance Amplifier Integrated Circuits for 100 Gbit/s Optical Links

Jochen Verbrugghe, *Member, IEEE,* Renato Vaernewyck, Bart Moeneclaey, *Student Member, IEEE,* Xin Yin, *Member, IEEE,* Graeme Maxwell, *Member, IEEE,* Richard Cronin, *Member, IEEE,* Guy Torfs, *Member, IEEE,* Xing-Zhi Qiu, *Member, IEEE,* Caroline Lai, *Member, IEEE,* Paul Townsend, *Member, IEEE,* and Johan Bauwelinck, *Member, IEEE*

(Invited Paper)

***Abstract*—Highly integrated electronic driver and receiver ICs with low power consumption are essential for the development of cost-effective multi-channel fiber-optic transceivers with small form factor. This paper presents the latest results of a two-channel 28 Gbit/s driver array for optical duobinary modulation and a four-channel 25 Gbit/s TIA array suited for both NRZ and optical duobinary detection. This research demonstrated that 28 Gbit/s duobinary signals can be efficiently generated on chip with a delay-and-add digital filter and that the driver power consumption can be significantly reduced by optimizing the drive impedance well above 50 Ω, without degrading the signal quality. To the best of our knowledge this is the fastest modulator driver with on-chip duobinary encoding and precoding, consuming only 652 mW per channel at a differential output swing of 6 V_{pp}. The 4 × 25 Gbit/s TIA shows a good sensitivity of −10.3 dBm average optical input power at 25 Gbit/s for PRBS $2^{31} - 1$ and low power consumption of 77 mW per channel. Both ICs were developed in a 130 nm SiGe BiCMOS process.**

***Index Terms*—Driver, driver array, transimpedance amplifier, transimpedance amplifier array, SiGe BiCMOS.**

I. Introduction

EVER increasing energy and bandwidth demands on the current network are driving the need for more advanced opto-electronic subsystems. For cost-sensitive applications, coherent transmission and digital signal processing are not considered as a practical solution. Instead, low-complexity modulation, multiplexing and signal processing are prefered as far as technology scaling economically allows. Applying multiple channels in parallel (e.g. fibers or wavelengths) is an effective approach to increase the system capacity, which can be further enhanced through the application of higher line rates or considering higher modulation schemes, which are still relatively easy to implement in electronics without ADCs and DSP (e.g. duobinary or 4-PAM). Integrating multiple transmitter and receiver blocks together, however, poses a number of challenges. As more circuits are combined on a single chip, the power consumption and power distribution becomes much more critical as the increased power consumption could lead to thermal problems or undesired voltage drops in the power supply nets on chip. As such, reducing the power consumption of all electronic circuits is of major importance, especially when integrating high-swing modulator driver circuits together. We demonstrated this strategy for the first time in a 10 × 11 Gbit/s EAM driver array consuming only 220 mW per channel [1]. As photonic components are often small compared to electronic ICs, especially in case of photodiodes, size constraints on the array integrated electronic channels lead to a number of challenges e.g. impacting power supply decoupling, low-side cut-off frequencies or crosstalk. This reasearch focused on the design of low-power driver and TIA circuits integrated into arrays. Delivering per lane/wavelength line rates of 25 Gbit/s–28 Gbit/s enables low-cost, 4 × 25 Gbit/s approaches to provide 100 Gbit/s connectivity in short-reach, inter-datacentre point-to-point links and metropolitan area networks. As an alternative for the conventional non-return-to-zero on-off keying (NRZ-OOK) format, optical duobinary (ODB) modulation is a good choice for metro-scale applications, since it offers greater chromatic dispersion tolerance, whilst retaining the advantage of simple low-cost direct detection receivers [2]. The reported driver array IC incorporates duobinary pre- and encoding, while delivering a large differential output swing at very low power consumption [3]. To the best of our knowledge such EAM driver arrays are not currently available on the market, whereas the TIA array offers similar performance with respect to the state-of-the-art, but with small footprint.

Sec. II presents the transmitter design, based on the duobinary driver array IC, and its experimental results, followed by a description of the receiver design in Sec. III. BER measurements are presented for both NRZ and duobinary modulation in back-to-back. Finally, Sec. IV gives the conclusions.

J. Verbrugghe, R. Vaernewyck, B. Moeneclaey, X. Yin, G. Torfs, X.Z. Qiu and J. Bauwelinck are with Ghent University, INTEC/IMEC, Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium (e-mail: johan.bauwelinck@intec.ugent.be).

R. Cronin and G. Maxwell are with CIP Technologies, Ipswich, United Kingdom, G. Maxwell now with Tyndall National Institute, Ireland

C. Lai and P. Townsend are with the Photonic Systems Group, Tyndall National Institute, University College Cork, Ireland.

J. Verbrugghe and B. Moeneclaey are supported by a grant from the Institute for the Promotion of Innovation by Science and Technology in Flanders (IWT).

Manuscript received January 31, 2014; revised April 31, 2014.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

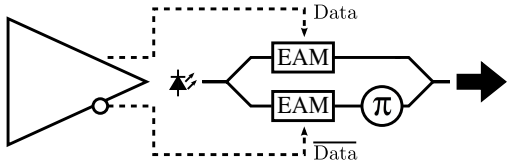


Fig. 1. EAM pair in MZ configuration.

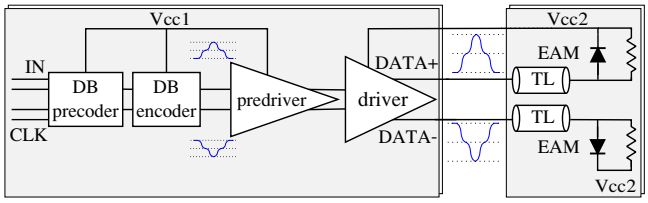


Fig. 2. Block diagram of the 2-channel duobinary driver.

II. Transmitter

A. EAM-based optical duobinary generation

Optical duobinary is a modulation format that is gaining interest in today's optical transmission. Thanks to its narrow optical spectrum, it is less sensitive to chromatic dispersion in long haul single mode links, but it is in fact suitable wherever the available bandwidth is limited, as the required bandwidth is about half that of NRZ. The electrical DB signal has three levels, denoted as -1, 0 and 1, which are translated into two optical intensities. The electrical 0 is transformed into a low optical intensity, whereas a high optical intensity is generated from both an electrical +1 and -1, but with a 180° optical phase difference [4]. In this way a conventional direct detection receiver is still viable in the optical link to detect the data signal. Current duobinary transmitters mostly employ Mach-Zehnder modulators (MZMs). On the other hand an electroabsorption modulator (EAM) pair in an MZ or, in case of reflective EAMs (REAMs), in a Michelson configuration can also be utilized, having the advantage of, firstly, a small form factor, which makes them easier to integrate into an array [5] and secondly, a low modulation voltage, which reduces the power consumption.

The MZ (or Michelson) configuration operates as follows: the positive and negative (three-level) data outputs of the driver are fed to two separate EAMs, of which one is followed by a pi-phase shifter (π), as shown in Fig. 1. The electrical +1 and -1 levels guarantee an output with a large optical intensity as in this case one of both EAMs is transparant and thus turned on. The 180° phase difference is ensured by the pi-phase shifter. In case of an electrical 0, both EAMs transmit a light signal with an equal power, which add destructively due to the pi-phase shifter, giving a low optical intensity at the output.

The three-level duobinary signal is created with a delay-and-add filter, which gives the possibility to adjust the bit rate as desired. The delay is implemented by a D-flip-flops using a clock frequency equal to the bit rate. Generally the encoder is followed by a low pass filter at half the bit rate. Here this functionality is achieved by the limited bandwidth of the driver stage. Due to the encoding, the received signal does not represent the original binary signal. This can be solved by a decoder at the receiver or a precoder at the transmitter. The decoder solution was not chosen for two reasons. Firstly, it can give rise to bit error propagation and secondly, an ambiguity arises due to the initial condition of the duobinary encoder. Therefore a precoder is used, implemented as a frequency divider. In [6] it is proven that the use of a precoder cancels the ambiguity caused by the initial condition.

Fig. 2 depicts the top level block diagram of the driver IC. First the NRZ data signal is converted by the aforementioned duobinary precoder and encoder. A predriver block amplifies the three-level DB signal and drives the large capacitive input of the actual driver. The predriver is directly followed by the driver, which has a configurable modulation current I_M and two configurable bias currents I_B for both positive and negative outputs. In Fig. 2 a pair of EAMs with 50 Ω input impedances is connected to the output through transmission lines (TL).

To reduce the power consumption, different supply voltages are used to operate the different circuits with minimum headroom. The driver stage can be supplied from 4.8 V up to 6.6 V (Vcc2 in Fig. 2), whereas a standard low supply voltage of 2.5 V (Vcc1 in Fig. 2) is fed to all other building blocks.

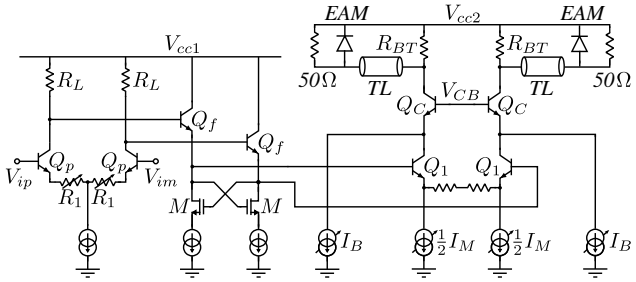


Fig. 3. Predriver (left) and driver circuit (right)

Fig. 3 shows the predriver and driver circuit. The predriver amplifies the duobinary signal to a level of typically 500 mVpp differentially and drives the input of the driver stage. Emitter degeneration resistor R_1 is used to linearize the predriver, because of the three-level duobinary signal. The linearity is however programmable to adjust the position of the cross-points, giving it the possibility to be completely linear. The driver uses a cascode configuration to reduce both the driver output capacitance and the capacitive loading of the predriver output. The driver stage also makes use of emitter degeneration, because of the duobinary signal, it isn't fully linear to keep the power consumption low. The back termination resistors R_{BT} were chosen to be 250 Ω, reducing the power consumption of the driver by 35 % in comparison to the typical 50 Ω back termination resistors.

B. Duobinary eye diagrams

The transmitter has been fabricated in a 130 nm SiGe BiCMOS technology. Fig. 4 shows the die micrograph, with the data path running from bottom to top. The total chip area is 2200 µm × 1200 µm, determined by the number of I/O pads

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

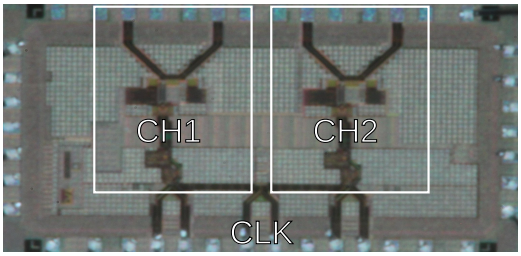


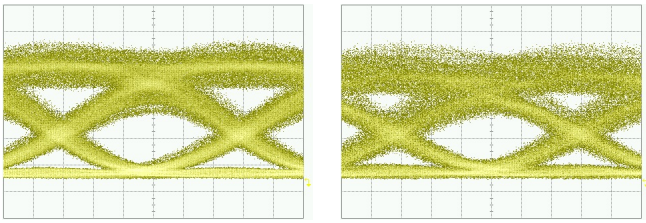
Fig. 4. Micrograph of the 2-channel duobinary driver.

and the 400 µm pitch between the EAM outputs. This gives sufficient room for on-chip decoupling capacitance, which is over 1.2 nF for each supply.

The electrical duobinary eye diagram is shown in Fig. 5(a), measured at a data rate of 28 Gbit/s by multiplexing four PRBS $2^{31}-1$ pseudo random bit sequences (PRBS). With a supply of 6.6 V, a swing of 6 V_{pp} was achieved, while both outputs were biased by the driver at a voltage of 1.5 V below Vcc2. The power consumption of the duobinary coding block was measured to be 127 mW/ch, while the driver consumption was only 525 mW/ch of which 90 mW was consumed externally in the 50 Ω resistors. Per channel this gives a power consumption of only 652 mW.

A smaller differential swing of 3 V_{pp} is shown in Fig. 5(b). Due to the smaller swing, the corresponding modulation current is lower and the supply voltage can be reduced to 4.8 V, resulting in a reduction of the driver power consumption to 198 mW/ch excluding the 127 mW for the duobinary coding. Thanks to the flexibility of the delay-and-add filter implementation, the transmission speed can go as low as 21 Gbit/s, as is shown in Fig. 5(c).

At the time of writing the integrated duobinary transmitter with a Michelson EAM configuration wasn't operational yet. Results of the duobinary driver connected to a dual drive Fujitsu FTM7937EZ MZM are shown in Fig. 6(a) at 25.3 Gbit/s. The creation of ODB with an MZM is similar to that with EAMs in MZ configuration, with the pi-phase shift generated by a correct biasing. In comparison, the eye diagram depicted in Fig. 6(b) is achieved by the EAMs to be used in the assembly. It is generated by configuring the reflective EAMs in a Michelson structure and employing a 7 GHz low pass Bessel filter to achieve the duobinary signal. Both eyes are clearly open.



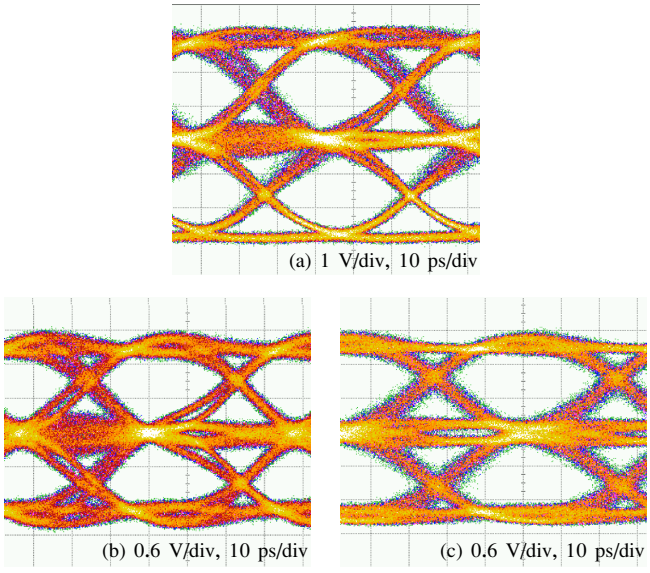
(a) (b)

Fig. 6. Optical duobinary eye diagrams at 25.3 Gbit/s captured with a conventional PIN-PD receiver (440 µW/div, 6.5 ps/div), (a) is generated by the presented driver chip and a MZM (b) is generated by a 7 GHz low-pass filter and EAMs in a Michelson configuration.

When comparing the power consumption to other papers it is important to consider both bit rate and output swing. To make the comparison clearer, a figure of merit (FoM) is defined as the energy per bit divided by the output swing (lower is better). A comparison of the state-of-the-art with low energy consumption is given in Table I.

TABLE I
COMPARISON OF STATE-OF-THE-ART IN ENERGY PER BIT

	FoM	bitrate	tech.	power	swing
	pJ/(bit V_{pp})	Gbit/s		W	V_{pp}
[7]	7.5	40	InP	1.5	5
[?]	6.89	40	GaAs	1.6	5.8
[8]	5.62	40	SiGe	1.35	6
[9]	5.38	50	GaAs	1.4	5.2
[10]	4.58	40	GaAs	1.1	6
work w/ coding	**3.88**	**28**	**SiGe**	**0.652**	**6**
work w/o coding	**3.13**	**28**	**SiGe**	**0.525**	**6**



(a) 1 V/div, 10 ps/div

(b) 0.6 V/div, 10 ps/div (c) 0.6 V/div, 10 ps/div

Fig. 5. Differential electrical eye diagrams: (a) 6 V_{pp} at 28 Gbps (b) 3 V_{pp} at 28 Gbit/s (c) 3 V_{pp} at 21 Gbit/s

III. RECEIVER

A. Topology

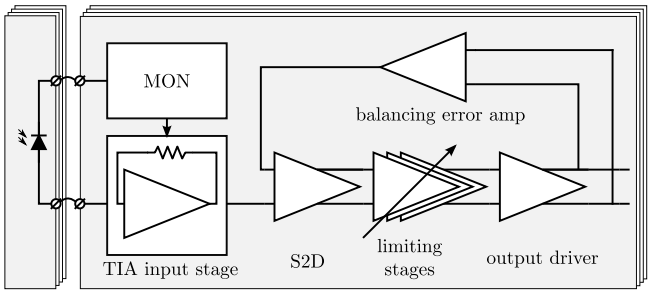


Fig. 7. Block diagram of the 4-channel receiver.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

The major circuits of the receiver assembly are represented in the block diagram, shown in Fig. 7. Light from the fiber array is coupled to the 4-channel photo diode array. For each photo diode, both anode and cathode are bonded to the die in order to mimimize loop inductance and susceptance to interference. The channel pitch equals the photo diode array pitch of 250 µm. The photo diode responsivity (including fiber coupling loss) is 0.41 A/W while its capacitance and series resistance is 115 fF and 10 Ω. respectively. Each channel consists of a transimpedance input stage, a single-ended to differential converter (S2D) stage, three low gain high bandwidth programmable limiting stages and a 50 Ω output stage. A control loop removes the DC-offset between the differential output signals by adjusting the DC-voltage at the inverting terminal of the S2D stage, thus providing balanced differential output signals. The total small-signal differential gain is typically 69 dBΩ. The *MON*-block measures the average photo current and adaptively biases the transimpedance stage, increasing its current sinking capability for larger input photo currents. It also provides a photo current monitor output and supplies a filtered voltage of around 3.25 V to the photo diode cathode. The anode voltage is 900 mV. The *MON*-block can be disabled. The die core runs of a 2 V supply and draws 38.5 mA per channel.

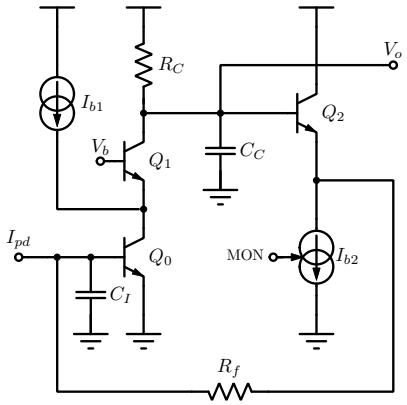


Fig. 8. Simplified circuit diagram of the transimpedance input stage.

Fig. 8 shows a circuit diagram of the transimpedance input stage. Its core is a conventional self-biased shunt-shunt feedback amplifier [11], providing a low-impedance input node. Common-emitter amplifier Q_0, R_C and emitter follower Q_2 make up the forward amplifier, while feedback resistor R_F and C_I, represent the feedback path. C_I is the total capacitance at the input node and includes photo diode, bondpad and TIA input capacitance. Cascode Q_1 protects Q_0 from excessive collector-emitter voltage and reduces its Miller capacitance contribution to C_I. In addition, it provides a convenient low-impedance input for the current source I_{b1}, which provides extra bias current to Q_0. In order to reduce Q_0's base resistor noise, it is necessarily big, leading to increased base-emitter junction capacitance. This calls for higher bias current in order to reduce the transition time through the base and improve the high-frequency response. Current sink I_{b2} both biases Q_2 and sinks most of the photo current. Power consumption is reduced at low input power by adjusting I_{b2} as the monitored DC photo current changes. Conventionally, the output is taken at the emitter of the follower Q_2, which is biased here around 800 mV. However, this would not leave any headroom for the tail current bias source in the S2D stage. Hence the output V_o is located at the collector of Q_1. Care must be taken to keep the capacitance at this node low, as the impedance level is somewhat higher than at the emitter of Q_2. The small-signal input-output transfer function can be approximated as:

$$H = (R_F + \frac{1}{g_{m,2}})\ \frac{T}{1+T} \tag{1}$$

$$T = \frac{T_0}{(1+s/\omega_1)(1+s/\omega_2)} \tag{2}$$

in which T equals the loop gain with low-frequency gain and poles:

$$T_0 = g_{m,0} R_C \tag{3}$$

$$\omega_1 = \frac{1}{R_F C_I} \tag{4}$$

$$\omega_2 = \frac{1}{R_C C_C} \tag{5}$$

Input pole ω_1 is dominant. In order to leave sufficient phase margin and limit time-domain overshoot, care must be taken to place output pole ω_2 at least on the gain-bandwidth product $T_0 \cdot \omega_1$ (GBW). The natural frequency of the resulting two-pole closed-loop transfer function is the geometric mean of ω_1 and ω_2. In this design, some peaking is allowed to increase the bandwidth, and ω_2 is placed two times higher than GBW. The input stage provides 50 dBΩ of gain and has simulated post-layout bandwidth of 22 GHz.

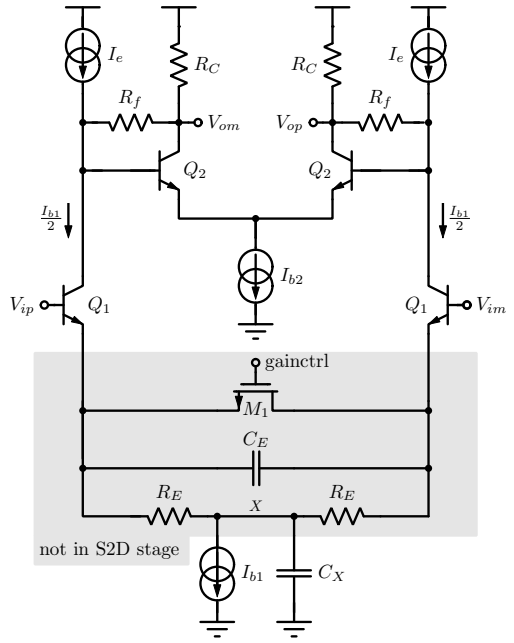


Fig. 9. Simplified circuit diagram of the S2D converter and a main amplifier stage.

The topology of the S2D-stage and main amplifier stages is depicted in Fig. 9. It constitutes a variation of a Cherry-Hooper stage [12], in which a transimpedance amplifier Q_2, R_f, R_C is used as the load of a transconductor Q_1. Usually, simple

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

differential pairs with emitter follower buffers are used in high speed amplifiers. However, the available supply voltage is too low to allow for an extra base-emitter drop while keeping the tail current sources of the subsequent stages in the active region. Moreover, the area requirements of on-chip capacitors precludes the use of AC coupling. As is the case in an emitter follower, the negative feedback in the transimpedance amplifier load reduces the output impedance, effectively decoupling the next stage from the former. In addition, it also presents a low input impedance to the tranconductance stage. Bias sources I_e source a part of Q_1's tail current I_{b1}, limiting the current through R_C. This avoids saturating Q_2 and keeps the DC level of the output nodes high enough to allow for DC coupling. In the three main amplifier stages, fixed resistive and capacitive emitter degeneration (R_E and C_E) is employed to create peaking in the input-output transfer function, hence increasing bandwidth. Furthermore, NMOS transistor M_1 acts as a variable resistance that changes the low frequency degeneration. It is used to program the gain of the stages. Each main amplifier stage has a simulated post-layout bandwidth of over 35 GHz with programmable gain between approximately 2 and 4, resulting in a total main amplifier gain range of 18 dB to 36 dB. As indicated in Fig. 9, the degeneration is not used in the S2D stage. The output signal of the TIA stage is applied to V_{ip}, while V_{im} is driven to same average voltage by the error amplifier of the balancing loop. The data signal is single-ended and travels through both an inverting and non-inverting path to V_{om} and V_{op}, respectively. It can be shown that in the case of an ideal bias tail current source I_{b1}, C_X zero and a perfect symmetrical circuit, both outputs are equal in magnitude but opposite in sign [13]. However, as the capacitive reactance to ground at node X decreases at high frequencies, part of the signal current is diverted to ground resulting in lower gain and excess phase shift in the V_{op} path. This effect is more pronounced when emitter degeneration is included. In order to make the transfer functions from input to both outputs more equal at low and high frequencies, care has been be taken to make the output capacitance of I_{b1} small and degeneration is avoided. Although this results in an earlier onset of clipping, this poses no problem in this application. The S2D stage has a fixed single-ended to differential gain of 3 dB and a simulated post-layout bandwidth of over 35 GHz. The output driver is a conventionial cascoded differential pair with 50 Ω load resistors. Total simulated input referred noise is 2.5 µA rms.

B. Experimental results

The receiver has been fabricated in a 130 nm SiGe BiCMOS technology. Fig. 10 shows the die micrograph. Each channel core occupies 250 µm × 800 µm (including bond pads), with an additional 210 µm × 310 µm for each balancing error amplifier, located at the edges of the chip. The total die size measures 2400 µm × 800 µm. The channel pitch is 250 µm, equal to the photo diode array pitch. Channels 1 and 4 are in the outer lanes, while channels 2 and 3 occupy the middle ones. Furthermore, channels 3 and 4 have extra test circuitry at their outputs. It follows that, even though all channel cores are identical, the topological and electrical differences will impact the respective channel performances. In order to mitigate performance degradation due to crosstalk, both V_{DD} and V_{SS} are electrically isolated for each channel. Other measures include careful use of deep trenches and guard rings.

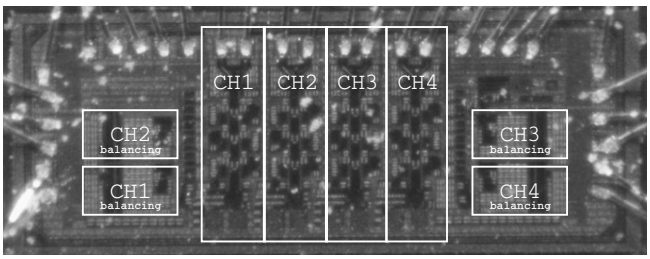


Fig. 10. Micrograph of the fabricated die.

The assembly with fiber array, photo diode array and receiver die is depicted in Fig. 11. The die is placed in a cavity in order to reduce bond wire inductance, in particular of the ground bond wires. Transmission lines fan out radially from the chip to SMP connectors. An aluminium structure holds the fibers in place.

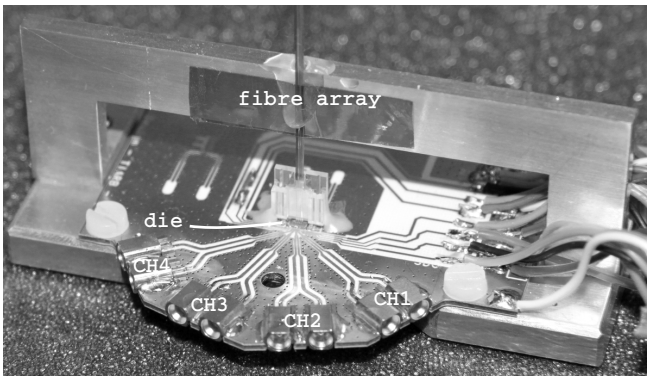


Fig. 11. Photo of the assembled fibers, photo diode array and receiver die.

Measured differential output eye diagrams are shown in Fig. 12 for all channels with the *MON*-block disabled. Input data is PRBS $2^{31} - 1$ NRZ at 28 Gbit/s, with extinction ratio and rms jitter of 14 dB and 950 fs, respectively. Average input photo current is 100 µA. Equipment used is an Agilent 86117A sampling amplifier with an Agilent 86107A precision timebase module to reduce oscilloscope jitter. All eyes are clearly open. The differential output amplitude is 400 mV peak-to-peak, while rms jitter amounts to 1.8 ps for channels 2–4. Channel 1, however, is somewhat noisier. The reason is a lower amount of power supply decoupling capacitance on the die for channel 1, as some of its area has been sacrificed for on-chip test structures. The eye diagrams suggest a high signal-to-noise ratio (SNR) for channel 4, followed by channel 2 with channel 3 marginally worse. The measured small-signal −3 dB bandwidth (using a Agilent lightwave analyzer) is around 14 GHz. This is lower than expected. A possible cause is long input bond wires and we expect higher bandwidth with an improved assembly. It should be noted that the eye diagrams and all further measurements represent the combined performance of the photo diodes and receiver including coupling loss

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

and loss due to on- board transmission lines and connectors. Unfortunately, after the eye diagram measurements, the fiber and photo diode of channel 4 misaligned, reducing the optical coupling to virtually nothing. As a fix would have required dismantling of the assembly, further measurements on channel 4 were not pursued.

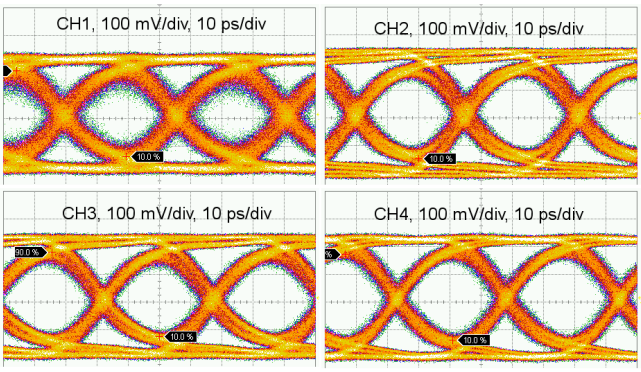


Fig. 12. Measured eye diagrams of channel 1–4 for 28 Gbit/s PRBS $2^{31}-1$ NRZ data, average input photo current 100 µA.

The bit error rate (BER) has been measured using an SHF 12100B pattern generator and SHF 11100B error analyzer using an off-the-shelf transmitter at 25 Gbit/s, in line with the available transmitter and receiver bandwidth. The extinction ratio and rms jitter of the optical input signal was 14 dB and 950 fs, respectively. Fig. 13 shows the BER curves of channel 1–3 for a NRZ PRBS 2^7-1 input signal at 25 Gbit/s. Channel 2 and 3 show a sensitivity of −11 dBm and −10.9 dBm at a BER of 10^{-12}, respectively. In line with expectations, channel 1 infers an extra penalty of 1 dB due to lower power supply decoupling.

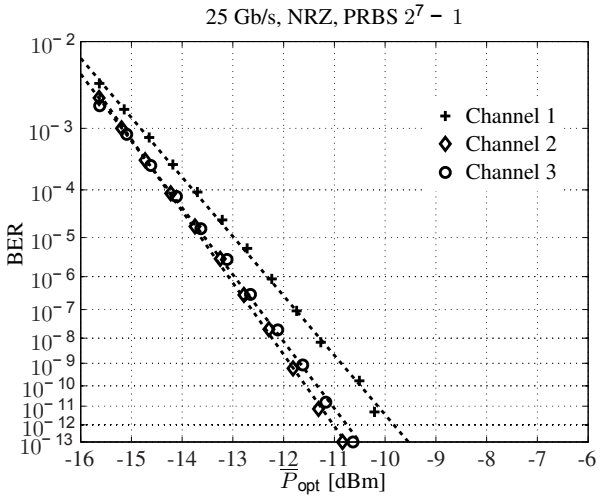


Fig. 13. Measured BER of channel 1–3 for 25 Gbit/s PRBS 2^7-1 NRZ.

Fig. 14 shows the BER for a NRZ PRBS $2^{31}-1$ data pattern at 25 Gbit/s data rate. Compared to PRBS 2^7-1, channel 2 and 3 infer a power penalty of 0.7 dB while the penalty for channel 1 is 2.4 dB. Also measured, but not shown, is the BER for a PRBS $2^{15}-1$ pattern. The results are similar to the results of PRBS $2^{31}-1$. The penalty for longer pattern

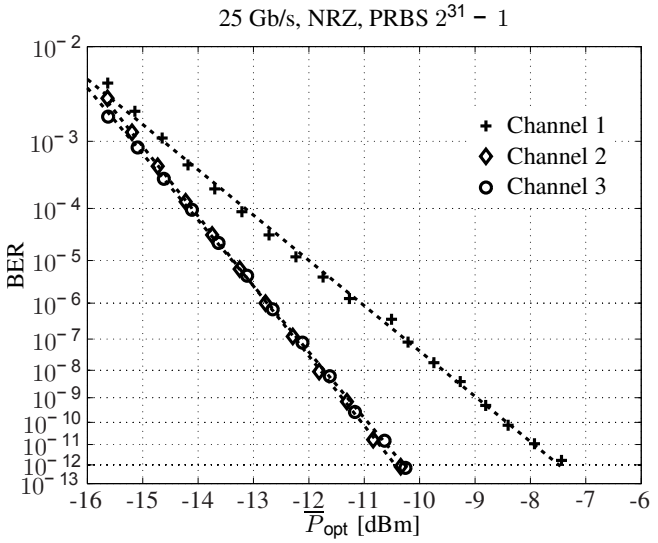


Fig. 14. Measured BER of channel 1–3 for 25 Gbit/s PRBS $2^{31}-1$ NRZ.

lengths is caused by a low-frequency high-pass pole in the data path, introduced by the balancing control loop. This acts similar to AC-coupling, hence causes droop [11]. The low cut-off pole frequency is 500 kHz. The bigger penalty for channel 1 indicates increased influence of the reduced supply decoupling at longer pattern lengths. Hereafter, further measurements on channel 1 are not presented. pass pole in the data path, introduced by the balancing control loop.

TABLE II
POWER PENALTY DUE TO CROSSTALK, 25 Gbit/s PRBS $2^{31}-1$

victim	aggressor	+5 dB	+8 dB
ch. 2	ch. 3	0.5 dB	0.6 dB
ch. 3	ch. 2	0.5 dB	0.6 dB

Crosstalk measurements are presented in Table II for channel 2 attacked by channel 3 and vice versa, for a 25 Gbit/s PRBS $2^{31}-1$ data pattern. The BER performance degradation is shown for an aggressor input power 5 dB and 8 dB higher than the sensitivity of the victim channel. In spite of the small channel pitch of 250 µm, only a penalty of 0.5 dB is observed for the +5 dB attacker. The major contributor to the crosstalk is inductive coupling between the bond wires of the adjacent channels, as the die substrate is high-ohmic and various on-chip isolation measures have been taken (separated supply rails and isolating trenches). This has been confirmed by 3-D field simulations in CST Studio. The extra penalty for the +8 dB attacker is a mere 0.1 dB. This can be explained by recognizing that, even though there is a twofold difference in input powers, in both cases the back-end stages of the attacking channel are limiting. Hence, the extra degradation must be caused by the front-end stages, in which the signals are smaller to begin with.

In addition to NRZ, an optical duobinary back-to-back link has been measured, with the transmitter described in Sec. II. The photo diode acts as an intensity detector. The extinction ratio and peak-to-peak jitter were 9 dB and 13 ps, respectively. Fig. 15 depicts the performance of channel 2 and 3 for 25 Gbit/s PRBS 2^7-1 and PRBS $2^{31}-1$. For PRBS

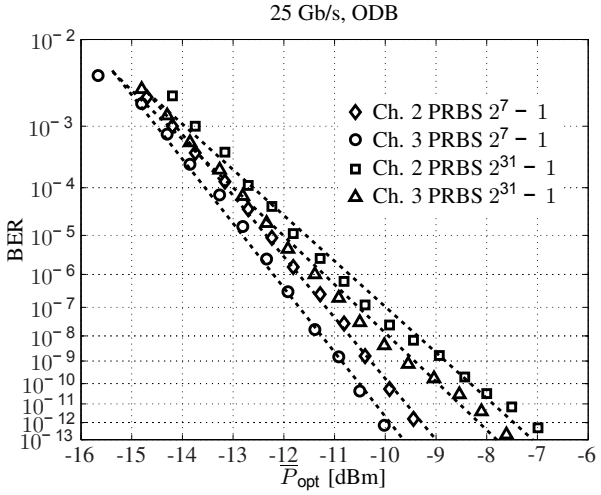


Fig. 15. Measured BER of channel 2 and 3 for 25 Gbit/s PRBS 2^7-1 and PRBS $2^{31}-1$ optical duobinary.

2^7-1, sensitivity is −10 dBm and −9.5 dBm for channel 2 and 3, respectively, indicating a power penalty of 1 dB to 1.4 dB as compared to NRZ signaling. An extra penalty of 2 dB is measured for PRBS $2^{31}-1$. The degradation, particularly pronunciated for the longer data patterns, is caused by the V-shaped eye opening typical for duobinary encoding and non-perfect timing in the transmitter, in combination with limited total system bandwidth.

A comparison with the state-of-the art is given in Table III. For comparable performance with previous receivers, this work obtains tighter integration using a standard 250 µm channel pitch.

IV. Conclusion

With ever increasing bandwidth demands, compact, low-power and low-cost multi-channel transmitter and receiver modules are an absolute necessity to scale up performance. This work focused on the development of a two channel duobinary transmitter and a four channel PIN-TIA receiver array, suited for both NRZ and optical duobinary reception. This research showed that 28 Gbit/s duobinary signals can be efficiently generated on chip with a delay-and-add digital filter and that the driver power consumption can be significantly reduced by optimizing the drive impedance well above 50 Ω, without degrading the signal quality. To the best of our knowledge this is the fastest modulator driver with on-chip duobinary encoding and precoding, consuming only 652 mW per channel at a differential output swing of 6 V_{pp}. The 4×25 Gbit/s TIA shows a good sensitivity of −10.3 dBm at 25 Gbit/s for PRBS $2^{31}-1$ NRZ at low power consumption, 77 mW per channel, while providing a transimpedance gain of 69 dB. The channel pitch is 250 µm. Power penalty due to crosstalk is 0.6 dB for an adjacent aggressor +8 dB higher than sensitivity. BER measurements using the developed transmitter and receiver in a back-to-back link showed a sensitivity of −7.5 dBm to −8 dBm for PRBS $2^{31}-1$ optical duobinary. The ICs were developed in a 130 nm SiGe BiCMOS process and the respective subsystems are being evaluated in a metro system test bed at the time of writing.

Acknowledgment

This work was supported by the EU-funded FP7 ICT Project C3PO and the Special Research fund of Ghent University. We would like to thank the Hercules project VeRONICa for the chip fabrication and Ludo Viaene and Danny Frederickx of IMEC for the chip on board wire bonding. Tyndall's contribution to this work was supported under C3PO and by Science Foundation Ireland under Grant 12/IA/1270.

References

[1] R. Vaernewyck, J. Bauwelinck, X. Yin, R. Pierco, J. Verbrugghe, G. Torfs, Z. Li, X.-Z. Qiu, J. Vandewege, R. Cronin, A. Borghesani, and D. Moodie, "113Gb/s (10 x 11.3Gb/s) ultra-low power EAM driver array." *Optics express*, vol. 21, no. 1, pp. 256–62, Jan. 2013.

[2] P. Winzer and R.-J. Essiambre, "Advanced Optical Modulation Formats," *Proceedings of the IEEE*, vol. 94, no. 5, pp. 952–985, May 2006.

[3] R. Vaernewyck, X. Yin, J. Verbrugghe, G. Torfs, X.-Z. Qiu, E. Kehayas, and J. Bauwelinck, "A Low Power 2x28 Gb/s Electroabsorption Modulator Driver Array with On-chip Duobinary Encoding," *IEICE Transactions on Communications*, to be published.

[4] T. Ono, Y. Yano, K. Fukuchi, T. Ito, H. Yamazaki, M. Yamaguchi, and K. Emura, "Characteristics of optical duobinary signals in terabit/s capacity, high-spectral efficiency WDM systems," *Journal of Lightwave Technology*, vol. 16, no. 5, pp. 788–797, May 1998.

[5] C. P. Lai, A. Naughton, P. Ossieur, C. Antony, D. W. Smith, A. Borghesani, D. G. Moodie, G. Maxwell, P. Healey, A. Poustie, and P. D. Townsend, "Demonstration of error-free 25Gb/s duobinary transmission using a colourless reflective integrated modulator." *Optics express*, vol. 21, no. 1, pp. 500–7, Jan. 2013.

[6] J. F. Buckwalter, J. Kim, X. Zheng, G. Li, K. Raj, and A. Krishnamoorthy, "A fully-integrated optical duobinary transceiver in a 130nm SOI CMOS technology," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, Sep. 2011, pp. 1–4.

[7] Z. Lao, M. Yu, V. Ho, K. Guinn, M. Xu, S. Lee, V. Radisic, and K. Wang, "40Gbits monolithic integrated modulator driver in InP SHBT technology," *Electronics Letters*, vol. 39, no. 16, p. 1181, 2003.

[8] C. Knochenhauer, J. C. Scheytt, and F. Ellinger, "A Compact, Low-Power 40-GBit/s Modulator Driver With 6-V Differential Output Swing in 0.25-um SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1137–1146, May 2011.

[9] K. Watanabe, M. Hashimoto, H. Kudo, H. Uchiyama, H. Ohta, K. Ouchi, and R. Takeyari, "50-Gbit/s AGC and modulator driver amplifier ICs based on InP/InGaAs HBT technology," in *International Conference onIndium Phosphide and Related Materials, 2003.* IEEE, 2003, pp. 370–373.

[10] H. Shigematsu, M. Sato, T. Hirose, and Y. Watanabe, "A 54-GHz distributed amplifier with 6-V/sub PP/ output for a 40-Gb/s LiNbO/sub 3/ modulator driver," *IEEE Journal of Solid-State Circuits*, vol. 2, no. 9, pp. 1100–1105, Sep. 2002.

[11] E. Säckinger, *Broadband Circuits for Optical Fiber Communication*. John Wiley & Sons, 2005.

[12] E. Cherry and D. Hooper, "The design of wide-band transistor feedback amplifiers," *Proceedings of the Institution of Electrical Engineers*, vol. 110, no. 2, p. 375, 1963.

[13] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2002.

[14] J. Proesel, C. Schow, and A. Rylyakov, "25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-based optical links in 90nm CMOS," in *2012 IEEE International Solid-State Circuits Conference*. IEEE, Feb. 2012, pp. 418–420.

[15] J.-Y. Jiang, P.-C. Chiang, H.-W. Hung, C.-L. Lin, T. Yoon, and J. Lee, "100Gb/s ethernet chipsets in 65nm CMOS technology," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2013, pp. 120–121.

[16] T. Takemoto, H. Yamashita, T. Yazaki, N. Chujo, Y. Lee, and Y. Matsuoka, "A 4×25-to-28Gb/s 4.9mW/Gb/s 9.7dBm high-sensitivity optical receiver based on 65nm CMOS for board-to-board interconnects," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2013, pp. 118–119.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2014.2319112, Journal of Lightwave Technology

TABLE III
COMPARISON TABLE WITH PRIOR PUBLISHED RECEIVERS AT A DATA RATE OF 25 Gbit/s PER CHANNEL.

	power	**responsivity**	**sensitivity**[a][b]	**pattern**	**pitch**	**area**	**technology**
	mW	A/W	dBm		µm	mm^2	
[14]	1×44.4	0.55	-4.0 OMA[c]	NRZ PRBS $2^7 - 1$	N/A	0.10	90 nm CMOS
[15]	4×69	0.47	-6.8 OMA	NRZ PRBS $2^7 - 1$	N/A	1.04	65 nm CMOS
[16]	4×137	0.8	-9.7 OMA	NRZ PRBS $2^{31} - 1$	400	6.06	65 nm CMOS
[17]	4×67.5	0.75	-12.6 OMA	NRZ PRBS $2^{31} - 1$	750	4.95	130 nm BiCMOS
this work	$\mathbf{4 \times 77}$	**0.41**	**-10.3 avg. (-7.3 OMA)**	**NRZ PRBS** $2^{31} - 1$	**250**	**1.92**	**130 nm BiCMOS**
			-8.0 avg.	**ODB PRBS** $2^{31} - 1$			

[a]OMA = optical modulation amplitude
[b]BER = 10^{-12}
[c]22 Gbit/s

[17] G. Kalogerakis, T. Moran, T. Nguyen, and G. Denoyer, "A Quad 25Gb/s 270mW TIA in 0.13μm BiCMOS with <0.15 dB crosstalk penalty," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2013, pp. 116–118.

Jochen Verbrugghe (S'10, M'13) received the M.S. degree in computer science engineering and the M.S. degree in electrical engineering from Ghent University, Belgium, in 2007 and 2009, espectively. In 2009, he joined the Intec Design group, where he pursues the Ph.D. degree, working on high speed optical receivers. His current fields of interest are analog circuits, including optical transceivers, continuous time event-driven processing and feedback control systems.

Renato Vaernewyck was born in Waregem, Belgium, in 1987. He received the engineering degree in applied electronics from Ghent University, Ghent, Belgium, in 2010. He has been a research assistant in the INTEC_design Laboratory, Ghent University, since 2010. His research focuses on high-speed, high-frequency (opto-)electronic circuits and systems.

Bart Moeneclaey (S'12) was born in Ghent, Belgium, in 1988. He received the Electronics Engineering degree from Ghent University, Belgium, in 2011 where he is currently working toward the Ph.D. degree. He has been a Research Assistant in the INTEC_Design Laboratory, Ghent University, since 2011. His research is focused on amplifier circuit design for high-speed optical communication systems.

Xin Yin (M'06) was born in Chongqing, China, in 1977. He received the B.E. and M.Sc. degrees in electronics engineering from the Fudan University, China, in 1999 and 2002, respectively, and the Ph.D. degree in electrical engineering from the Ghent University, Belgium, in 2009. Since 2007, he has been a researcher in IMEC-INTEC/Ghent University. He is also collaborating in European and International projects such as DISCUS, Phoxtrot, MIRAGE and GreenTouch consortium. His current research interests include high-speed opto-electronic circuits and subsystems, with emphasis on burst-mode receiver and CDR/EDC for optical access networks, and low-power mixed-signal integrated circuit design for telecommunication applications. He is author or co-author of more than 50 national and international publications, both in journals and in proceedings of conferences.

Guy Torfs (S'07, M'13) received the M.S. and Ph.D. degree in electrical engineering from Ghent University, Belgium in 2007 and 2012 respectively. From 2007 on, he has been working at the INTEC_design laboratory associated with imec and part of the department of information technology at Ghent University. His research interests include high speed and RF electronics, mainly focused on frequency synthesis and clock and data recovery.

Xing-Zhi Qiu (M'98) received the Ph.D. degree in applied sciences, electronics from Ghent University, Ghent, Belgium in 1993. She joined the department of information technology (INTEC) of Ghent University in 1986. She gained 27 years R&D experience within INTEC_design laboratory in the field of high speed O/E/O front-ends and physical layer hardware design for broadband optical networks in general and burst-mode receiver/transmitter technologies for passive optical networks in particular. She has been strongly involving in many EU-funded projects, and managing high speed opto-electronic analog/digital chip/sub-system designs within IMEC-INTEC/Ghent University. She is author or co-author of more than 150 publications and 6 patents on ASIC and telecom system designs.

Caroline P. Lai (S'07, M'12) received the B.A.Sc. degree (with Hons.) from the University of Toronto, Toronto, ON, Canada in 2006, and the M.S. and Ph.D. degrees from Columbia University, New York, NY, in 2008 and 2011, respectively, all in electrical engineering. She is currently a Postdoctoral Researcher in the Photonic Systems Group at Tyndall National Institute, Cork, Ireland. Her research interests include energy-efficient photonic technologies and cross-layer optimized communications for future optical access and metro transport networks, in addition to optical interconnection networks for high-performance computing systems and datacenters. She is a member of the IEEE Photonics Society and the OSA.

Johan Bauwelinck (M'02) was born in Sint-Niklaas, Belgium, in 1977. He received the engineering degree in applied electronics and the Ph.D. degree in applied sciences, electronics from Ghent University, Ghent, Belgium, in 2000 and 2005, respectively. He has been a research assistant in the INTEC_design laboratory, Ghent University since 2000, and he is currently a full-time tenure track professor. His research focuses on high-speed, high-frequency (opto-) electronic circuits and systems and he is a member of the ECOC technical program committee.