True high-order VCO-based ADC

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This document is an author's draft version submitted for publication in ELectronics Letters.
The actual version was published as [1].

REFERENCES

[1] A. Babaie-Fishani and P. Rombouts, "True high-order VCO-based ADC," *Electron. Lett.*, vol. 51, no. 1, pp. 23–U53, Jan. 8 2015.

A true high order VCO-based ADC

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In this brief, we present a novel approach to use a VCO as the first integrator of a high order continuous time Delta Sigma Modulator. In the proposed architecture, the VCO is combined with a digital up-down counter to implement the first integrator of the continuous time Delta Sigma Modulator. This way, the first integrator is digital friendly and hence can maximally benefit from technological scaling.

Introduction: In most cases, in Continuous Time Delta Sigma Modulators (CT-DSMs) the first integrator is the bottle neck in terms of power consumption and noise. In deep-submicrometer processes, this block is becoming more and more difficult to implement in the voltage-domain due to the limited voltage headroom and gain of narrow channel transistors. For this reason, there is an increasing interest in VCO-based ADCs. Here, an integrator is based on a voltage controlled oscillator (VCO) which is typically implemented as a ring oscillator. Such a ring oscillator consists of a loop of inverters controlled by a current-mode or voltage-mode signal. Therefore they are a very good option for digital friendly technologies. One of the main issues with current VCO-ADCs with a VCO input stage is that they can only provide 1st order noise shaping. There have been a few attempts to increase the order by using multi-loop mash approaches [1, 2], but these techniques are very sensitive to analog imperfections [1].

A notable attempt to obtain a single-loop high-order VCO ADC which uses a VCO as the first integrator is [3]. However, this approach suffers from a high complexity and power consumption, and additionally it has high sensitivity to the center frequency of the VCO which makes this idea impractical. In this work, we will construct an alternative, very general technique for high-order ADC's with a VCO input stage and indicate how its simplest form can be implemented by adding a well established Phase Frequency Detector (PFD).

Proposed Scheme: First, we will start from a basic structure of a VCO-ADC, and then we will step by step transform it into the new ADC structure. Fig. 1*a* shows the basic structure of a VCO-ADC which consists of a VCO and a reset counter [4]. The VCO converts the input voltage, V_{in}, to a square wave of which the frequency is proportional to the input voltage. Then the reset counter counts the number of rising edges of the square wave in every clock cycle. This way, it quantizes the phase which is the integral of the frequency. The reset function compensates this integration with an inherent differentiation. Apart from the quantization error, the resulting digital output signal D_{out} will be equal to:

$$D_{out} \approx \frac{f_{vco}}{f_s} = \frac{f_c + k_{vco} V_{in}}{f_s} \tag{1}$$

where f_{VCO} stands for the VCO output frequency, f_c for the free running (zero input) frequency of the VCO, k_{vco} for the gain of the VCO and f_s for the sampling frequency.

An equivalent system is depicted in Fig. 1*b*, [4]. In this alternative structure the integration and differentiation functions (which previously happened simultaneously in the reset counter) are separated. After the VCO there is an up-counter which counts the rising edges of the output waveform of the VCO (the integration), and after sampling, the output is differentiated in the digital domain. Of course this implementation of a VCO-ADC is only conceptual , because in practice the output signal of the up-counter would go to infinity. In a next step, the differentiator in Fig. 1*b* can be replaced by a feedback loop with an integrator, which results in Fig. 1*c* and which is still strictly equivalent to Fig. 1*a*. Now that we have managed to create a loop in the digital domain, we can extend the loop and bring it to the analog domain using a zero order hold DAC, as in Fig. 1*d*.

In order to have a balance in the terminology in the analog and digital domain, an integrator in the digital domain can be called and viewed as an "up-counter". Since the output of the two up-counters are being subtracted from each other, we can combine the two and call it an "up-down counter", as in Fig. 1*e*. This "up-down counter" functions as follows: at every rising edge of the VCO, its output is incremented by one. At every rising edge of the clock the counter output is decreased by the value D_{out} of the register (which will normally be multibit). By using a Return to Zero (RTZ) pulse, every rising edge of the clock also occurs in the feedback signal such that the up-down counter is now triggered by edges at both its inputs. We will come back to the implementation of such an asynchronous digital block later on.

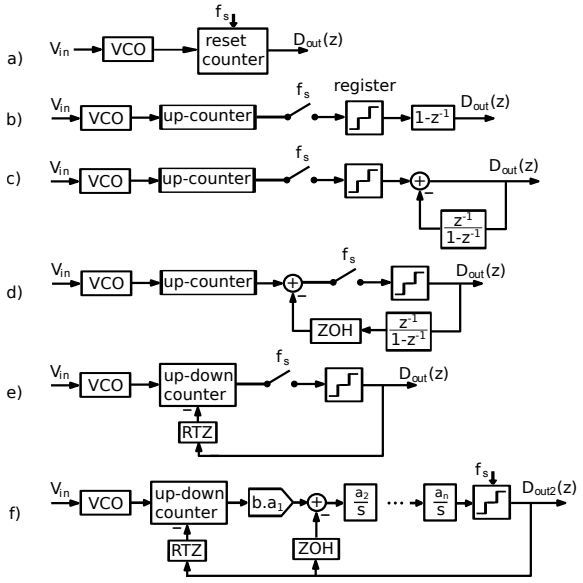

Fig. 1 *Metamorphosis of a first order VCO-ADC to a multi-order one.*
a the basic structure of a VCO-ADC
b An equivalent system with up-counter and digital differentiator
c replacing the differentiator with an integrator in the feedback
d extending the loop from digital to analog domain
e replacing the up-counter and the integrator with an up-down counter
f increasing the order of the proposed VCO-ADC

We have already discussed that an up-down counter, from a system level point of view, behaves as an integrator; so we can clearly see that the system proposed in Fig. 1*e* is a first order Sigma Delta Modulator. The output of this up-down counter doesn't go to infinity, in fact it's a limited pseudo digital integer number. However, since it can change at the rising edge of the VCO wave form, it is not synchronous with the sampling clock. In fact the information is partially stored in the position of the edges. This signal can be referred to as a "multi-level PWM" waveform. Note that the structure of Fig. 1*e* is still strictly equivalent to Fig. 1*a-d*.

Now that we have managed to redraw the VCO-ADC as a feedback loop, the next and final step is to increase its order by introducing additional integrators in the loop, Fig. 1*f*. It is clear that the resulting structure can be of any order. Its first integrator is implemented by the combination of the VCO and the up-down counter, and hence is digital friendly and suitable for integration in today's deep submicrometer CMOS. The second and later integrators are still in the analog domain, but their implementation is very relaxed because their errors are reduced by the gain of preceding integrators. Moreover, particularly the second integrator has a pseudo digital input and can be realized using a set of charge-pump integrators (switched current sources and a capacitor) [5]. Local feedbacks to create notches in the Noise Transfer Function (NTF), as in conventional CT-DSMs, can also be integrated into this scheme.

Summarizing, the proposed structure is equivalent to a conventional CT-DSM with the same integration coefficients, a_i (see Fig. 1*e*), provided that the design is scaled according to the following equations:

$$f_c = \frac{f_s \cdot (2^{n_{bit}} - 1)}{d}, \quad k_{vco} = \frac{f_c}{V_{ref}}, \quad b = \frac{2 \cdot V_{ref}}{2^{n_{bit}} - 1} \tag{2}$$

Here n_{bit} stands for the number of bits in the quantizer, or alternatively $2^{n_{bit}}$ for the number of levels in the quantizer. The parameter b scales the integer output of the up-down counter to the full scale of the system. The full scale voltage is defined by the reference voltage and equals $\pm V_{ref}$.

Simulation Results: Some typical system level simulation results are shown in Figures 2 and 3. Here the modulator is a 3rd order single bit design with a Butterworth NTF and a $h_\infty = 1.6$ and a local feedback to create a notch in the NTF. Fig. 2*a* shows the output spectrum for the conventional modulator for the case of a -14dBfs input signal. The results for the corresponding new structure of Fig. 1*f* are shown in Fig. 2*b*. It is clear that the output spectra for both cases are nearly identical.

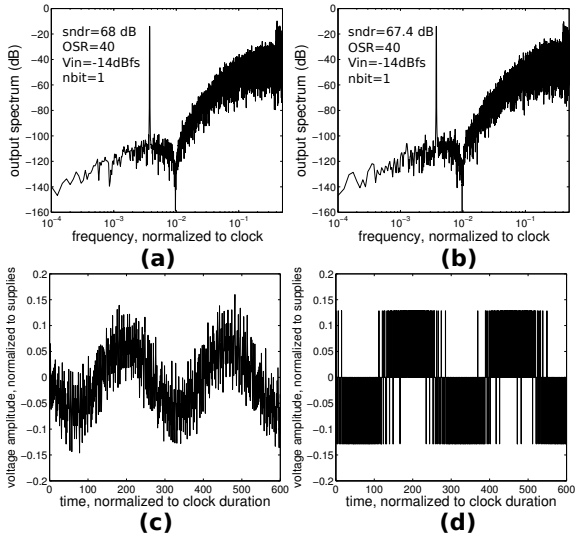

Fig. 2 *Simulation results of two 1-bit CT-DSMs with a -14dBfs input tone.*
a output spectrum of a conventional 3rd order modulator
b output spectrum of a VCO-based modulator with the same NTF
c output signal of the first integrator for the conventional modulator
d output signal of the first integrator for the VCO-based modulator

A look at the internal waveforms of the two modulators, however, shows that they have a completely different time-domain behaviour. Fig. 2*c* and *d* compare the output signals of the first integrators of the two ADCs. As it was previously explained, the output of an up-down counter is a multi-level PWM signal, which is in this case a 3-level signal, Fig. 2*d*. Despite this obvious difference in the internal waveforms, the two modulators maintain almost identical spectral integrity.

The amplitude of the main tone (corresponding to the input signal) at the output of an integrator in a CT-DSM (be it conventional or VCO-based), which is normally the dominant contribution at these nodes, is proportional to the amplitude of the input signal. Therefore, an increase in the input voltage will increase the signal level at these nodes too. In the case of the proposed VCO-ADC, this higher swing would translate to a higher number of levels.

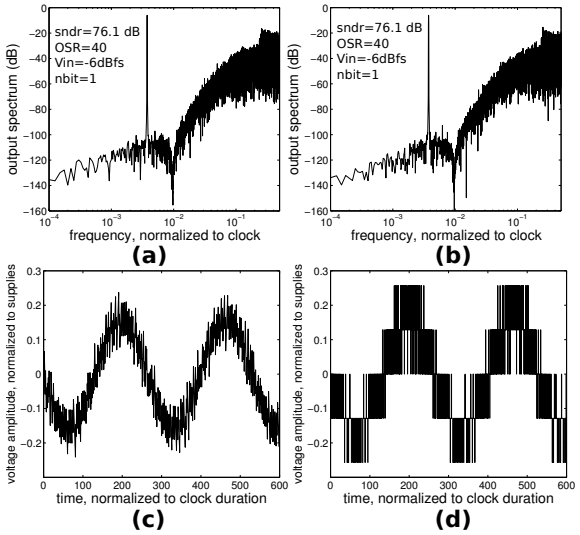

Fig. 3 *Simulation results of two 1-bit CT-DSMs with a -6dBfs input tone.*
a output spectrum of a conventional 3rd order modulator
b output spectrum of a VCO-based modulator with the same NTF
c output signal of the first integrator for the conventional modulator
d output signal of the first integrator for the VCO-based modulator

For Fig. 3, a higher input amplitude ($-6dB$ instead of $-14dB$) is used. Again the overall output spectra are almost identical. As Fig. 3*c* shows, for the conventional CT-DSM, the voltage swing at the internal node has clearly increased. The equivalent node for the VCO-based CT-DSM, Fig. 2*f*, also shows an increase in the signal swing, except here a higher swing simply means that more levels are used in the PWM waveform.

Implementation considerations: The proposed structure has a VCO input stage and as such it is directly affected by VCO's nonlinearity. However, there are a several ways to solve this problem, including PWM pre-coding [4, 5] and post calibration [6].

Another imperfection that can be associated with a VCO is inaccuracy in its carrier frequency f_c and its voltage to frequency conversion gain k_{vco}, but these imperfections in the VCO don't impose any problem on the proposed scheme. Any error in f_c will be translated to a mere DC offset in the output and an error in the value of k_{vco} can be viewed as a gain error for the overall modulator.

The most important new block is the up-down counter which is triggered by edges at its both inputs. This way, this is basically an asynchronous circuit and in general its implementation can be challenging. However, its design can be greatly simplified by using a single bit quantizer (as was done in the simulations of Fig. 2 and 3). An additional important parameter is the signal swing at the output of the up-down counter. This swing can be controlled either by appropriately scaling the modulator coefficients or by restricting the modulator's input range. In the particular case that the output swing is only three-level (as in fig. 2*b*) the up-down counter collapses to the well known Phase-Frequency Detector (PFD) which is widely used in PLL's and for which efficient implementations are well known. If a higher swing is needed, some additional logic of similar complexity as a PFD is needed.

Conclusion: We have proposed a novel system structure for a true high order VCO-ADC where the VCO is the first and hence most important integrator of a CT-DSM. It uses a digital up-down counter, which in combination with the VCO acts as the first (and most important) integrator of the continuous time delta sigma modulator. The up-down counter can have many implementations and we have indicated how in some cases it can even be very simple. However, whichever implementation is used, it will always be a fully digital block and hence can maximally benefit from technological scaling.

Acknowledgment: This work has been supported by the Fund for Scientific Research Flanders (FWO-Vlaanderen) Belgium.

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