

Demonstration of Silicon-on-insulator mid-infrared spectrometers operating at 3.8 μ m

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Abstract: The design and characterization of silicon-on-insulator mid-infrared spectrometers operating at 3.8 μ m is reported. The devices are fabricated on 200mm SOI wafers in a CMOS pilot line. Both arrayed waveguide grating structures and planar concave grating structures were designed and tested. Low insertion loss (1.5-2.5dB) and good crosstalk characteristics (15-20dB) are demonstrated, together with waveguide propagation losses in the range of 3 to 6dB/cm.

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1. Introduction

While silicon photonic waveguide circuits were originally conceived to be used for datacommunication and telecommunication applications, a myriad of other application domains have emerged in recent years, including the use of these waveguide circuits for sensing applications [1] and biomedical instrumentation [2,3]. Just like in datacommunication applications, the rationale for realizing these functions on a silicon photonics platform is related to the maturity and scalability of the CMOS fabrication technology used to fabricate these photonic integrated circuits, which can lead to low-cost advanced photonic integrated circuits. Typically one holds on to the 1.3-1.55 μm wavelength range also for these non-communication oriented applications. However, spectroscopic sensing applications, which allow analyzing the content of gas or liquid samples of interest by probing their absorption spectrum, would benefit from the extension of the wavelength range supported by the silicon-on-insulator material platform. Research in this direction has started over the few last years, first by addressing the short-wave infrared wavelength range up to 2.5 μm , both for linear [4] and nonlinear optics [5] applications. Silicon however is optically transparent up to 8 μm , which allows to dramatically extend the wavelength range of operation of the platform [6]. This is beneficial for spectroscopic sensing applications, since the absorption cross-sections of the molecules of interest become much stronger in the mid-infrared (2.5-8 μm). In this paper we present the first integrated mid-infrared spectrometers realized on silicon-on-insulator, fabricated in a CMOS pilot line, targeting the 3.8 μm wavelength range. This wavelength range lies close to the edge of the transparency window of the buried SiO₂ layer [7], which defines the actual transparency window of the silicon-on-insulator material platform. The developed spectrometer can find applications in future integrated spectroscopic sensor systems, in miniature spectroscopic telescope systems (given the atmospheric transmission window of 3-5 μm) or as a wavelength multiplexer for future quantum cascade / interband cascade laser light engines.

2. MidIR silicon photonics technology

We used two slightly different material platforms for the fabrication of midIR silicon photonic waveguide circuits in a CMOS pilot line: the *imecAP* and *imec400* process. *ImecAP* is a multiple project wafer run service (MPW) offered by imec, Belgium through ePIXfab [8]. In the *imec400* process we used dedicated CMOS processing for the waveguide fabrication. The detailed fabrication process is explained in the following sub-sections.

2.1 ImecAP

The *imecAP* process starts with 200mm SOI wafers with 220 nm of crystalline silicon (c-Si) on top of 2000 nm of buried oxide. First 5 nm of thermal SiO₂ is grown after which 160 nm of amorphous silicon (a-Si) is deposited using a low-pressure chemical vapor deposition process. The 5 nm of thermal SiO₂ serves as protective layer for the underlying c-Si during the waveguide etching. On top of the a-Si 10 nm of SiO₂ and 70 nm of SiN are deposited using plasma enhanced chemical vapor deposition process. This SiN layer serves as a hard mask for the waveguide etching and as a polish stop layer during the chemical-mechanical planarization of the wafer. The wafer stack is then annealed at 750 °C for 30 minutes, which converts the a-Si to poly-silicon (p-Si). This step is performed in order to increase the temperature budget for eventual post-processing on the silicon wafer. This wafer stack is used

for waveguide circuit fabrication using 193nm deep UV lithography and halogen based dry etching. Figure 1 schematically shows the wafer-stack fabrication steps.

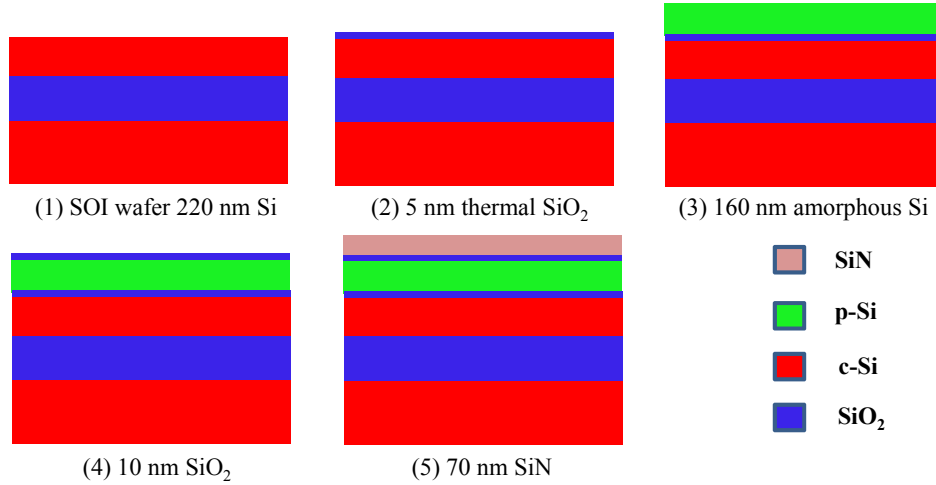


Fig. 1. Schematic view of wafer-stack fabrication by layer deposition (drawings are not to scale).

To define a waveguide in the Si device layer that is 380 nm thick (160 nm p-Si and 220 nm c-Si) different etch steps are available. For the waveguides presented in this paper we make use of single step 160nm etch and a two-step 380 nm etch (in a first step the 160 nm poly-silicon is etched while in a second step the 220 nm c-Si layer is etched after removal of the thin SiO₂ intermediate layer). As a 193nm lithography stepper tool is being used the alignment accuracy for two etch step process is better than 50 nm. Additionally, a 230nm etch step is available for parts of the photonic integrated circuits, such as the grating couplers and distributed Bragg reflectors in the planar concave grating spectrometers.

After etching the photoresist is stripped and a blanket layer of SiO₂ is deposited using a high density plasma process. After this deposition chemical mechanical planarization is performed to flatten the topography. This planarization process stops on the 70 nm SiN mask. Now this SiN is stripped off using hot phosphoric acid and 800 nm of blanket SiO₂ layer is deposited again to serve as top cladding for the waveguide circuits. Also now a flat top surface is achieved which is desirable for some post-processing e.g. the bonding of III-V semiconductor material on top for light sources or photo-detectors. This lies however outside the scope of this paper. The *imecAP* process is offered in a multi-project wafer run service, which allows the cost-effective fabrication of mid-infrared photonic integrated circuits alongside conventional near-infrared circuits. Figure 2(a) shows a representative scanning electron microscope (SEM) cross-section of a waveguide realized in this advanced passive platform, with the associated mode profile at 3.8 μ m plotted in Fig. 2(d).

2.2 Imec400

The *imec400* process uses 200mm SOI wafers with a 400 nm thick crystalline silicon device layer on top of 2000 nm of buried oxide. A thermal oxide/LPCVD SiN stack is used as a hard mask for the waveguide definition, similar to the *imecAP* process. This pattern is further transferred to the underlying 400 nm Si using selective dry etching through the complete device layer stack. After waveguide etching the SiN hardmask is stripped. No top-cladding is applied in this case. Figure 2(b) shows a bird's eye SEM view of an imec400 waveguide. The mode profile is shown in Fig. 2(e).

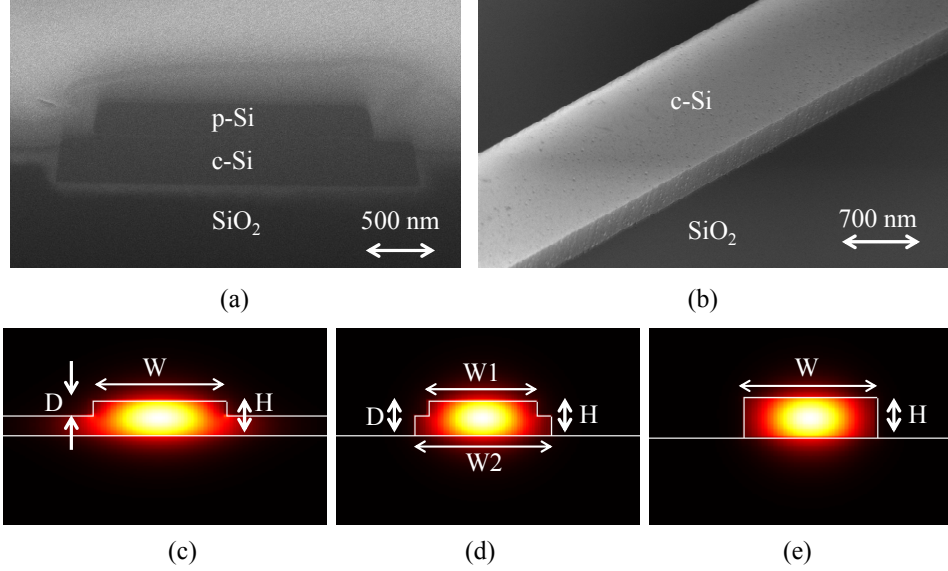


Fig. 2. (a) Representative SEM cross-section image of a waveguide structure implemented in the *imecAP* process where top oxide is partially etched for better imaging; (b) a bird's eye view of an *imec400* waveguide structure; (c-d) mode profile of the *imecAP* waveguide cross-sections; (e) mode profile of the *imec400* waveguide cross-section. Actual dimensions for waveguides are given in section 3.1.

3. Spectrometer design and measurements

Single mode waveguides as well as two types of spectrometers (arrayed waveguide gratings and planar concave gratings) were realized in both the *imecAP* and *imec400* processes. The waveguide circuits were characterized using grating coupler based fiber-chip interfaces connected to input and output ports of different devices on the chip. The details of the measurement setup are discussed in [9], to which only two changes were made. Firstly, the source now consists of a tunable quantum cascade laser (tuning range: 3725 nm – 3895nm) from Daylight Solutions which was used also in [10, 11] and secondly instead of butt coupling to the waveguide structures vertical coupling is used. The designs and corresponding measurements are discussed in the following sub-sections.

3.1 Waveguides and fiber-to-chip grating couplers

Three types of waveguide structures were designed and fabricated as shown in Fig. 2. WG1 and WG2 are designed for *imecAP* while WG3 is designed for *imec400*. The single mode widths for these waveguides are calculated using a full vectorial finite difference solver [12]. WG1 is an *imecAP* rib waveguide fabricated by selectively etching only the p-Si and stopping on the 5nm thermal oxide grown between the 220nm c-Si and 160 nm p-Si. The waveguide dimensions are $H = 380$ nm, $W = 1350$ nm, $D = 160$ nm and it has a top oxide thickness of 800 nm. WG2 is an *imecAP* strip waveguide fabricated by using two selective etch steps (160 nm and 220 nm) lithographically aligned to each other. The waveguide dimensions are $H = 380$ nm, $W1 = 1150$ nm, $W2 = 1450$ nm, $D = 380$ nm and it also has a top oxide thickness of 800 nm. $W2$ is deliberately selected 300 nm wider than $W1$ to allow for a misalignment of the second lithography step, which is very safe considering the 50nm alignment accuracy. WG3 is an *imec400* strip waveguide fabricated by selectively etching the 400 nm c-Si in one step. The waveguide dimensions are $H = 400$ nm and $W = 1350$ nm. No top oxide cladding is used in this case.

The different components fabricated in this work are connected to grating couplers as input and output ports for vertical coupling to optical fiber. The single mode waveguide

structures are tapered up to 15 μm over 400 μm and the grating couplers are fabricated in this wider section. The grating coupler layouts are shown in Fig. 3. GC1 is connected to components with input/output waveguides type WG1, GC2 is connected to components with input/output waveguides type WG2 and GC3 is connected to components with input/output waveguides type WG3. The period, fill factor and etch depths for GC1, GC2 and GC3 are (2000nm, 50%, 230nm), (2000nm, 50%, 230nm) and (2140nm, 78%, 400nm) respectively. All grating couplers have 20 periods. In Fig. 3, for GC1 and GC2 the top oxide cladding is not shown. The simulated insertion loss and 3dB optical bandwidth of such grating coupler structures are (-10dB, 220nm), (-13dB, 220nm), (-5dB, 180nm) respectively around 3.8 μm . These grating coupler structures are polarization sensitive and only couple transverse electric (TE) polarized light to the waveguide circuit. Therefore all subsequent measurements are for TE polarized light.

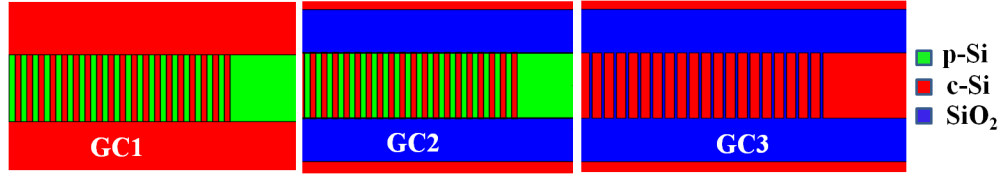


Fig. 3. Schematic top view of grating couplers connecting to the different types of waveguide circuits.

To characterize the waveguide losses we used cut back method where spirals of three different lengths are used for each waveguide type. The bend radii in the spirals (70 μm for WG1, 30 μm for WG2 and 70 μm for WG3) are at-least two times larger than the simulated minimum bend radius; therefore no excess bend loss is expected. From Fig. 4 one can find that the losses at 3760 nm are 5.3 dB/cm, 5.8 dB/cm and 3.1 dB/cm for waveguides WG1, WG2 and WG3 respectively. Figure 5 shows the waveguide loss as function of wavelength for the respective waveguide types. Part of this loss can be attributed to substrate leakage loss, especially at longer wavelengths, as illustrated in Fig. 6, which shows the simulated substrate leakage loss as a function of wavelength for the different waveguide geometries.

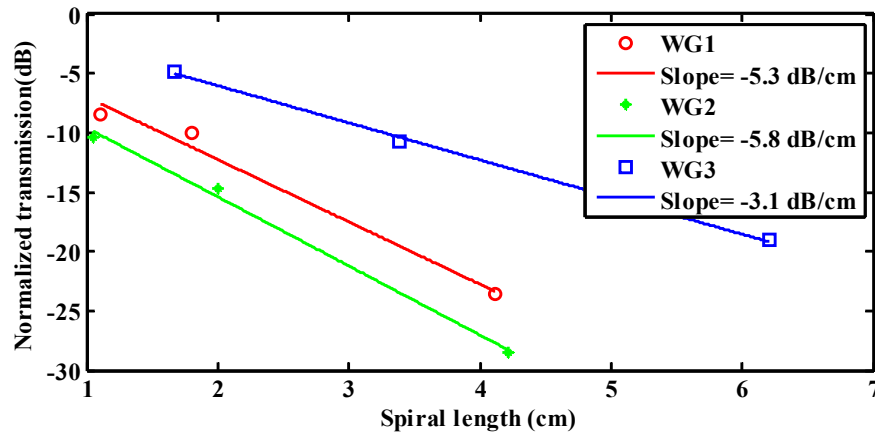


Fig. 4. Waveguide losses at wavelength 3760 nm.

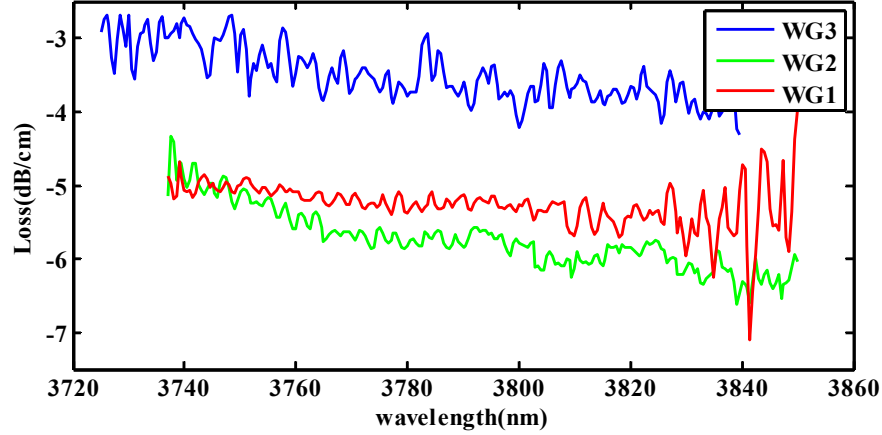


Fig. 5. Waveguide loss versus wavelength.

Clearly the losses of the WG3 geometry are lower than the waveguide structures implemented in the *imecAP* process. This is related to the scattering losses in the polycrystalline silicon overlay (160nm p-Si) of WG1 and WG2. While less performant in terms of waveguide losses, the *imecAP* process has the advantage that near-infrared and mid-infrared circuits can be implemented side by side on the same multi-project wafer, thereby leveraging cost-sharing. Methods to further reduce the scattering losses have been presented in literature [13, 14], which can in principle also be applied to this *imecAP* process. The lower substrate leakage contribution for WG1 is related to the rib type geometry used, compared to the strip waveguide configurations for WG2 and WG3. Further reduction of the substrate leakage loss is possible by increasing the buried oxide layer thickness from 2 μm to 3 μm , which is also a commercially available buried oxide layer thickness [10, 11].

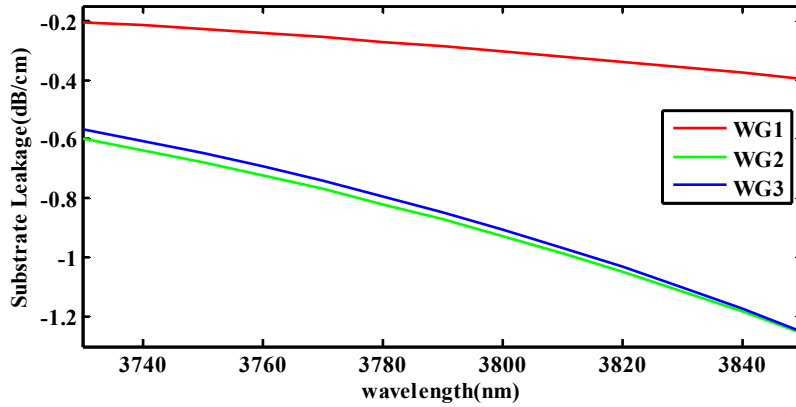


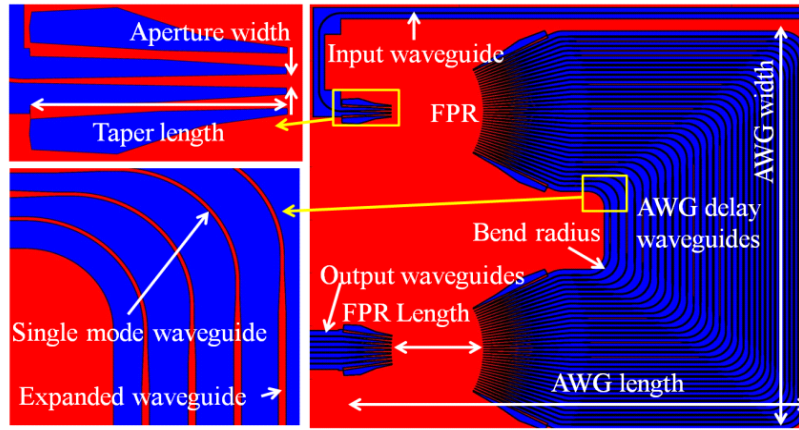
Fig. 6. Substrate leakage loss versus wavelength for the respective waveguide structures.

3.2 Arrayed waveguide gratings

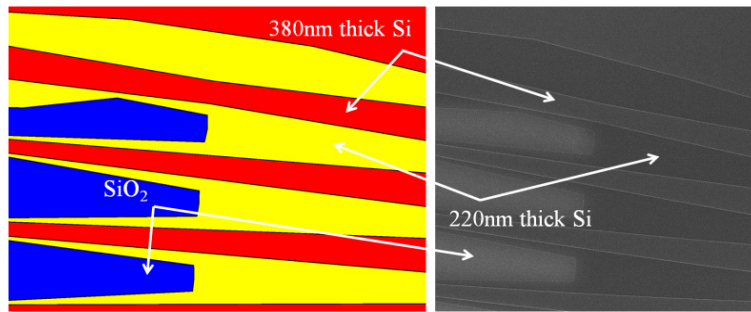
Two arrayed waveguide grating (AWG) de-multiplexers for *imecAP* (named AWG1 and AWG2) and one for *imec400* (named AWG3) were designed. The schematic of such an AWG is shown in Fig. 7 with important layout parameters labeled. An AWG consists of two free propagation regions (FPR) connected together through an array of delay waveguides with constant length increment between them. The other ends of the FPRs (also called star coupler) connect to input and output apertures. Light enters the input star coupler through an input port where it is diffracted towards the array of delay waveguides. Due to the constant length increment between delay waveguides, at the output star coupler the light in consecutive delay

arms has a constant phase delay, which depends on the actual wavelength. As a consequence different wavelengths are focused at different output ports. More information on the design and operation principle of an AWG can be found in [15].

The specifications and layout parameters of the different AWGs designed in this work can be found in Table 1. All AWGs are designed for TE-polarized light. In terms of specifications AWG1 and AWG2 are very similar but their layout and fabrication is different. AWG1 is fabricated in a single etch step using WG1 waveguide structures while AWG2 uses a shallow to deep transition for the star coupler apertures, as shown in Fig. 7(b), while the delay waveguides are fabricated using WG2 waveguide structures. AWG3 is also fabricated in single etch step but using WG3 waveguide structures. Phase errors due to different fabrication anomalies like silicon thickness variation, waveguide width variation, etc. limit the achievable crosstalk level [16]. To make the AWGs more fabrication tolerant we used expanded waveguides in the straight sections of the delay lines, as shown in Fig. 7(a), in order to reduce the phase noise.



(a)



(b)

Fig. 7. (a) Schematic view of an AWG illustrating all critical structures. (b) a detail of the shallow-deep transition used in AWG2 at the star coupler waveguide interface together with an SEM picture of this part of the AWG.

Table 1. Design and layout parameters summary for AWGs

	AWG1	AWG2	AWG3
Center wavelength (nm)	3800	3800	3800
FSR (GHz)	1600 (≈ 77 nm)	1600 (≈ 77 nm)	2000 (≈ 96.3 nm)
Channel spacing (GHz)	200 (≈ 9.6 nm)	200 (≈ 9.6 nm)	250 (≈ 12 nm)
No. of output waveguides	6	6	6
No. of arrayed waveguides	32	32	32
FPR length (μm)	166.3	166.3	169.9
Single mode WG width (μm)	1.35	1.45	1.35
Expanded WG width (μm)	2.5	2.8	2.5
Taper length (μm)	60	60	90
Bend radius (μm)	60	20	40
Aperture width (μm)	4	4	4.5
Arrayed WG spacing (nm)	400	400	200
Etch type	WG1	WG1 + WG2	WG3
Device size: L \times W (mm \times mm)	1.1 \times 0.78	1.05 \times 0.71	0.85 \times 0.75

Figure 8 shows the transmission measurement results for all three AWGs. The transmissions are normalized to corresponding reference waveguides as to only represent the loss of AWGs themselves.

The performance of these AWG (de)multiplexers comes close to the state-of-the-art for silicon-on-insulator AWGs at telecommunication wavelengths (insertion loss of -1 dB and cross-talk of -25 dB [17]), which is remarkable since these devices have gone through many optimization cycles. The higher insertion loss in AWG3 is related to the larger losses at the waveguide / star coupler interface due to the abrupt transition between fully etched strip waveguides and the 400nm silicon free propagation region. While there are differences in design between AWG1 and AWG2 as indicated in Table 1, their performance is similar.

3.3 Planar concave gratings

To show the flexibility and the potential of the platform for mid-infrared spectrometers two planar concave gratings (also known as echelle gratings) were also designed. The design is based on the Rowland geometry with one stigmatic point [18]. PCG1 and PCG2 have been designed for and fabricated in *imecAP* and *imec400* processes, respectively. The schematic of a PCG is shown in Fig. 9 mentioning important layout parameters. The PCG combines the functionality of a flat grating to spatially separate different wavelengths and a curved mirror, which can focus the light to one or more output waveguides. The light enters from an input aperture into the free propagation region (FPR) after which it diffracts and hits the concave grating on the other end, which reflects as well as focuses different wavelengths at different output waveguides.

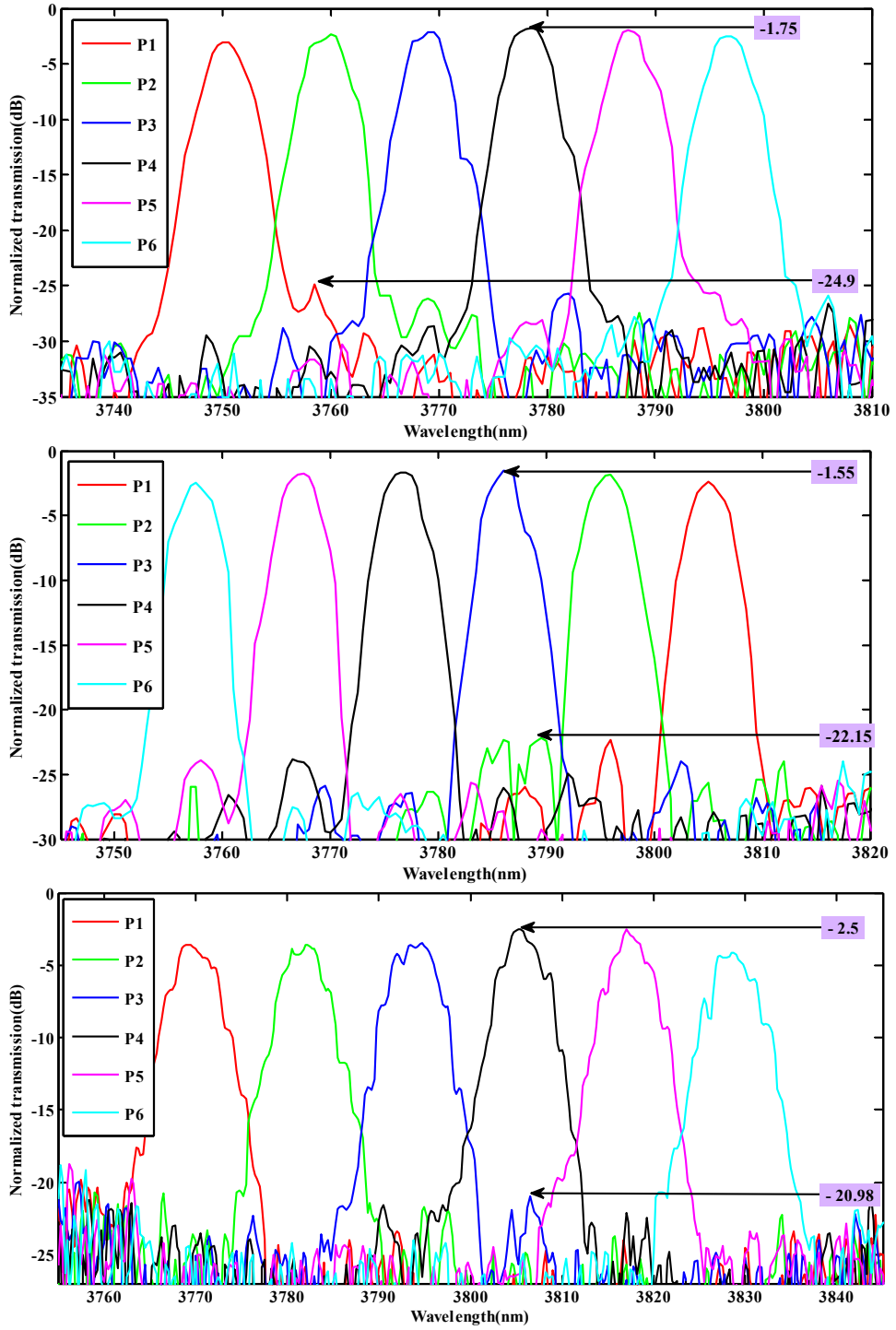


Fig. 8. Transmission spectrum of AWG1, AWG2 and AWG3 respectively.

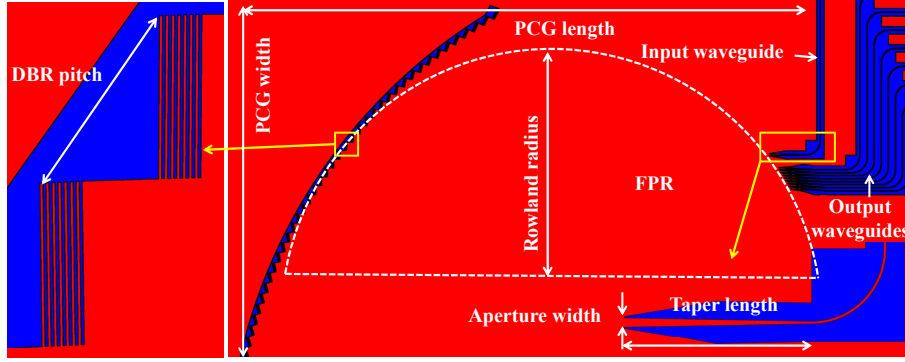


Fig. 9. Schematic view of planar concave grating

Table 2. Design and layout parameters summary for PCGs

	PCG1	PCG2
Center wavelength (nm)	3800	3800
FSR (nm)	105	124
Channel spacing (nm)	10	12
Number of output waveguides	8	8
Input angle (degrees)	34	37
Output angle (degrees)	37	32
DBR pitch (μm)	35	29.9
DBR etch depth (nm)	230	400
No. of grating facets	57	53
DBR period (nm)	880	880
DBR fill factor (%)	50	50
Grating order	27	23
Aperture width (μm)	3	5
Output waveguides spacing (μm)	9	9
Linear dispersion (output wg spacing / channel spacing)	900	750
Rowland radius (μm)	866.6	745.5
Etch type	WG1	WG3
Device size: L \times W (mm \times mm)	1.8 \times 1.7	1.6 \times 1.1

In order to enhance the reflectivity of the grating facets, a distributed Bragg reflector (DBR) is implemented as can be seen in Fig. 9. More details about the design and functioning of a PCG can be found in [18, 19]. The specifications and layout parameters of both PCGs designed in this work are shown in Table 2. Both PCGs are designed for TE-polarized light.

Figure 10 shows the transmission measurement results for both PCGs. The transmissions are again normalized to reference waveguides such that only the insertion loss of PCGs themselves is shown. Similar conclusions as in the case of the arrayed waveguide gratings can be drawn with respect to the differences between the *imecAP* and *imec400* device in terms of insertion loss. The higher crosstalk in PCG2 is attributed to (1) air top clad as compared to oxide top clad in PCG1 (2) different non-optimized layout parameters (e.g. aperture width of 5 μm as compared to 3 μm in PCG1 for same output waveguides spacing) and (3) aperture and star coupler abrupt deep etch transition.

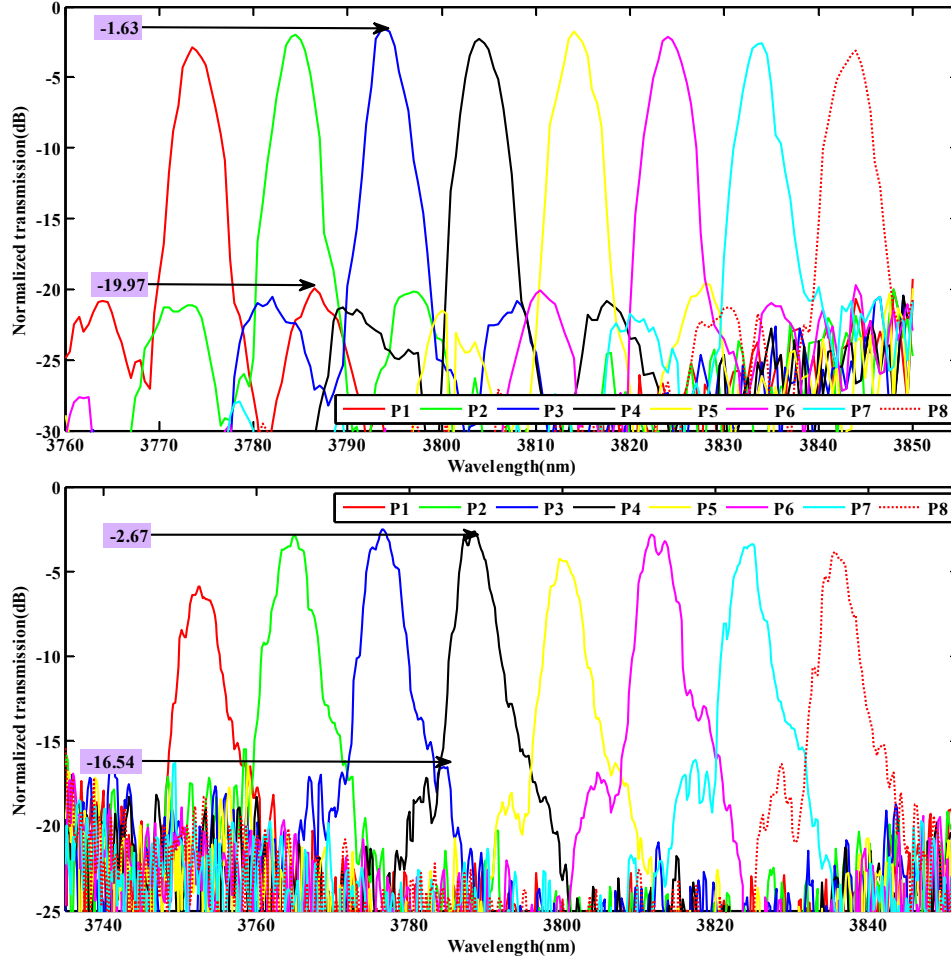


Fig. 10. Normalized transmission response of PCG1 and PCG2 respectively.

4. Conclusion

In this paper we demonstrated the first complex midIR photonic integrated functionality, implemented on a silicon waveguide platform at wavelengths up to 3850nm. The devices were fabricated in a CMOS pilot line, illustrating the potential for large-volume and low-cost manufacturing of such circuits. Moreover, since the *imecAP* process is offered as a multi-project wafer run service, these midIR circuits can be designed alongside near-infrared photonic integrated circuits. Both arrayed waveguide grating demultiplexers as planar concave grating structures were designed and fabricated. Although among the devices reported in this paper the AWGs perform better than PCGs, for applications requiring a large channel spacing PCGs can be a better choice.

Acknowledgments

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