Manuscript for Review

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Journal:	*Electronics Letters*
Manuscript ID:	ELL-2010-2213.R1
Manuscript Type:	Letter
Date Submitted by the Author:	12-Aug-2010
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Keywords:	ANALOGUE-DIGITAL CONVERSION, CMOS INTEGRATED CIRCUITS, COMPARATORS (CIRCUITS), HIGH-SPEED INTEGRATED CIRCUITS

Low-Power 4-bit Flash Analogue to Digital Converter for Ranging Applications

G. Torfs, Z. Li, J. Bauwelinck, X. Yin, G. Van der Plas and J. Vandewege

A 4-bit 700 MS/s Flash ADC is presented in 0.18µm CMOS. By lowering the kickback noise of the individual comparators it was possible to reduce the power consumption to 4.43mW. Improved calibration capabilities resulted in a INL and DNL smaller than 0.25 LSB. These low non linearities give rise to 3.77 effective number of bits at the Nyquist input frequency and this in turn yields an overall figure of merit of 0.46pJ per conversion step. The lowest figure of merit reported for ADCs with sampling rate above 500MHz in 0.18µm CMOS.

Introduction: Scaled silicon technologies made it possible to integrate high speed applications in portable devices. A large subsection of these devices are situated into sensor networks. While these sensors are collecting information, which can then be used by the network, used by a central controller or stored in a database, the knowledge of its actual location would be a very important asset. Markets ranging from tracking of postal packets, organization of warehouses to security and healthcare applications can see the advantages of such a technology. Location aware devices such as [1] require a bandwidth of at least 250MHz to perform an accurate time-of-arrival ranging. The ultra-wide band pulse based radio sends a signal with a fast risetime which makes it possible to detect the arrival of the signal within a range of 3ns, giving a resolution of less than 1m. Flash ADCs are the preferred ADC type for this wideband application requiring

500Msps to digitize an analogue signal with a bandwidth of e.g 125MHz after IQ downconversion. The required resolution to process the ranging signal is 4-bit, and the focus of this work was to minimize the power consumption, which is one of the most important figures for battery powered sensor nodes. This paper presents such an ADC: a 4-bit, 700MHz, 0.46pJ/conversion-step ADC fabricated in 0.18µm CMOS.

Flash Architecture: For high speed, low resolution ADCs, the flash architecture is a promising approach. [2] presents a 0.8pJ per conversion 4 bit ADC working at 1GSps designed in 0.18µm CMOS. An ADC like the one described in [2] offers a low power solution with a linear sample-frequency – power trade-off. The different comparators used in the ADC have a build-in threshold. This is realized by scaling the width of the different input transistors, the resulting offset is then:

$$\Delta V_{th} = \frac{V_{GS} - V_{Tn}}{2} \frac{\Delta W}{W}$$

With V_{GS} the gate-source voltage of the input transistors and V_{Tn} their threshold voltage. This integrated offset reduces the need for a static reference ladder and removes its power consumption. Such a comparator is displayed in Fig 1. A downside of this approach is the kickback noise generated by the comparators. Due to the difference in gate-drain capacitors of transistors M_{n2} and M_{n3}, a memory effect is introduced. During the reset phase of the comparator (when the sample clock (clk) is going from logic high to logic low), the nodes X_L and X_R are pulled up to the supply voltage. Assuming the output code was '1' (V_{out+} = high, V_{out-} = low), node X_R would initially be charged through M_{p6} in parallel with the series connection of M_{n5} and M_{p3}. Node X_L will only be charged through transistor M_{p1}. This results in a different time constant for the charging of the two branches, which induces different charges stored on the drain-gate capacitance of M_{n2} and M_{n3}. Different charges mean different voltages at the input nodes. Depending on the

driving impedance these can give a big disturbance at the next sample time.

An approach to reduce kickback noise is proposed in [3]. By adding transistors M_{n4} and M_{n5} in Fig. 2 the input transistors and their gate capacitance are disconnected from the nodes X_L and X_R and they are discharged more or less symmetrically during the reset phase via transistor M_{n1}. With the addition of the extra transistors, M_{n1} can be biased to reduce the current consumption of the comparator which slows down the slewing inside the comparator which will further reduce the kickback noise. The result is an increased sensitivity and giving the possibility to do a more accurate calibration.

Reduction of the kickback noise makes it possible to drive the ADC with a higher impedance, which in turn reduces the power dissipated in this stage. The driver is designed as a 500MHz two-stage unity gain feedback operational amplifier implemented on the same die providing a high input impedance to the preceding stage, a big advantage compared to [2] which needs a 50 Ohm drive to function properly.

Experimental results and comparison: The ADC has been fabricated in a 0.18µm CMOS technology. The differential input signal was applied to the chip through a balun and the output codes were sampled with a 10GSps digital oscilloscope and processed offline. The linearity was measured by applying a 10MHz triangle wave. The resulting differential (DNL) and integral non-linearity (INL) is shown in Fig. 3. Without calibration large variations and even missing codes can be observed. Due to process and mismatch errors, the threshold of the comparators can vary up to 2 LSB. After calibration the DNL is below 0.2 LSB and the INL below 0.25 LSB.

The dynamic performance is analysed by applying a full scale differential sine wave. The captured data is then fitted to an ideal sine wave, and with these parameters the signal to noise and distortion ratio (SNDR) and the effective number of bits (ENOB) was

calculated. The resulting measurements for sample frequencies of 500 and 700MHz are shown in Fig. 4. The ENOB with a sample frequency of 500MHz is 3.92 at the Nyquist frequency and 3.77 with a sample clock of 700MHz. After 700MHz the ENOB starts to degrade quickly due to the speed limitations of the ROM-based digital circuit which converts the thermometer code of the comparators to binary code. Adding a flip-flop in between the comparators and the ROM would solve this timing issue, extending the operating frequency with only a marginal increase of the power consumption.

The measured power consumption is 4.30 mW at 500MHz and 5.56mW at 700MHz from a 1.8V supply. These figures include the 2-stage input buffer which consumes 1.13mW. Without the power consumption of the buffer the figure of merit (FoM) of the ADC core is respectively 0.42pJ and 0.46pJ per conversion step at 500 and 700MHz. Including the power consumption of the buffer the FoM is still 0.57pJ and 0.58pJ per conversion step respectively. Table 1 compares these figures with the state of the art [2,4-8]. To the author's knowledge, this design achieves the lowest FoM for flash ADCs in this technology node.

Conclusion: A 4 bit 700MHz ADC in a 0.18µm CMOS technology is designed and tested. It was shown that by reducing the kickback noise of the individual comparators, the power consumption could be lowered to 4.43mW without degrading the linearity which at a Nyquist input signal still remained 3.77 effective number of bits, yielding a figure of merit of 0.46pJ/conversion step. The lowest figure of merit reported for ADCs with sampling rate above 500MHz in 0.18µm CMOS.

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Figure captions:

Fig 1. Comparator with build-in threshold

Fig 2. Reduced kickback comparator
Fig 3. Differential and integral non linearity before calibration and after calibration at a

sample rate of 700MHz

Fig 4. Effective number of bits versus input frequency at sample rates of 500MHz and 700MHz

Table captions:

Table 1. Comparison with state-of-the-art Analog to digital converters.

Fig 1.

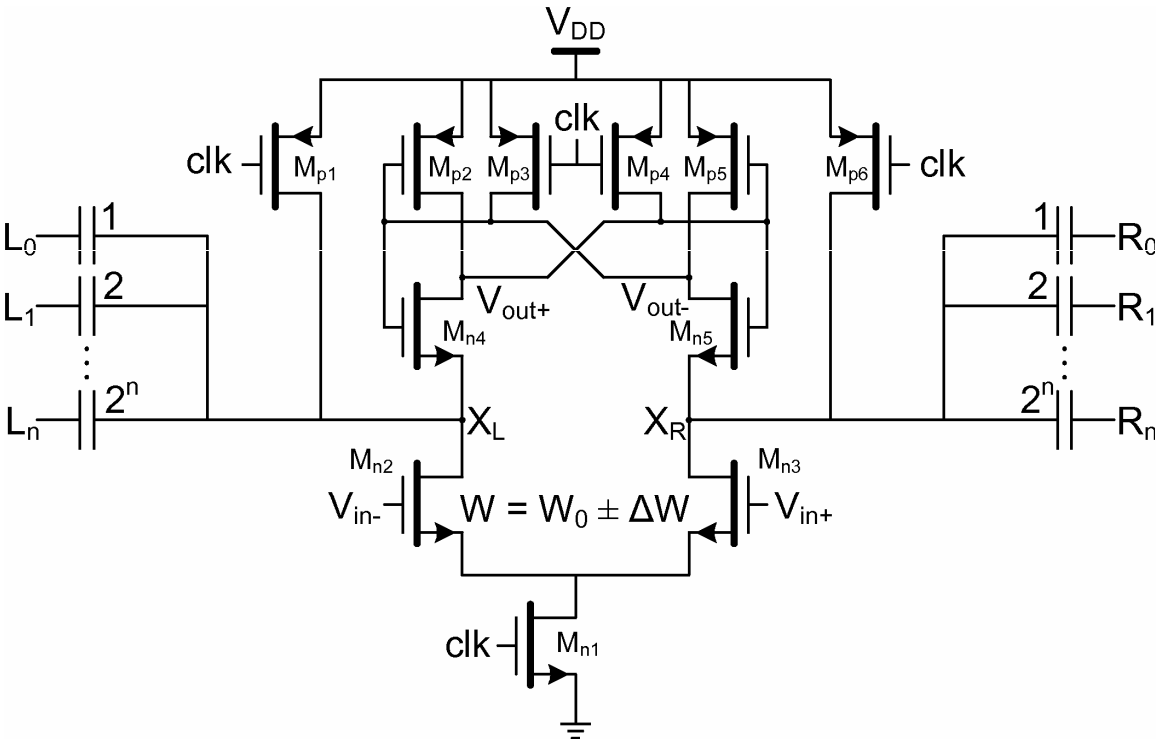
V_{DD}
clk
clk
M_{p1}
M_{p2}
M_{p3}
M_{p4}
M_{p5}
M_{p6}
clk
L_0
1
L_1
2
L_n
2^n
V_{out+}
V_{out-}
M_{n4}
M_{n5}
X_L
X_R
1
R_0
2
R_1
2^n
R_n
M_{n2}
M_{n3}
V_{in-}
$W = W_0 \pm \Delta W$
V_{in+}
clk
M_{n1}

Fig 2.

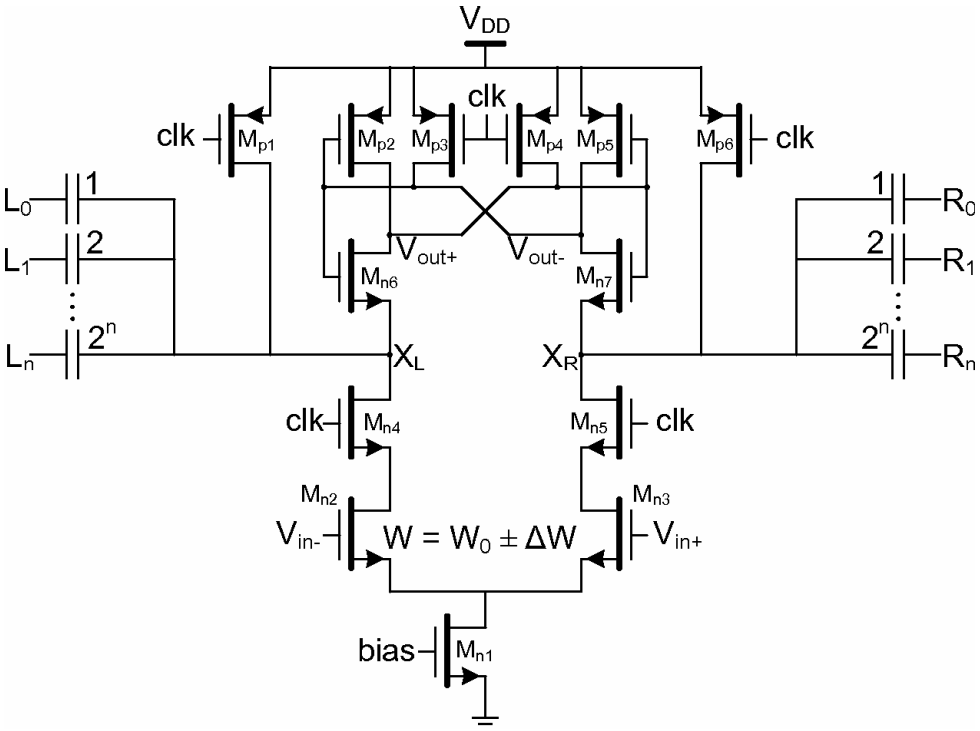
VDD
clk
clk
Mp1
Mp2
Mp3
Mp4
Mp5
Mp6
clk
L0
L1
Ln
1
2
2n
Vout+
Vout-
Mn6
Mn7
1
2
2n
R0
R1
Rn
XL
XR
clk
Mn4
Mn5
clk
Mn2
Mn3
Vin-
W = W0 ± ΔW
Vin+
bias
Mn1

Fig 3.

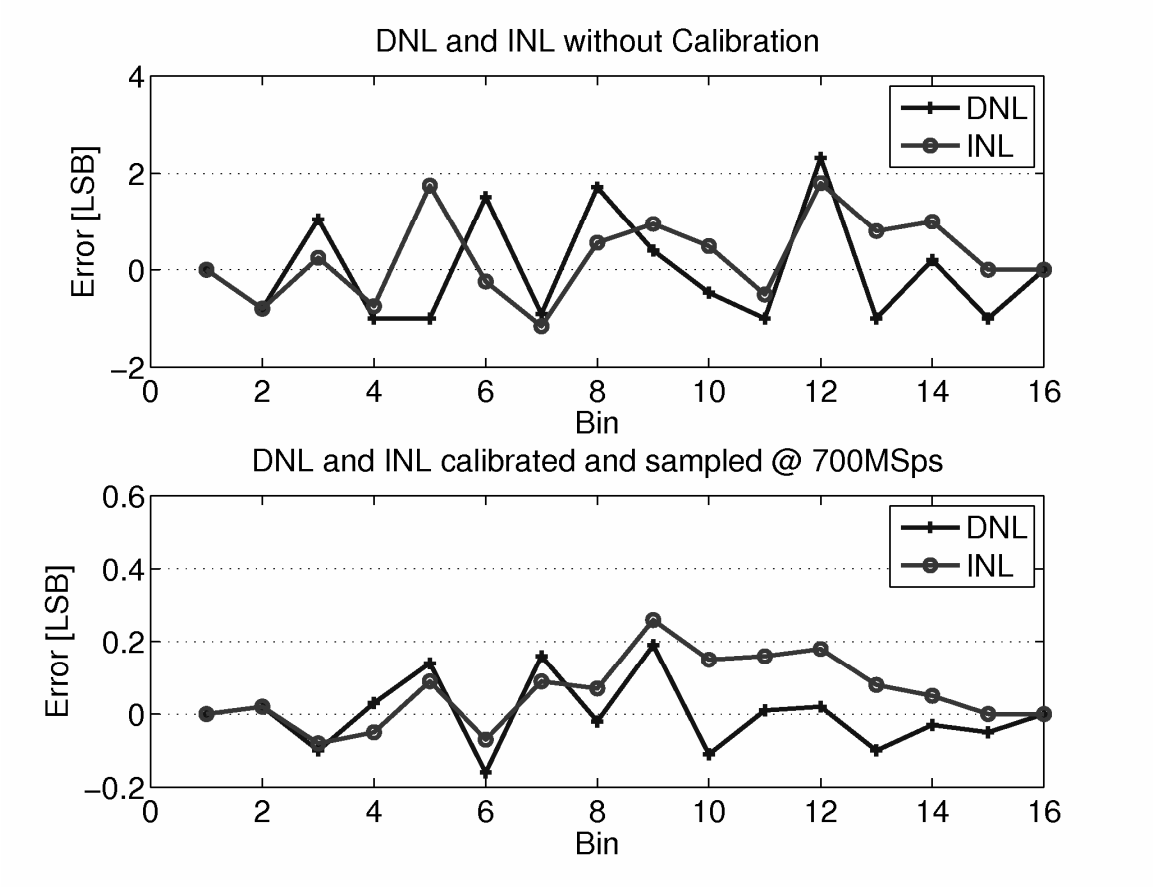
DNL and INL without Calibration
Error [LSB]
Bin
DNL
INL
DNL and INL calibrated and sampled @ 700MSps
Error [LSB]
Bin
DNL
INL

Fig4.

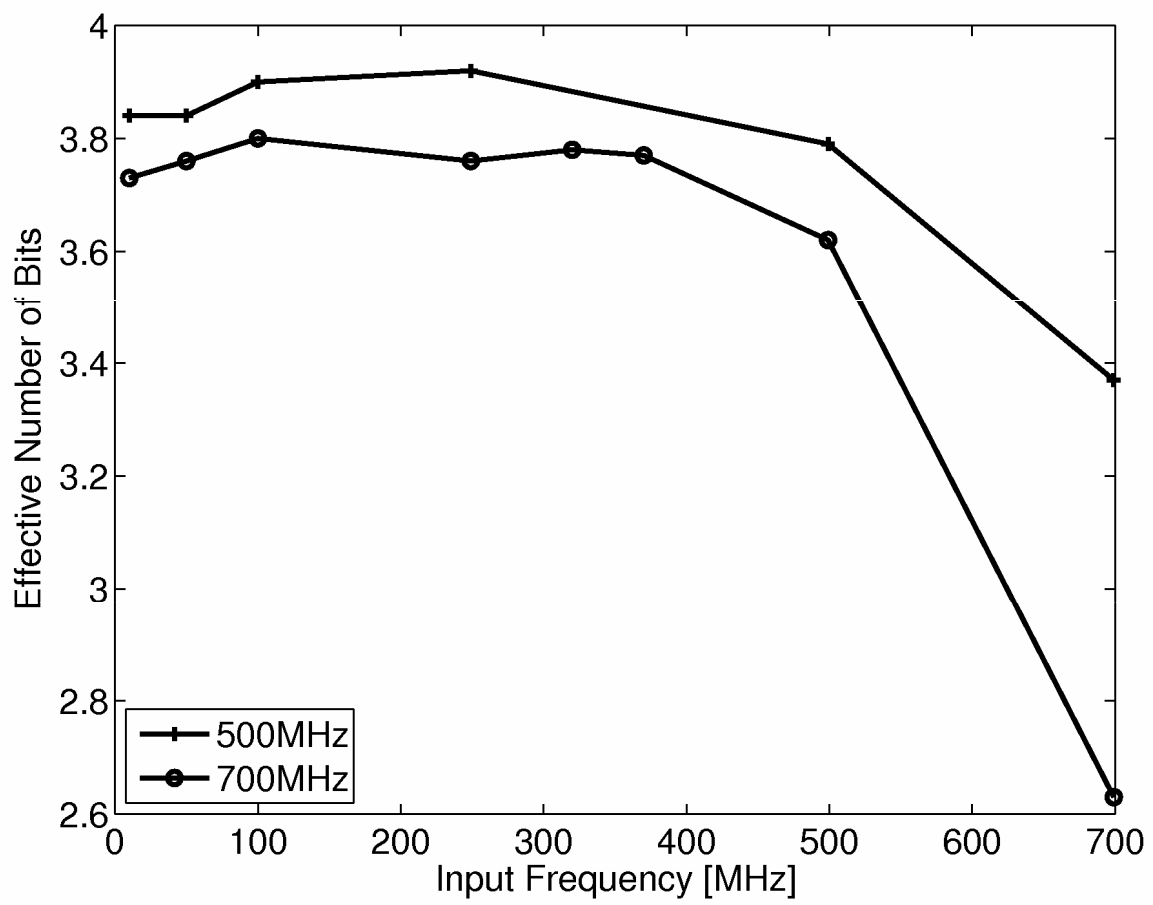
Effective Number of Bits
Input Frequency [MHz]
500MHz
700MHz
4
3.8
3.6
3.4
3.2
3
2.8
2.6
0
100
200
300
400
500
600
700

Table 1.

	Technology	# of bits	DNL	INL	ENOB @ Nyquist	Sample Frequency (MHz)	Power (mW)	FoM (pj/conv)
This work	0.18μm	4	<0.19	<0.27	3.77	700	4.43	0.46
[2]	0.18μm	4	<0.25 3.7	<0.17 1000	3.8	500	5.2 10.6	0.73 0.81
[4]	0.18μm	4	0.4	1.1	3.24	400	20	5.30
[5]	0.18μm	4	0.04	0.06	3.61	2000	42	1.72
[6]	0.13μm	6	0.49	0.42	4.69	1600	180	4.36
[7]	0.13μm	6	<0.6 5.7	<0.4 1200	5.6	600	90 160	3.09 2.56
[8]	0.13μm	5	<0.24	<0.39	4.44 4.54	2000 3200	120 120	3.07 4.30