High dynamic range 60 MHz powerline front-end IC

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Presented for the first time, is a novel broadband powerline front-end realised in 0.25 μm SiGe BiCMOS with superior performance. The frequency range of the transmitter (TX) and the direct conversion receiver (RX) exceeds 60 MHz with a very wide dynamic range up to 99.5 dB for the lowest channel bandwidth. The integrated IF filter is tunable from 1 up to 8 MHz. The measured input-referred noise of the TX with low third intermodulation distortion (IMD3) is −140 and 144.5 dBm/Hz for the RX.

Introduction: Broadband over powerline communications employing the electricity distribution network is an alternative approach to provide broadband services to users who are not within the deployment strategy of incumbent operators. Many different powerline communication (PLC) systems are being developed and several proposals are under discussion in the IEEE P1901 working group [1]. Frequency division multiplexing (FDM) is undoubtedly the most straightforward way to achieve coexistence between different PLC systems (even homeplug AV includes the possibility to use FDM for coexistence). Besides realising coexistence, there is a strong demand to exploit higher transmission frequencies, to reduce electromagnetic (EM) radiation and to be more robust against interferers. The proposed patent pending powerline front-end IC solves these issues in combination with a high degree of integration, a very high dynamic range, and provides the highest frequency range reported to date.

Conventional PLC front-ends, designed for a time division multiple access (TDMA) scheme (e.g. homeplug), do not use frequency conversion in the analogue front-end [2–4]. As a consequence, the receiver (RX) and the ADC capture the complete frequency range. This puts very high requirements on the ADC in terms of number of bits and conversion rate. Scaling to higher transmission frequencies would require a proportional increase of the ADC conversion rate (e.g. 300 Msps for a 100 MHz system), which is difficult to achieve at low cost and low power consumption. Moreover, the higher the PLC system bandwidth (BW), the more vulnerable the system becomes to interferers [5].

Existing powerline front-ends for FDM systems can be divided in two groups. The first employs a classical heterodyne upconversion architecture [6], requiring filters at high IF which are difficult to integrate on chip with good selectivity and linearity. External filters (e.g. SAW filters) are usually used with fixed BW. The second group uses a number of fixed input bandpass filters, which leaves very little flexibility to select the channel frequency and BW [7, 8].

Design concept: The proposed powerline front-end architecture is shown in Fig. 1. The transmitter (TX) generates a multicarrier signal with variable BW of 2/4/8/16 MHz in the frequency range from 1.6 to 60 MHz. The transmit section on the chip consists of a sixth-order Sallen-Key Butterworth reconstruction filter and a variable gain amplifier (VGA) with a 1 dB gain step, which is connected to the external line driver. The receiver (RX) section has a direct conversion architecture. The variable gain low noise amplifier (LNA) with a 1 dB gain step can be bypassed by a variable attenuator so that the receiver can operate linearly up to the breakdown voltage of IO's of the IC. The LNA can select one out of four inputs, each corresponding to a different preselector filter band delimited by an off-chip crossover filter. This is particularly useful when the spectrum contains strong interferers, e.g. low frequency noise or ham radios. The mixer is passive, arranged in a Weaver topology, of which the second stage of the mixer is in the digital domain. The mixer is followed by a passive lowpass filter (LPF) and a VGA. The IF filters (fifth-order Chebychev Gm-C) are integrated on the chip, including a switched capacitor frequency stabilisation loop. The purpose of this filter is to attenuate out-of-band noise and interferers as well as anti-aliasing (the lowest aliasing frequency is attenuated >60 dB when the ADC clock is four times the filter BW). The BW of the IF filter is tunable to 1, 2, 4 and 8 MHz to support a wide class of service requirements. The frequency stabilisation and tuning occurs in the background, with no effect on signal reception.

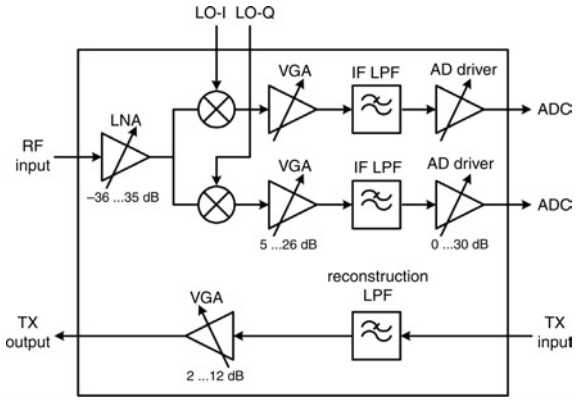

Fig. 1 *Analogue front-end ASIC architecture*

The proposed architecture provides high flexibility (very wide gain range, tunable channel BW and arbitrary centre frequency), and a high degree of integration, and can be scaled to higher frequency ranges (e.g. 100 MHz) because the ADC performance (and the ADC cost) is not the limiting factor. Scaling up to higher frequencies requires only a redesign of the LNA, the mixer and the TX reconstruction filter, which is certainly feasible in the chip technology. All blocks are fully differential and strong feedback linearisation was used to reduce distortion.

Experimental results: The presented chip was fabricated in a 0.25 μm SiGe BiCMOS technology. The die size is 3.5 × 3.5 mm^2 and power consumption from a single 2.5 V supply is 668 mW. The TX BW is 72.4 MHz at max gain (11.5 dB) and 79.1 MHz at min gain (2.3 dB). The TX provides more than 20 dB attenuation (21.3 dB/24.2 dB at min/max VGA gain) of the DAC image frequencies (above 148 MHz). The measured third-order intermodulation distortion (IMD3) is shown in Fig. 2 as a function of frequency, and the input-referred noise is −140.2 dBm/Hz (measured at 10 MHz with max gain). The RX BW is 62 MHz (measured at 21 dB LNA gain). The input-referred noise of the RX is shown in Fig. 3 as a function of LNA gain (LO at 10 MHz). The measured RX noise (−144.5 dBm at max LNA gain) is well below typical powerline noise levels (−130 dBm/Hz), even at low gain settings. The IMD3 is shown in Fig. 4 as a function of the input level, in which the gain was set to achieve a 1 Vpp at the AD driver output (RF at 10 MHz, LO at 8 MHz). The RX operates linearly up to the breakdown voltage of the IO's, so that the maximum input level is 18 dBm. Integrating the input noise over the minimum channel width (2 MHz) yields a noise level of −81.5 dBm and a very high dynamic range of 99.5 dB. For the maximum channel width of 16 MHz, 90.5 dB dynamic range is reached. This novel design provides the highest frequency range to date ([2–4] are limited to 20 or 30 MHz), whereas the architecture provides more flexibility (channel frequency/BW) and the possibility to filter interfering signals prior to AD conversion, in combination with a very high dynamic range.

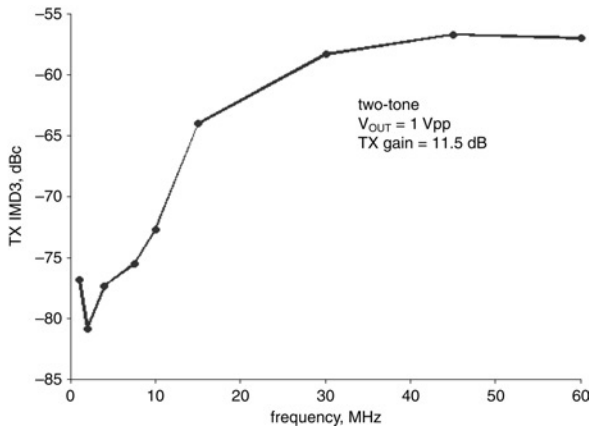

Fig. 2 *Transmitter two-tone IMD3 measurement for 1 Vpp output swing as function of frequency*

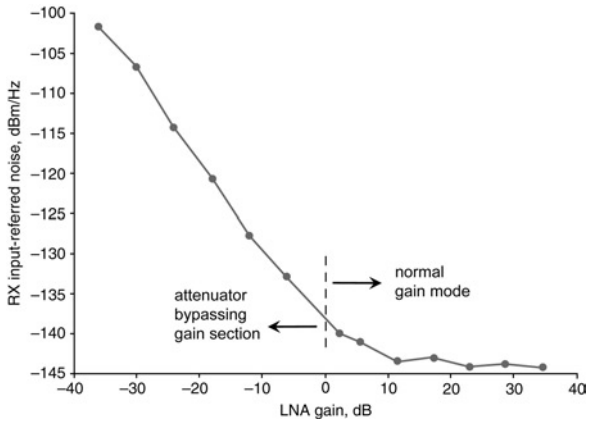

Fig. 3 *Receiver input-referred noise as a function of LNA gain*

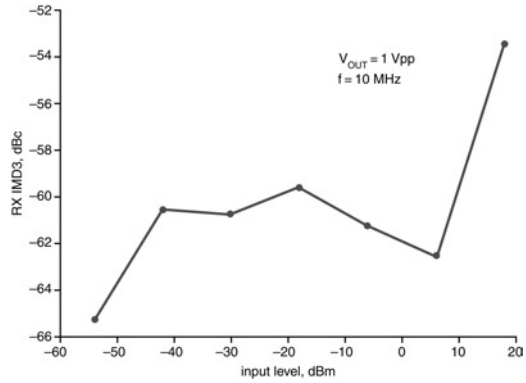

Fig. 4 *Receiver two-tone IMD3 measurement for 1 Vpp output swing as function of input level (RF around 10 MHz, LO at 8 MHz)*

Conclusion: An innovative broadband powerline front-end approach is presented. Operation up to 60 MHz has been demonstrated, with a very high dynamic range (90.5 to 99.5 dB). The RX noise floor is well below typical powerline noise levels and the RX can operate linearly up to the breakdown voltage of the IO's. Furthermore, the new architecture provides more flexibility and a higher robustness against interferers compared to existing solutions owing to the preselector filter, the frequency conversion, the tunable IF filter and the linear operation up to 18 dBm.

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