A Reconfigurable Digital Platform for the Real-Time Emulation of Broadband Copper Access Networks

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***Abstract*—This paper presents a reconfigurable platform for the real-time digital emulation of broadband copper access networks. The instrument, which uses hard real-time digital-signal-processing techniques on Xilinx Virtex II field-programmable gate arrays, is capable of accurately reproducing the physical layer of a digital subscriber line (DSL). The magnitude and the true phase of the insertion and return loss of the twisted pair access loop, which consists of cables with various characteristics and length, are digitally emulated over the full DSL bandwidth. The innovative character and advantages of digital emulation techniques over conventional analog loop emulation are demonstrated, and its performance is assessed using several test cases.**

***Index Terms*—Digital signal processor (DSP), digital subscriber line (xDSL), emulation, field-programmable gate array (FPGA), physical layer of communication systems, real time.**

I. Introduction

THE WIDE-SCALE deployment of fiber-optic backbone networks is already a fact; yet, for the last mile(s) up to the subscriber, the reuse of current copper access networks is a standard practice. In most cost studies, this "last mile," which connects individual houses, takes the biggest share, and the reuse of twisted pair telephony cables is favored. This explains the success of the digital subscriber line (DSL) technology, which can support megabit data rates over phone lines connecting nearly every home. However, the copper pair networks were designed for voice traffic with a limited bandwidth of 3.4 kHz, but T1, E1, asymmetric DSL (ADSL), ADSL2(+), and very high speed DSL (VDSL) may exceed the voice bandwidth more than a thousand fold. The efficient exploitation of copper pair access networks at high bandwidth therefore presents a formidable challenge, and the capability of accurately analyzing and emulating specific access line cables and topologies has become quite important.

A reconfigurable digital module for the emulation of the physical layer of communication systems is presented. The feasibility of such a system is demonstrated through the development of a proof-of-concept digital access loop emulator for VDSL applications within the framework of the European MEDEA+ project MIDAS [1]. This compact prototype instrument can emulate (i.e., imitate in real time) quite complex phone line networks. Therefore, for the first time, a single instrument can support a wide range of cable types and loops. Measurements can even be made in the field and later transferred to the emulator to precisely replicate field-installed phone lines.

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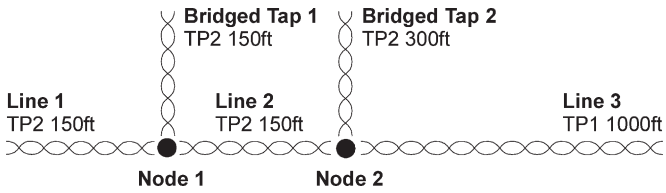

Fig. 1. ANSI VDSL4 access loop topology.

II. Problem Analysis

A. Access Loop Topologies

The connection between the DSL subscriber and the local exchange usually consists of a cascade of twisted pair lines, which can vary in type and length. In some cases, open ends of the unused twisted pair, which are called bridged taps, are connected in parallel somewhere along the loop (Fig. 1).

A topology of lines and bridged taps gives rise to echoes or reflections, which interfere with the original signal. A good example is the transfer function of the "VDSL4" [2] line topology as shown in Fig. 2. A highly irregular low-pass pattern appears, which illustrates the complex task that the DSL equipment has to perform to provide reliable high-speed data transmission over this medium.

B. Shortcomings of Analog Access Loop Emulators

Analog line emulators are a valuable asset to DSL designers as they allow the emulation of transmission line topologies in a laboratory environment. However, these instruments have limited flexibility, i.e., typically only supporting a set of loops as defined by the standardization bodies [2], [3]. Analog line emulators are bulky and usually require more than one instance of the instrument to emulate a full loop topology. Furthermore, emulators based on lumped elements can exhibit precursor energy, which results in an incorrect impulse response of the loop.

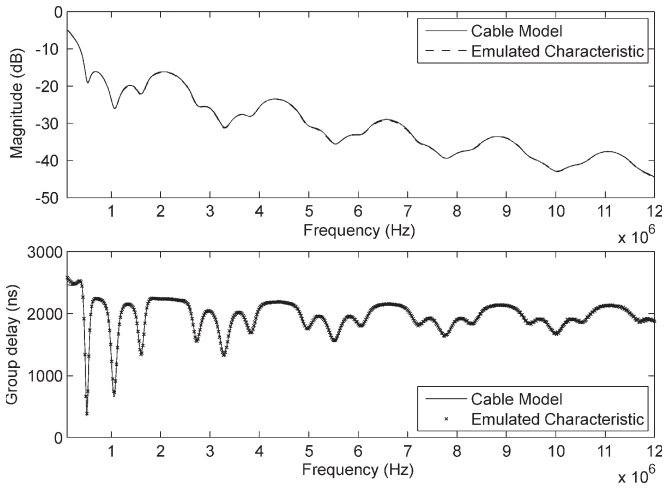

Fig. 2. ANSI VDSL4 transmission characteristic: emulation versus model.

Passive analog emulators aim to accurately reproduce the primary transmission line parameters (R, L, C, and G) of a twisted pair instead of the secondary parameters (attenuation, group delay, impedance, and return loss). Although being products of the primary parameters, the secondary line parameters are of importance to the performance of the xDSL communication equipment, and a direct emulation of the secondary parameters is beneficial for the achievable accuracy.

Finally, analog component tolerances, combined with variations caused by environmental conditions and aging, pose a performance barrier for the accurate and consistent channel emulation.

Active analog line emulators can be somewhat more flexible and show less precursor energy, but many other problems remain unsolved. Active analog emulators are generally limited to the emulation of a single line segment such that to emulate a complex loop topology, several boards or instruments may be needed. Due to the active components, this type of emulator has a higher noise floor and a poorer strong-signal performance than its passive counterparts.

III. Reconfigurable Hardware Platform for Digital Emulation

A. Introduction

A field-programmable gate array (FPGA)-based digital-signal-processing module that is capable of emulating the physical layer of a broadband communication system in real time is presented. Depending on the communication system for which the emulator is designed, different behavioral characteristics and specifications will apply. This myriad of different requirements makes the design of the module more challenging and illustrates the flexibility of the digital emulator concept. The feasibility of such a system is demonstrated through the development of an access loop emulator for VDSL applications.

Several attempts to digitally perform physical layer emulation are documented in the literature. In most cases, simplifications are made to the original model to reduce the complexity or to increase the feasibility of a real-time implementation. This leads to partially inaccurate representations of the physical medium of interest.

In [4], a frequency-domain approach for telephone access network emulation is described using digital techniques. However, the approach does not result in an accurate reproduction of a real loop topology for two reasons. First, the author uses block-based processing of the input signal stream, which inevitably results in a misrepresentation of the group delay response of the topology, because the sampling window generally exceeds the group delay of most loop topologies. Second, the author describes a unidirectional solution and discards the effects of loop reflections on the transmitter end.

In the domain of powerline communications, Götz and Dostert propose a reduction of the theoretical model derived [6] by only extracting the dominant paths in what is perceived as a multipath environment and employ finite-impulse-response filter structures to approximate the channel response. A real-time implementation such as the one proposed in [6] certainly profits from this complexity reduction but fails to include all details of the original channel.

The proposed hardware concept again only provides a unidirectional emulation of the channel, i.e., suffering from the same limitations as in [4]. It will be shown that a solution based on bidirectional IIR filters is able to alleviate these shortcomings.

B. Real-Time Digital Emulation

A lossy transmission line can be described by three parameters, i.e., its characteristic impedance Z_0, the exponential wave propagation function $\gamma(\omega)$, and its length L. In [7] and [8], it is shown that a transmission line can be exactly emulated with a system that decomposes the line behavior into the exponential wave propagation function and its characteristic impedance, as illustrated in Fig. 3.

Two reflection modules are responsible for the immediate effects due to the impedance mismatch at the loop ends. The propagation module, which emulates the exponential wave propagation function in real time, is the scope of this paper.

Digitally implementing this propagation module has a number of advantages over the classical analog designs for physical layer emulation.

1) Reconfigurability: The capability to reconfigure the platform (within seconds) so as to accommodate different types of physical media within a specific technology is an important asset. It allows changing physical layer models to include additional aspects that were not covered in the original models or even add new models without making labor-intensive hardware modifications. The processing core in fact is quite generic, i.e., offering emulation of bidirectional propagation and filtering over a wide bandwidth, long delay, and high dynamic range. Its reconfigurable nature, combined with a high-performance analog front end, results in a versatile platform suitable for a wide range of instrumentation applications.

2) Reproducibility: A digital core produces consistent results over a prolonged time period and is not prone to aging and environmental influences as are analog designs. However, the necessary conversion to and from the analog domain reduces the deterministic character. In-system calibration procedures

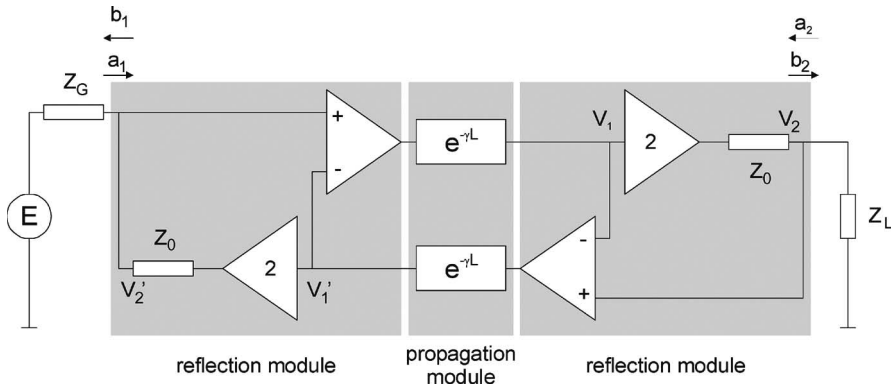

Fig. 3. Equivalent transmission line structure.

compensate for the introduced inaccuracies without any modification to the actual hardware platform as the compensation is digitally performed.

3) Delay Emulation: The correct emulation of group delay (true phase) of the transmission medium is important. Advanced communication systems typically use one or more mechanisms to compensate for the frequency-dependent characteristics of the transmission medium, which are commonly called equalizers. From a digital perspective, the group delay can be efficiently emulated using delay lines, which support very long delays, while maintaining a fine granularity. Analog delay lines, although feasible, cannot achieve the same combination of flexibility and range.

4) Time-Variant Fading Channels: An important parameter of a communication system is its stability against channel variations. This impairment is typically observed in wireless communications, but it also exists in the telephone access network. Temperature variations affect the primary loop characteristics, especially the resistance per unit length and to a lesser degree the inductance per unit length [9]. The need to evaluate the performance of a wireline communication system with channel variations has been recently identified in [10]. Although a testing method based on heating or cooling real cable sections is proposed, digital emulation provides a far more accurate and reproducible means to realize the equivalent channel variations.

C. Design Constraints

Digital emulation has several advantages over the current passive and active analog approaches yet faces a set of technology-related hurdles, which are discussed below. The combined specifications on linearity, bandwidth, dynamic range, noise floor, and accuracy are very high and require state-of-the-art components and novel design approaches as the emulator needs to outperform the already high-performance DSL equipment to successfully validate it.

1) Hard Delay Constraints: The correct emulation of the phase response and its first derivative, i.e., the group delay, is a constraint not often found in the design of a digital (sub)system. Strict end-to-end delay budgets need to be met, which results from the physical propagation along the emulated line segments. The available computational window, i.e., the time available to perform the necessary calculations, is equal to the delay of the emulated physical medium minus the time needed for the A-to-D and D-to-A conversions and the delay of the analog low-pass filters. This means that for one of the shortest sections in the European Telecommunications Standards Institute (ETSI) and ANSI VDSL test loops, i.e., a 150-ft cable, only 257 ns of processing time is available (Fig. 1). It is clear that very high performance digital filter structures are needed, especially for the shorter cable lengths. The delay budget needs to be carefully distributed over the building blocks of the system.

2) Bandwidth: The bandwidth of the system is limited by the throughput rate of the FPGA-based signal processing core through the Nyquist condition. A sample rate of 32 MSPS is necessary to process the full VDSL bandwidth of 12 MHz without too stringent anti-aliasing filter specifications. Typical clock rate improvements such as pipelining the critical paths cannot be applied here as this increases the throughput delay.

3) Noise Floor and Dynamic Range: Compared to a fully passive approach, the use of active components requires a more careful optimization of the noise floor performance and dynamic range. As the noise contribution due to roundoff inside the digital core is minimized by using a processing word width of 32 bit, the analog front-end including the A/D and D/A conversion forms the limiting factor. Special care was taken to optimize the design from a system perspective.

D. Digital Processing Core

The core of the system is a fixed-point second-order IIR filter or biquad. The six filter multiplications are calculated using Xilinx Virtex-II 18×18 bit two's complement embedded multipliers. To accommodate for the internal sample representation of 32 bits, two of these multipliers and a registered adder are combined to build a 32×18 bit multiplier.

A straightforward area-efficient filter implementation requires a single 32×18 bit multiplier running at six times the sample rate of 32 MHz (192 MHz). At this speed timing closure can only be reached by adding an input register to the multipliers at the expense of increased throughput latency. In view of the primary application constraint (throughput delay), an alternative approach was favored.

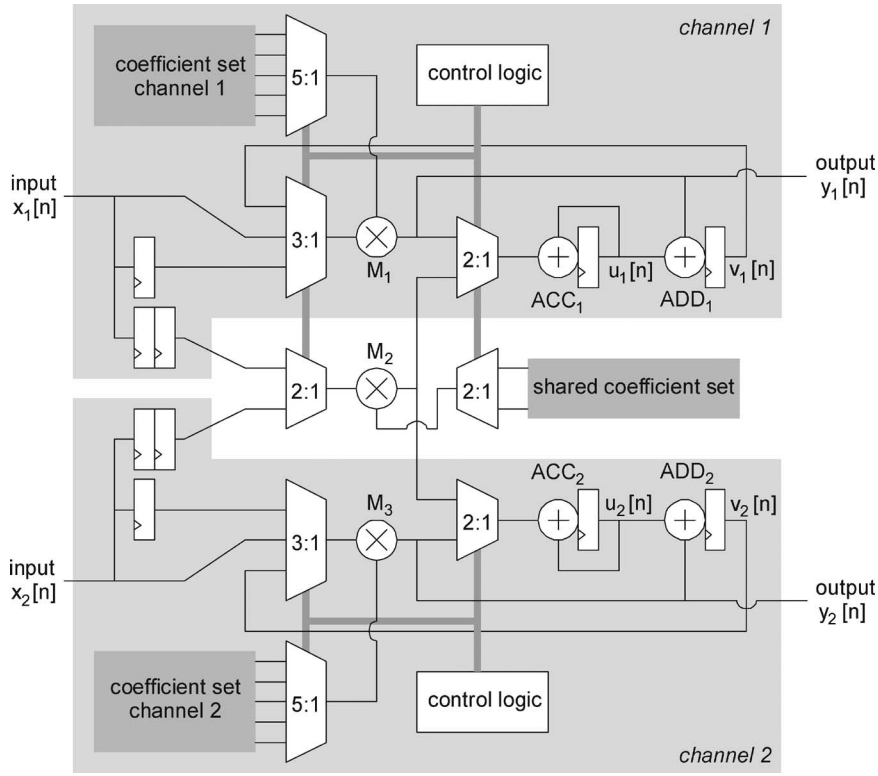

Fig. 4. Biquad architecture.

Using a single-stage pipelined multiplier clocked at five times the sample rate, a throughput latency of one sample cycle is achievable. The downside of this approach is the necessity to include a second multiplier to perform the sixth multiplication, which reduces the average multiplier efficiency to a mere 60%. However, by combining two biquads into a single structure and sharing a third multiplier, the efficiency can be raised to 80%. Furthermore, such a dual-channel structure easily supports the bidirectional signal propagation the system requires.

The basic structure of the two-channel biquad is shown in Fig. 4. At the heart of the biquad, three single-stage multipliers are located. Multipliers M_1 and M_3 each perform five multiplications per sample cycle, whereas M_2 only performs two. This choice, as opposed to evenly distributing all 12 multiplications over the three multipliers, was made to minimize the routing delays and the probability of routing congestion caused by nonrelated signal paths. Because the nominal clock frequency of 160 MHz is lower than in the single-channel biquad implementation, the routing margin for paths toward the multipliers is considerably larger, and the routing issues are avoided.

The accumulators ACC_1 and ACC_2 are fed by 2-to-1 multiplexers that switch between the dedicated and the shared multiplier outputs, and sum four intra-biquad products to produce the intermediate value $u[n]$ as

$$\begin{aligned} u[n] &= b_1 x[n-1] + b_2 x[n-2] - \frac{a_1}{a_0} v[n-1] - \frac{a_2}{a_0} v[n-2] \\ v[n] &= b_0 x[n] + u[n] \\ y[n] &= \frac{1}{a_0} v[n]. \end{aligned} \tag{1}$$

The final addition is performed in a registered adder (ADD) to generate $v[n]$, whose output is fed back to the multiplier to produce the biquad output, after multiplication by $1/a_0$. The additional adder was introduced for a specific purpose, i.e., as it is only enabled in one out of five cycles, it doubles as a memory element storing $v[n-1]$. The order in which the feedback path multiplications are executed is chosen such that an additional memory element for $v[n-2]$ is not required. A single multiplexer port is therefore sufficient for all three feedback multiplications, which limits the total number of multiplexer inputs at the multipliers. If the equations above are put together and transformed into the Z-domain, the expected transfer function appears as

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{a_0} \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + \frac{a_1}{a_0} z^{-1} + \frac{a_2}{a_0} z^{-2}}. \tag{2}$$

The filter fully reflects the design constraints. It allows for bidirectional signal propagation and has a low latency of 31.25 ns, high dynamic range, and sufficient bandwidth for VDSL applications. Next to the signal flow discussed here, a control interface is present to load the filter coefficients even while operating. This way, the channel characteristics varying over time can be emulated.

E. Building Block Architecture

The accurate emulation of the four scattering parameters of a given loop topology requires several second-order IIR filters to be combined into a higher-order filter. The filter architecture proposed in this paper splits a loop topology, as shown in

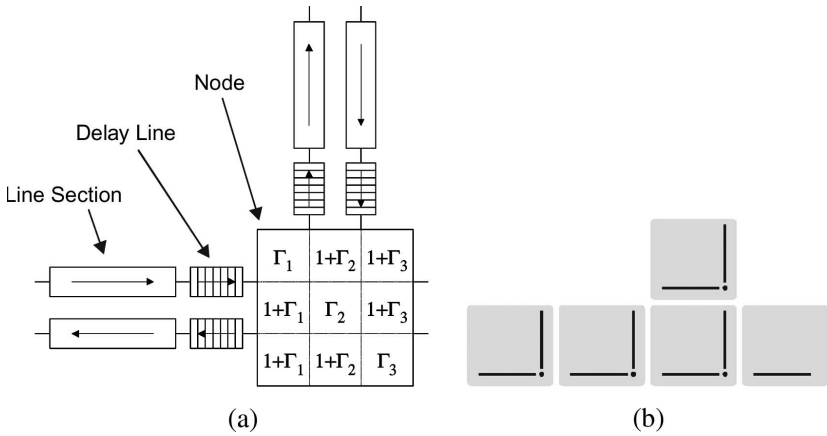

Fig. 5. (a) Basic building block (BBB). (b) Decomposition of a line topology into BBBs.

Fig. 1, into building blocks, namely lines and bridged taps, and so remains close to the actual cable layout. Apart from lines and bridged taps, which have a physical equivalent, a virtual element, called a node, is introduced as well. The node represents a splice where cable sections are joined together and is responsible for the frequency-dependent reflections that occur due to the characteristic impedance mismatches between cable sections.

These line and node sections are devised from several cascaded second-order IIR filters. The line sections also include a delay line that emulates the constant part of the total group delay. A line, a node, and a bridged tap are combined in what is referred to as a "basic building block" or BBB. Multiple BBBs are concatenated to form the cable topology of interest (Fig. 5).

F. Distributed Delay Compensation

The system must be capable to emulate cables of various lengths. Short cable sections require the device to be optimized for minimal delay, but long delays must also be possible. This is easily achieved with the introduction of a digital delay line in the system. A dedicated control interface allows setting delays up to 32 μs with a granularity of 31.25 ns even while running.

Delays are also introduced in other system components, e.g., A-to-D and D-to-A conversion, the biquad filter processing time, anti-aliasing filters, and the phase characteristic of the configured biquads. The former two introduce a constant group delay, and the latter two introduce a group delay varying over frequency. The total group delay of a cable topology can be distributed over these blocks as long as the total end-to-end delay of any signal path still matches the real topology. Thus, the nonzero delays of processing elements can be compensated by lowering the delay line values. Careful delay distribution over the building blocks allows for lines as short as 150 ft to be accurately emulated.

G. System Configuration

Two key elements contribute to the flexibility of the system: the reconfigurable nature of the FPGA and the programmability of the BBBs. An FPGA design combines a number of BBBs at top level, which defines the shape of the access loop. The actual length of individual cable sections and their characteristic impedance is later defined with IIR filter coefficients [11] and delay line settings loaded through the control interface of each block. To maximize the flexibility of an FPGA design, some building blocks can be bypassed, which is an important gain on the end-to-end delay budget. Furthermore, the FPGA designs are fully in-system programmable, which thus allows the emula tion of time-varying parameters such as temperature influences.

This highly modular and flexible approach allows the accurate emulation of ETSI and ANSI VDSL test loops 0 to 4, as well as custom loop topologies in a single instrument.

H. Hardware Overview

The digital propagation module consists of two identical interconnected boards each hosting an FPGA, a high-performance 14-bit A/D converter (ADC), one 14-bit D/A converter (DAC), and a Universal Serial Bus (USB) 2.0 interface (Figs. 6 and 7). One module interfaces to a hybrid connected to the subscriber DSL modem, and the other module connects through a second hybrid with the central office equipment.

The hard real-time signal processing is performed on two Xilinx Virtex-II XC2V3000-6 FPGAs with a full duplex communication link of 1 Gb/s interconnecting them. To address even more complex line topologies, each board can be equipped with a second identical Xilinx Virtex-II FPGA, which doubles the number of available logic gates up to 12 million.

Special care was taken in the design of the analog frond end. First of all, a custom shielding made of a solid metal slab was fabricated to achieve isolation of better than 104 dB between the A/D and D/A channel for frequencies below 16 MHz.

Second, the noise floor of each channel was optimized. This results in a system with a noise floor below -140 dBm/Hz and a dynamic range of over 80 dB (see Test Case C).

The control platform of the system is a PC running Linux with a custom USB kernel module. The USB 2.0 connection is used to configure the FPGAs and perform settings afterward.

IV. Results

In this section, the performance of the emulator core is evaluated against a simulation model of the test loops. The

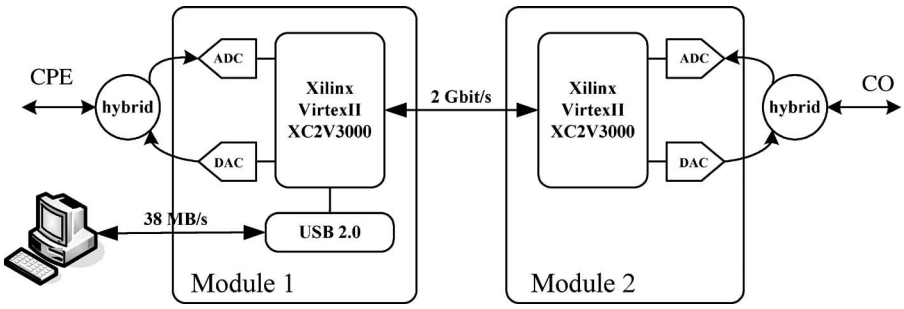

Fig. 6. Dual module emulation setup.

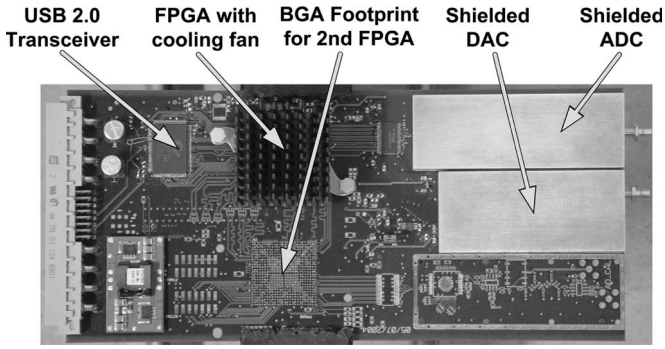

Fig. 7. Overview of a digital module.

reference simulation model is generated using a Matlab-based simulation tool, i.e., the FTW xDSL simulation tool [12], which contains model data for all the standardized DSL test loop sets. All the test loops evaluated here are extracted from the standardized reference test loops mentioned in [2] and [3], and are based on the models provided in [13] to provide a basis for objective reference. The actual frequency characteristics were measured with a Hewlett-Packard network analyzer of type HP4395A. The measurements shown in the following paragraphs are obtained without the reflection modules in place to evaluate the performance of the digital core.

The specifications adhered to are those listed in [3], i.e., a maximum magnitude deviation of 3% on a decibel scale and a group delay error of less than 3% on a linear scale. A schematic view of the topologies covered in the different test cases is shown in Fig. 8.

A. Test Case "ANSI VDSL2"

The ANSI VDSL2 test loop consists of a cascade of two transmission line sections with a relatively long second section that represents street cabling and a first shorter section that may represent cabling at the subscriber's premises. The design loaded in the first FPGA contains the 250-ft section and the node. It consumes 35% of the slices and 43% of the 96 embedded multipliers. The second FPGA only contains a line section, which consumes 20% of all the slices and 25% of the embedded multipliers. Fig. 9 shows the accuracy with which the loop is emulated. The rather long TP2 section already introduces considerable attenuation at higher frequencies, yet the measured frequency response remains closely matched to the expected model, i.e., to within 0.5 dB. The emulated loop accuracy exceeds the ETSI requirements: the group delay always remains within the 3% allowed margin of error with an average deviation of less than 20 ns.

B. Test Case "ANSI VDSL4 1 kft"

An example of a complex loop topology is the ANSI VDSL4 test loop. This topology is an excellent example of a delay-constrained design and requires careful distribution of the delay budget over the building blocks of the system. The first node, where signal reflections occur, is encountered after only 150 ft and corresponds to a roundtrip delay of 457 ns. This figure includes the propagation delay across the propagation modules and the signal conversion circuits, which amounts to approximately 200 ns, which leaves only 257 ns to digitally process the incoming signals. This demonstrates that the digital emulator is capable of meeting the strict delay budgets.

The first FPGA contains two nodes with the bridged taps consuming 65% of the logic and 83% of the embedded multipliers. Clearly, the number of available multipliers and not the number of slices is the limiting factor with respect to the loop complexity that can emulated. The design in the second FPGA is identical to case B but programmed with a different set of parameters.

The location of the notches and their depths are clearly defined (Fig. 2), which indicates correct emulation of both the group delay and the amplitude response of the two bridged taps. Fig. 10 quantifies the close correspondence between the model of the emulated topology and the measurements. The group delay remains within the allowed margin of error except for the lowest frequency notches, where the coefficient generation algorithm [11] has difficulty tracking the desired characteristic. However, the severity of this deviation is debatable considering the fact that the DSL equipment will generally avoid transmission in these notches. With the exception of these notches, the coefficients loaded into the FPGA produce a group delay characteristic that is accurate to within a 50 ns margin.

C. Test Case "ANSI VDSL4 4.5 kft"

The FPGA design discussed in the previous case can be easily reprogrammed with new settings to lengthen the TP1 section to 4500 ft. The result is shown in Fig. 11 and is an excellent illustration of the dynamic range that can be reached with the digital building block concept. Above 6 MHz, the attenuation remains below 98 dB. The group delay maintains compliance up to 4.5 MHz, above which noise prohibits an

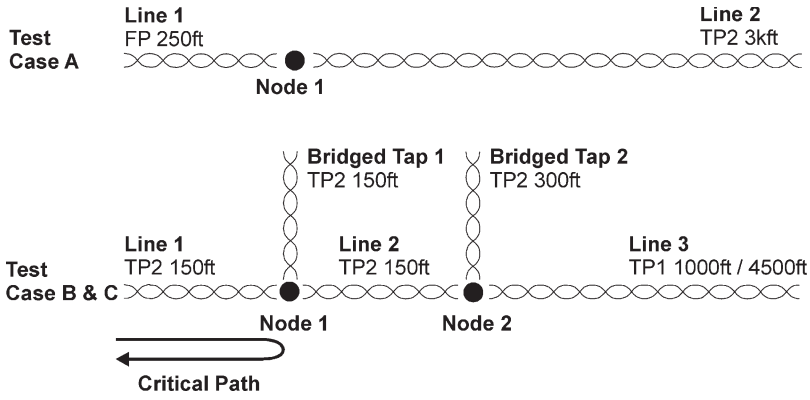

Fig. 8. Loop topologies of test cases A, B, and C.

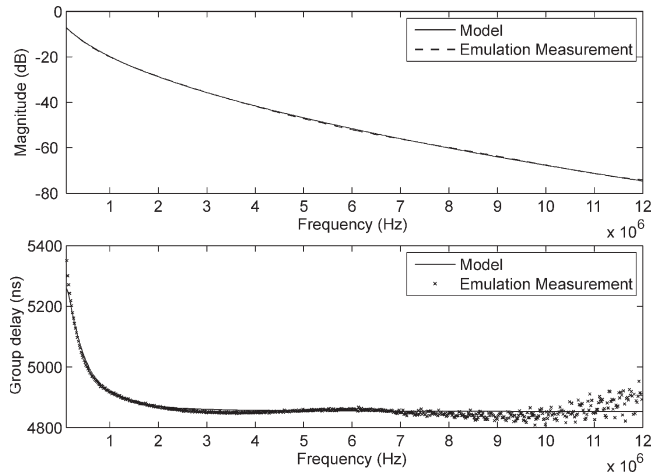

Fig. 9. ANSI VDSL2: Emulation versus Measurement (S_{21}).

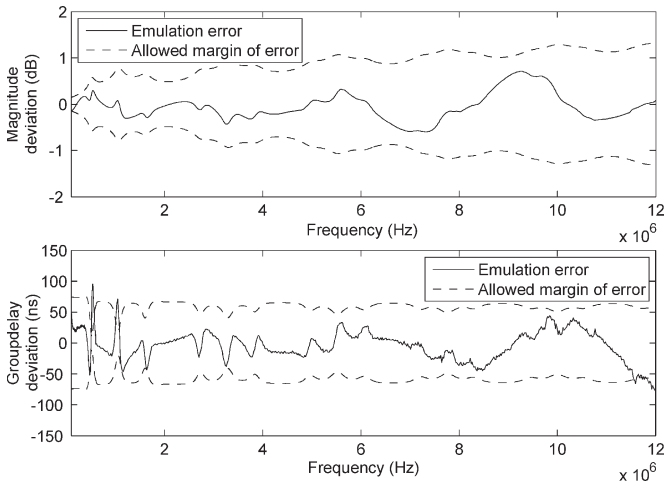

Fig. 10. Emulation Accuracy of ANSI VDSL4 1 kft (S_{21}).

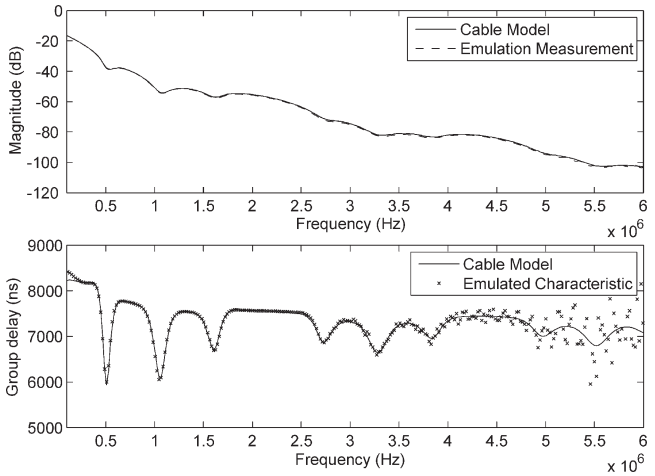

Fig. 11. ANSI VDSL4 4.5 kft: Emulation versus Measurement (S_{21}).

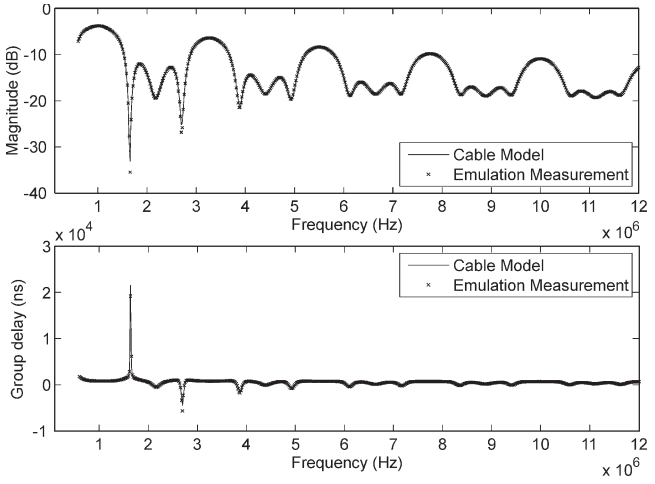

Fig. 12. ANSI VDSL4 4.5 kft: Emulation versus Measurement (S_{11}).

accurate phase measurement. However, the average group delay is maintained up to 6 MHz.

Finally, the scattering parameter $S_{11}(\omega)$ of this loop topology is shown in Fig. 12, which demonstrates the delay accurate emulation of extremely short line sections. The accurate representations of the reflections at both the network side and the customer side are important in the evaluation of the DSL equipment, because high-level reflections of the upstream signal may mask the considerably lower power downstream signal. Second, the correct emulation of the group delay at both sides of the loop is necessary to realize the correct input impedance of the loop, which is dependent not only on the characteristic impedance of the line section but also on the frequency response of the propagation module. The performance of the emulator is exemplary as even in the notches the emulator accurately reproduces the complex loop behavior.

V. Conclusion

In this paper, a reconfigurable platform for the emulation of telephone access networks has been presented. The multimillion-gate FPGA design is capable of emulating both the amplitude and the absolute phase of a complex line topology even for very short line sections with high accuracy and has several advantages over commercially available emulators. The modular building block concept, easy reconfiguration, and high-performance analog signal handling make this a very flexible instrument for further the exploration and development of the DSL technology.

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