A High-Resolution Burst-Mode Laser Transmitter With Fast and Accurate Level Monitoring for 1.25 Gb/s Upstream GPONs

Johan Bauwelinck, *Student Member, IEEE*, Wei Chen, Dieter Verhulst, *Student Member, IEEE*, Yves Martens, Peter Ossieur, *Student Member, IEEE*, Xing-Zhi Qiu, *Member, IEEE*, and Jan Vandewege, *Member, IEEE*

***Abstract*—An innovative burst-mode laser transmitter (BM-TX) is presented for gigabit-capable passive optical network (GPON) upstream transmission at 1.25 Gb/s. The laser bias and modulation current each can reach 80 mA with a resolution of 0.1 mA providing a total drive current up to 160 mA. Both currents are generated by 10-bit current steering digital-to-analog converters (DACs), the architecture of which is specially adapted to yield a monotonic current setting at settling times below 12.8 ns. Tests show that fast automatic power control (APC) can stabilize and track the launched optical power with a tolerance of less than 1 dB over a wide temperature range for outdoor operation. The APC only requires a straightforward calibration of the "0" and the "1" level at room temperature. Optical level monitoring on strings of four consecutive "0" bytes and two consecutive "1" bytes at 1.25 Gb/s is demonstrated. APC based on such short strings of data has not been shown before.**

The circuits have been designed in a 0.35 μm SiGe BiCMOS process. Experimental results show that this dc-coupled BM-TX meets the specifications of the recently approved ITU-T Recommendation G.984.2 supporting an intelligent power leveling mechanism (PLM).

***Index Terms*—Burst-mode laser drivers, current comparators, current mirrors, digital–analog conversion.**

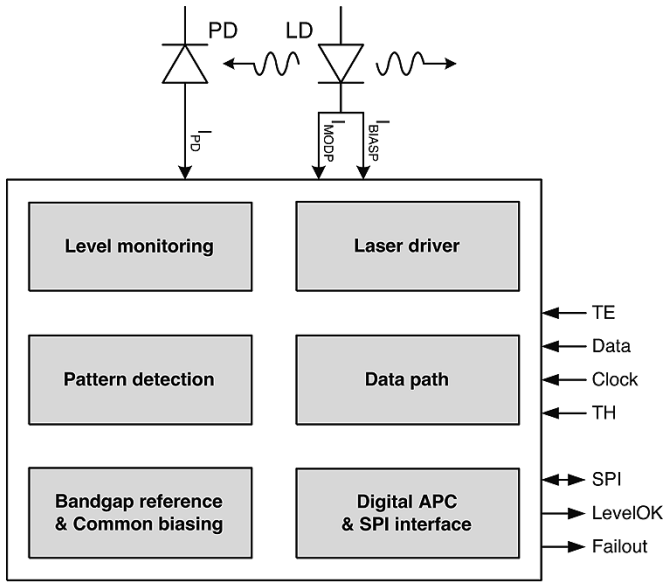


Fig. 1. Building blocks of the BMLD.

I. Introduction

A BURST-MODE laser transmitter (BM-TX) is one of the key building blocks of a gigabit-capable passive optical network (GPON), in which the capacity of the fiber plant is shared among a group of subscribers. Only one subscriber at a time is allowed to send data upstream, so that all subscriber lasers have to operate in burst or intermittent mode. A 3.3-V mixed-mode burst mode laser driver (BMLD) chip is presented (Fig. 1). The BMLD directly modulates the laser diode (LD) in burst mode and regulates the launched power (P_{OPT}) via an automatic power control (APC) loop. The chip is programmable via an SPI interface and generates all time-critical signals internally, which makes it easy to use. The driver is enabled by the transmit high (TH) signal, or the burst envelope signal that enables the bias level. The current mode logic (CML) data, clock, and TH signal are connected to the data path. The data path retimes the data (and TH) before applying it to the laser driver stage (LDS) and provides the necessary signals to the pattern detection block. The LDS switches the bias (I_{BIAS}) and modulation (I_{MOD}) current required by the LD. These currents are generated by 10-bit current digital-to-analog converters (DACs). During data strings of successive 1's or 0's, the level monitoring (LM) circuit compares the monitor current I_{PD} (generated by a back facet monitor photo diode PD in the laser module) with two reference currents ($I_{\mathrm{REF\_"1"}}$ and $I_{\mathrm{REF\_"0"}}$), corresponding to the desired "1" and "0" launched optical power respectively. As the presence of these strings in the data stream is self-detected by the pattern detection block, no time-critical signals such as a preamble envelope or an arming signal is required for the APC. Subsequently, the digital APC block makes use of these measurements to adjust the I_{BIAS} and I_{MOD} setting, respectively. During initialization of the optical power (in a "ranging window"), a binary-like search algorithm (with maximum power level protection) regulates I_{BIAS} and I_{MOD}. After initialization, subsequent bursts start from the APC adjusted values for I_{BIAS} and I_{MOD} of a previous burst and only small adjustments (e.g., 0.1 mA) are made to I_{BIAS} and I_{MOD} in between the bursts. The APC supports the power leveling mechanism (PLM) described in the ITU-T (International Telecom-

Manuscript received August 6, 2004; revised February 8, 2005. This work was supported in part by the Flemish Government under the Research Contract IWT 2001-0019 Sympathi, in part by the European Commission under the Research Contract IST-2001-34523 GIANT, and in part by STMicroelectronics and Alcatel Bell.

The authors are with the Department of Information Technology, INTEC/IMEC, Ghent University, B-9000 Gent, Belgium (e-mail: johan.bauwelinck@intec.UGent.be).

Digital Object Identifier 10.1109/JSSC.2005.848024

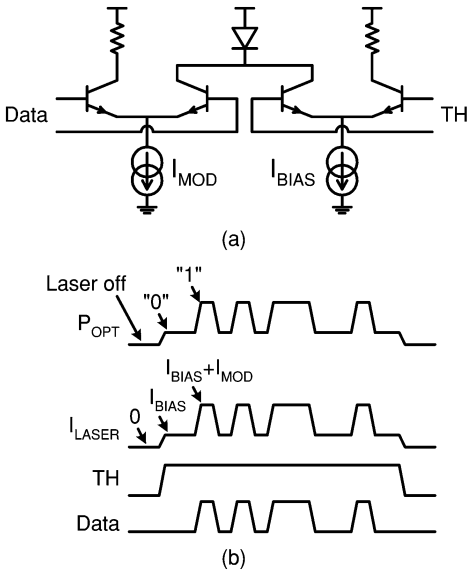


Fig. 2. (a) Conventional burst-mode laser driver stage and (b) principle of operation.

munication Union–Telecommunication Standardization Sector) Recommendation G.984.2 [1]. The PLM option was adopted to relax the dynamic range requirement of the upstream burst-mode optical receiver at the access node of the network. The required PLM state (encoded in a downstream message) is extracted by a digital network termination chip, which changes the PLM state in the BM-TX via the SPI interface. The BM-TX then automatically increases/decreases the laser power by 3 or 6 dB. The LevelOK signal indicates the completion of the initialization of the optical "0" and "1" power. Failures of the APC loop are indicated by the Failout signal. The transmit enable (TE) signal is used to disable some parts of the circuitry when no burst is sent upstream for power consumption reduction. In this paper we focus on the design and the experimental results of the LDS and the LM as these are the most critical blocks in a BMLD.

The remainder of this work is organized as follows. Section II presents the LDS including the 10-bit current DACs that generate I_{BIAS} and I_{MOD}. Section III presents the current-mode LM circuitry and Section IV describes the experimental results of the test chip. Finally, conclusions are drawn in Section V.

II. Laser Driver Stage

A. Introduction

For a GPON upstream transmitter a dc-coupled BMLD is required [2]. During transmission, the LD must be biased above its threshold to reduce the turn-on delay and to limit the duty cycle distortion. Fig. 2(a) shows two conventional dc-coupled differential pairs [3] that are combined to a BMLD sinking the laser current (I_{LASER}). Besides switching I_{MOD} at the data rate, a BMLD has to turn I_{BIAS} on and off quickly (controlled by TH) as shown in Fig. 2(b). The major disadvantage of a dc-coupled interface is that the voltage drop of the LD (up to 1.6 V) reduces the collector-emitter voltage V_{CE} of the output transistor. The

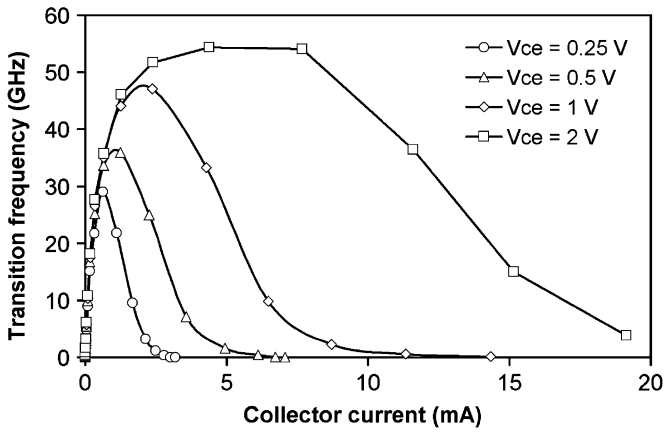


Fig. 3. Transition frequency as a function of collector current for a typical SiGe BiCMOS npn transistor.

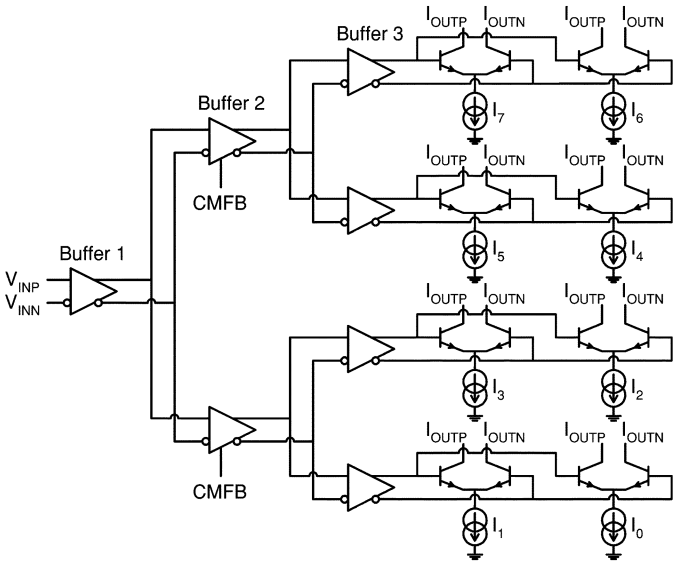


Fig. 4. Laser driver stage architecture. The data path generates the inputs $V_{\mathrm{INP}}, V_{\mathrm{INN}}$ based on the incoming data or the TH signal. $V_{\mathrm{INP}}, V_{\mathrm{INN}}$ switch between the levels $V_{\mathrm{DD}} - V_{\mathrm{BE}}$ and $V_{\mathrm{DD}} - V_{\mathrm{BE}} - V_{\mathrm{DIFF}}$ in which V_{DD} is the supply voltage $(3.3\ \mathrm{V} \pm 5\%)$, V_{BE} the base-emitter voltage drop of an emitter follower and V_{DIFF} is the differential voltage swing. The output I_{OUTP} connects to the LD whereas I_{OUTN} connects to a resistor.

RF performance of the switching transistors depends heavily on V_{CE} and on the collector current I_C as shown in Fig. 3.

An alternative dc-coupled configuration is described in [4]. In this alternative configuration the laser cathode is grounded. A fast (npn) differential pair is used to generate a fast switching current which is subtracted from a dc current source to make the "0" and "1" level laser currents. However, for GPON burst mode operation, an "off" state and a fast enabling/disabling of the "0" power is required [1]. This enabling or disabling is not straightforward for the configuration of [4] as the "0" optical power is determined by the difference of two current sources.

B. Circuit Description

From Fig. 3 it is clear that, a single dc-coupled differential pair cannot be fast enough over a wide current range. For this reason we split the differential pair in branches having different tail currents as shown in Fig. 4. Two separate circuits similar to

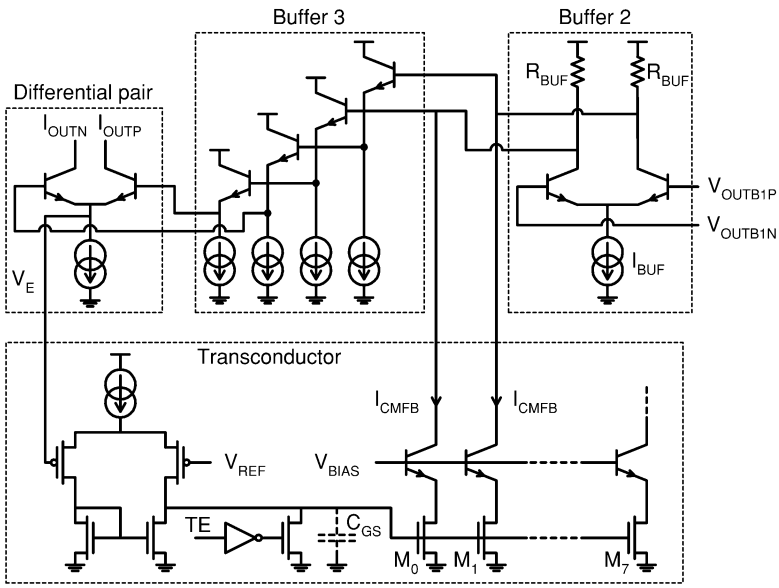


Fig. 5. Common mode feedback loop.

the one in Fig. 4 are used to switch $I_{\rm MOD}$ and $I_{\rm BIAS}$ to guarantee a fast enabling/disabling of the laser current. In this architecture, low $I_{\rm BIAS}$ or $I_{\rm MOD}$ currents are concentrated in one differential pair, whereas the largest currents use eight differential pairs. Every 10 mA an extra differential pair is used so the current range of every differential pair is limited assuring fast operation. Buffer 1 is comprised of two emitter followers (one for every input) buffering the inputs and performing a level shift (see further). The outputs of Buffer 2 (shown in Fig. 5) switch between $V_{\rm DD}$ and $V_{\rm DD} - R_{\rm BUF}I_{\rm BUF}$. Each of the outputs of Buffer 2 connects to a cascade of 2 emitter followers driving the differential pairs of the LDS as shown in Fig. 5.

Besides optimizing the current range of the differential pairs it is also needed to maximize their $V_{\rm CE}$. This is done by minimizing the emitter voltage $(V_{\rm E})$ as the collector voltage (V_C) depends on external factors (e.g., the LD). The $2V_{\rm BE}$ level shift in Buffer 3 is insufficient and temperature dependent so the common mode feedback (CMFB) loop shown in Fig. 5 was added. The CM level of Buffer 2 (and consequently $V_{\rm E}$) is lowered by drawing the $I_{\rm CMFB}$ current from the collector resistances $(R_{\rm BUF})$. For a loop gain $\gg 1$, the emitter voltage $V_{\rm E} = V_{\rm DD} - 3V_{\rm BE} - R_{\rm BUF}I_{\rm CMFB}$ equals $V_{\rm REF}$ which was chosen 400 mV, which ensures that the bipolar transistors making the current sources (I_0 to I_7) in Fig. 4 are still in the forward active region.

Drawing the $I_{\rm CMFB}$ current from the $R_{\rm BUF}$ resistors of Buffer 2 however lowers the $V_{\rm CE}$ of the differential pair in Buffer 2 and slows it down. For this reason Buffer 1 was added. In the design of Buffer 2 a trade off was made between power consumption and speed (1.25 Gb/s). The lower the resistance of $R_{\rm BUF}$ the faster the buffer, but the higher the $I_{\rm BUF}$ and $I_{\rm CMFB}$ currents required. We selected $R_{\rm BUF} = 1200\ \Omega$ and $I_{\rm BUF} = 250\ \mu$A.

The CMFB loop, shown in Fig. 5, operates as an integrating feedback loop. The error voltage $(V_{\rm E} - V_{\rm REF})$ is converted to a current by a simple transconductor. This current is integrated on the combined gate-source capacitance $(C_{\rm GS})$ of eight large

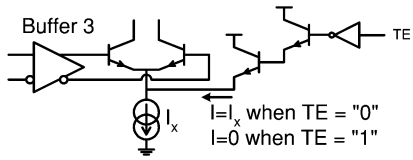


Fig. 6. Disabling feature.

nMOS transistors ($\rm M_0$ to $\rm M_7$), which generate the $I_{\rm CMFB}$ currents. A small cascode npn transistor is added to isolate the large nMOS transistors ($\rm M_0$ to $\rm M_7$) in order to minimize the output capacitance of the $I_{\rm CMFB}$ current sources, because this capacitance is shunting the high-frequency data path. The peak $I_{\rm CMFB}$ currents generated by $\rm M_0$ to $\rm M_7$ are up to 1.061 mA providing a voltage shift of 0.919 V.

Using the TE signal can save a significant amount of power. The CMFB is disabled by discharging $C_{\rm GS}$ when $\rm TE = $ "0". When the data path is disabled then $V_{\rm INP}$ equals $V_{\rm INN}$ by which the $I_{\rm MOD}$ and $I_{\rm BIAS}$ currents are not forced to the negative current output of the LDS, which would result in light to be emitted. For this reason we added the disabling circuitry, shown in Fig. 6, to the LDS. This disabling feature is also active at start-up to avoid accidental light emission until all blocks are initialized. The total enabling time is less than 110 ns which is short enough for an FSAN GPON compliant BMLD.

Both $I_{\rm MOD}$ and $I_{\rm BIAS}$ are set by a 10-bit digital code. The LDS comprises eight separate current sources (I_0 to I_7 in Fig. 4) in a custom designed DAC architecture. The current DACs are not located under the differential pairs of the LDS, because the output capacitance of the DAC would deteriorate the current switching behavior of the LDS. A cascode transistor could solve this problem but the extra voltage drop cannot be tolerated ($V_{\rm E}$ can be as low as 300 mV). So the DAC currents are transferred to the differential pairs via current mirrors (Fig. 7) built with fast npn transistors, to not deteriorate the settling time of $I_{\rm BIAS}$ and $I_{\rm MOD}$. A ratio of 12 was selected as a compromise between DAC settling time and power consumption. An nMOS follower

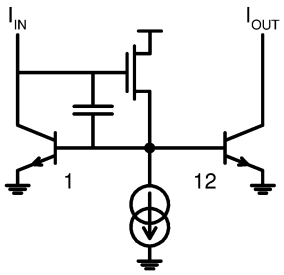


Fig. 7. Current mirror for the tail currents of the differential pairs.

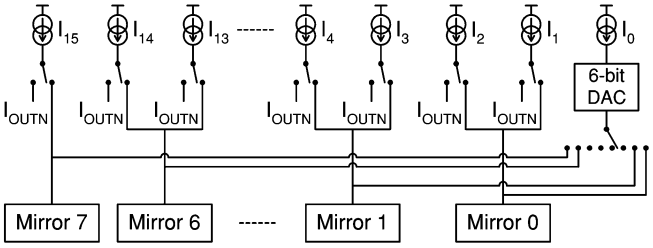


Fig. 8. 10-bit current DAC architecture.

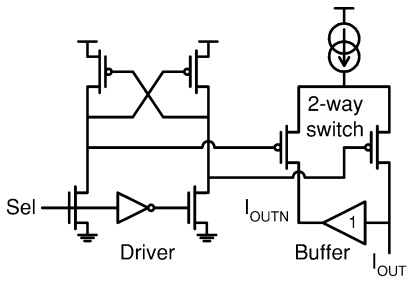


Fig. 9. Two-way switch with driver and buffer.

TABLE I
SPECIFICATIONS AND PARAMETERS RELATED TO THE LM BLOCK

Parameter	Specification
PD capacitance	up to 15 pF
PD coupling factor	25 µA/mW to 1400 µA/mW
PD tracking error	up to ± 1.5 dB
Loss WDM filter (separating upstream and downstream traffic)	0.5 dB to 1.5 dB
Optical "0" level (bias)	-13.5 dBm
PLM: optical "1" level settings	-2.5 / 0.5 / 3.5 dBm
Target I_{PD} "0" level (obtained after calibration at room temperature)	1.25 µA to 88 µA
Target I_{PD} "1" level (obtained after calibration at room temperature)	15.8 µA to 4427 µA
Worst-case I_{PD} range	0.89 µA to 5574 µA
Average optical power variation [1]	± 2.5 dB
Extinction ratio [1]	> 10 dB
Available pattern to perform both a "0" and a "1" level measurement	10 bytes at 1.25 Gbit/s

delivers the considerable base current, assuring a fast response at the cost of an extra current source (100 μA) in the follower. A gate-source capacitor is added for high-frequency stability [5].

I_{BIAS} and I_{MOD} are composed of eight currents, each supplied by a different current mirror with a certain degree of mismatch. Fortunately only a monotonic behavior has to be guaranteed because the DACs are in the APC loop that controls the I_{MOD} and I_{BIAS} settings. By consequence we designed for a differential nonlinearity (DNL) <1 LSB (least significant bit). The settling time, measured after the current mirrors, is less than two bytes at 1.25 Gb/s (12.8 ns). This allows for a fast initialization of the optical power by a binary-like search algorithm and an update of the currents during the short "guard time" (4 bytes at 1.25 Gb/s) separating consecutive bursts.

The DAC must source current into the npn current mirrors. The segmented current steering architecture of Fig. 8 shows 16 current sources (I_0 to I_{15}) and a 6-bit current dividing DAC, compatible with the LDS architecture (Fig. 4). The 6-bit current dividing DAC is always connected to current source I_0. Switching the 6-bit DAC from current source to current source as in [6] would be better for the DNL but this makes the settling time long as the number of switches increases and the decoder becomes more complex. The 4 most significant bits (MSB) control the connections to the current mirrors whereas the 6 LSBs control the 6-bit current dividing DAC. The switching scheme is such that the DAC is monotonic if the matching of I_0 to I_{15} and the linearity of the 6-bit current dividing DAC are appropriate, independent of the mismatch of the different npn current mirrors, and these requirements are easily met.

The 6-bit DAC is a simple pMOS current divider. Every fraction has its own nine-way switch (to one of the eight current mirrors or to I_{OUTN}) because this yields faster settling. Current sources I_0 to I_{15} are 437.5 μA and generated by a (low-voltage) pMOS cascode mirror. Currents I_1 to I_{15} are switched to either I_{OUTN} or to a particular current mirror by the switch shown in Fig. 9. The driver reduces the cross-point voltage of the control signals (Sel and the inverted Sel) so that the voltage swing at the drain of the current source is reduced during switching [7]. We further improved the speed by using a unity-gain buffer to make the voltage at I_{OUTN} equal to the voltage at I_{OUT} [8]. This makes a considerable difference because I_{OUT} is fed into a current mirror of which the input voltage varies with the current. The buffer guarantees that the voltage at I_{OUTN} equals the voltage at I_{OUT} so that parasitic capacitances charge or discharge less when switching.

Some simple combinatorial logic makes the 10-bit input code 0 when $\mathrm{TE} =$ "0" to reduce power consumption in the LDS when no I_{BIAS} or I_{MOD} current is required.

III. LEVEL MONITORING

A. Introduction

In contrast to continuous wave laser drivers, a BMLD cannot regulate its emitted power by means of a slow averaging measurement (no stable average power available). Moreover an equal repartition of "0" and "1" bits is not guaranteed for upstream transmissions in a GPON. By consequence the APC is based on discrete measurements of the optical "0" and "1" power performed by the LM block. The photocurrent is not measured directly but compared with $I_{\mathrm{REF\_"1"}}$ and $I_{\mathrm{REF\_"0"}}$. The main speed-limiting factor of the LM circuitry is the parasitic capacitance of the monitor PD (C_{PD}). The specifications of the LM block are summarized in Table I. Due to the relatively high C_{PD} value a string of successive "0" or "1" bits is required to detect small changes in the optical "0" and "1"

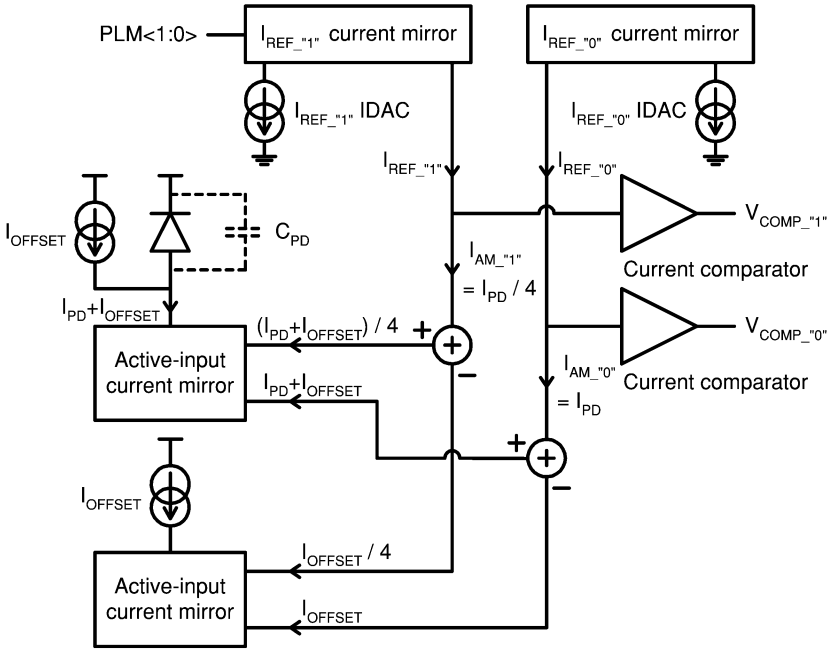


Fig. 10. Improved level monitoring architecture.

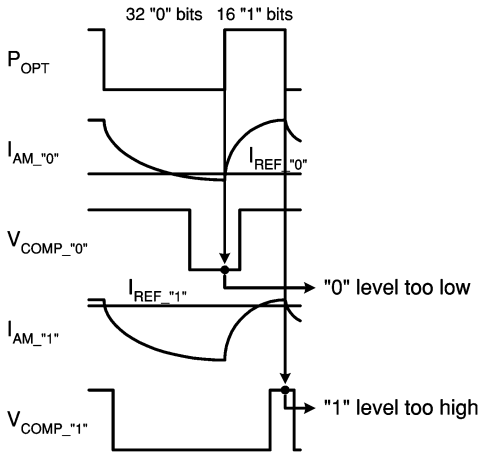


Fig. 11. Simplified description of level monitoring.

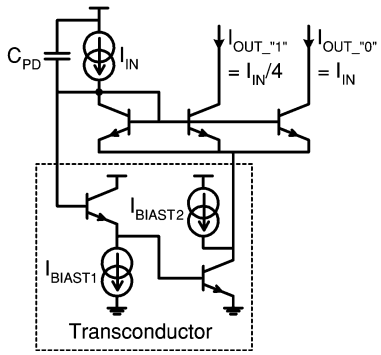


Fig. 12. Active-input current mirror.

power. These strings can be programmed in a GPON PLOAMu (physical layer operation administration and maintenance upstream) field, where up to 10 bytes of "data" can be used for tracking the launched optical power [9]. Consequently, the LM is the most critical block of the APC because it handles a very wide range of photocurrents on a relatively short timescale and despite a high $C_{\rm PD}$.

B. Circuit Description

The concept of the current-mode LM is shown in Fig. 10. Simplified waveforms of the operation are shown in Fig. 11. An active-input current mirror reduces the impact of $C_{\rm PD}$ by clamping the input node to a given voltage $(V_{\rm CLAMP})$, so that this capacitance does not introduce unacceptable delays. The mirror produces two copies of the photo current, one to be used for the "0" level measurement and another, divided by four, for the "1" level measurement. An offset current $(I_{\rm OFFSET})$ was added to the photocurrent to increase the speed of the active-input current mirror (see further). In this mirror the input current provides the base currents. However, these base currents are temperature dependent, thus impacting the accuracy. For this reason a second, identical current mirror was added to compensate the temperature variation of the most important base currents (e.g., resulting from $I_{\rm OFFSET}$). Otherwise this variation would deteriorate the accuracy of the smallest photocurrents. The outputs of both current mirrors are subtracted, which gives the $I_{\rm AM\_"0"}$ and the $I_{\rm AM\_"1"}$ currents in Figs. 10 and 11. A current comparator compares $I_{\rm AM\_"0"}$ to $I_{\rm REF\_"0"}$ and a second comparator compares $I_{\rm AM\_"1"}$ to $I_{\rm REF\_"1"}$. For the PLM we multiply $I_{\rm REF\_"1"}$ by 2 (thus increasing the "1" level by 3 dB) for PLM state 1 and by 4 (thus increasing the "1" level by 6 dB) for PLM state 2, while $I_{\rm REF\_"0"}$ is not changed. At the end of a pattern of sufficiently long consecutive 0's or 1's a valid measurement is present at the output of one of the current comparators $(V_{\rm COMP\_"0"}, V_{\rm COMP\_"1"})$. A single calibration of each reference current at room temperature takes all absolute errors into account (offsets, base currents etc.). Consequently, the accuracy of the APC is determined by the variation of the absolute

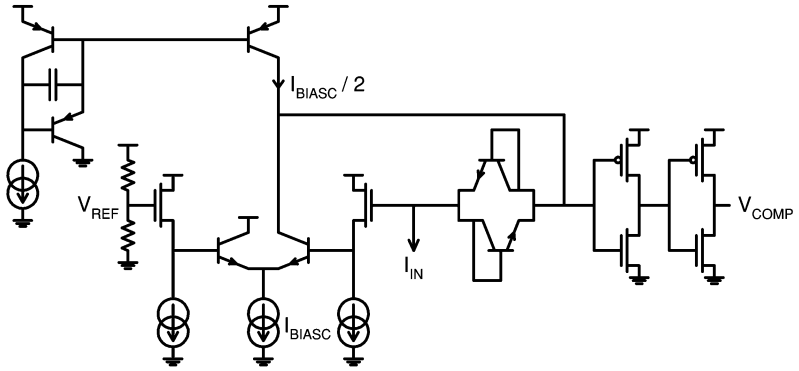


Fig. 13. Current steering current comparator.

errors over temperature and supply. Extensive Monte Carlo simulations evaluated the APC performance.

The proposed active-input current mirror is shown in Fig. 12. It produces two currents, $I_{\text{OUT\_"0"}}$ to be used for the "0" level measurement, $I_{\text{OUT\_"1"}}$ for the "1" level measurement. The use of a conventional OTA, as in [10] and [11], was avoided because this would result in high power consumption (even for low input currents) because the bias current in the OTA should be high enough for driving more than 10 mA. A single transistor (biased by $I_{\text{BIAST2}} = 1$ mA), preceded by an emitter follower (biased by $I_{\text{BIAST1}} = 50\ \mu$A) was used, as shown in Fig. 12, clamping the input node to $2V_{\text{BE}}$. This is possible because it does not matter to which voltage the input is clamped (as long as there remains enough inverse voltage across the monitor PD). The proposed active-input current mirror is very simple but very fast and power efficient as the maximum drive current does not depend on any bias current in the circuit. The time constant is inversely proportional to current at low input currents, and tends to settle for large currents [11]. By consequence large input currents pose no problems. For the worst-case C_{PD} and input current, the time constant τ can be approximated by

$$\tau = \frac{C_{\text{PD}}}{g_{\text{mi}} g_{\text{mt}} r_{\text{ot}}} \tag{1}$$

where g_{mi} is the transconductance of the diode connected input transistor, g_{mt} is the transconductance of the transistor biased by I_{BIAST2} and r_{ot} is the output resistance of the latter transistor. From (1) it is clear that the speed of the active-input current mirror can be improved by increasing g_{mi} or g_{mt}. Instead of decreasing the time constant by only increasing I_{BIAST2} (g_{mt}) we also added an offset current ($I_{\text{OFFSET}} = 20\ \mu$A) to the input current. This costs little extra power but is very effective in increasing the (worst-case) speed of the mirror. Unfortunately the I_{OFFSET} current should be chosen rather small compromising speed versus accuracy. The simulated worst-case bandwidth of the active-input current mirror is 103.2 MHz for a C_{PD} of 15 pF at 1 μA input current. For an identical-sized simple bipolar current mirror this bandwidth is only 0.3 MHz.

The current comparator features a maximum input signal of 5.5 mA and a zero offset. As shown in Fig. 13, it has the same operating principle as [12]. The current comparator employs nonlinear feedback. For small changes of the input current around the quiescent point ($I_{\text{IN}} = 0$), the diodes are off, so that the equivalent resistance at the input node is large and, consequently, the circuit preserves the high-resolution feature of a capacitive input. For larger positive (negative) currents, V_{IN} decreases (increases) and the transconductor $(\text{differential pair} + I_{\text{BIASC}}/2\ \text{current source})$ turns on one of the diodes, closing a feedback loop. So the current comparator combines the advantages of capacitive and resistive input architectures: high resolution and reduced delay for low current levels, and reduced input voltage excursion for large current levels. Due to the integrating feature in the transition region virtually zero current offset is obtained (the only offset term is due to leakage currents) without relying on precise device matching. Depending on the sign, the input current will flow through one of the diodes so that the voltage at the input of the cmos inverters is $V_{\text{REF}} + V_{\text{BE}}$ or $V_{\text{REF}} - V_{\text{BE}}$. This $2V_{\text{BE}}$ voltage swing is high enough to be converted to a CMOS signal by a simple CMOS inverter with a switching point equal to V_{REF}. As the switching point changes with the supply voltage, a resistive divider is used to make the V_{REF} voltage so that the delay changes very little with the supply voltage. The V_{REF} is chosen 2 V to leave sufficient headroom for the I_{BIASC} current source. The current necessary to charge the parasitics of the diodes is supplied by the transconductor so that the charging current is much larger than the input current. An npn differential pair is chosen for speed, and preceded by small (low capacitance) nMOS followers so that no base current is subtracted from I_{IN}, as this would result in an offset current for the current comparison. The $I_{\text{BIASC}}/2$ current is generated by a pnp mirror, because the pnp transistors add less parasitic capacitance to the input of the inverters.

A disadvantage of this current comparator is that I_{BIASC} must be large enough, as the maximum/minimum input current is $\pm I_{\text{BIASC}}/2$. The input current of the "0" level current comparator can reach 5.5 mA (the maximum I_{PD} during the "1" bits), which results in a rather high power consumption for this comparator. However the PLM setting is known so that I_{BIASC} is scaled accordingly and the current comparator can be disabled when no data is transmitted. Notwithstanding its power consumption we used a current steering current comparator because of its much better transient response over current switched current comparators [13]. This transient response is very important as the sign of a small current has to be detected following a large input current (e.g., the "0" pattern is always preceded by at least one "1").

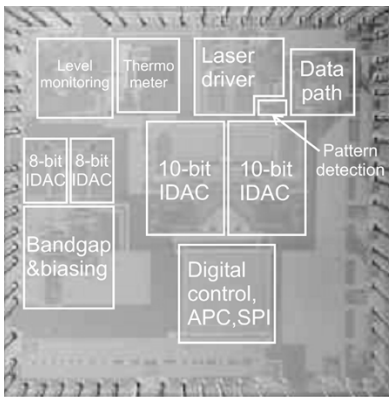


Fig. 14. Die micrograph.

TABLE II
MEASURED POWER CONSUMPTION OF THE COMPLETE BM-TX FOR THE DIFFERENT MODES OF OPERATION

Mode of operation	Power consumtion (mW)
TE = "0"	294
PLM state 0 (P_{AVG} = -5.5 dBm)	512
PLM state 1 (P_{AVG} = -2.5 dBm)	536
PLM state 2 (P_{AVG} = +0.5 dBm)	579

IV. RESULTS

The presented BMLD chip was fabricated in a five-metal 0.35 μm SiGe BiCMOS process with vertical isolated pnp transistors. The npn transistors feature an f_{T} at 1.5 V of 45 GHz, an $f_{\max}$ at 1.5 V of 60 GHz and a $\mathrm{BV_{CEO}}$ of 3.6 V. Fig. 14 shows the die micrograph. The die, sized 4 by 4 mm, is housed in a 68-pin VFQFPN package. The die is placed asymmetrically in the die cavity to reduce the parasitic inductance of the I_{MOD} bond wires. Extra test pins were bonded out for the extensive evaluation of this chip. Table II gives an overview of the measured power consumption of the complete 3.3-V BM-TX (including the BMLD, the LD, etc.).

A. Laser Driver

Several 1.25 Gb/s optical eye diagrams corresponding to different temperatures for a $(2^{15}-1)$ pseudorandom bitstream (PRBS) are shown in Fig. 15. The diagrams were measured after a fourth-order Thomson filter (cutoff frequency 933 MHz) for a bias level of -13.5 dBm and an average level of -5.5 dBm, and fall nicely into the mask specified in the ITU-T G.984.2 recommendation [1]. The burst turn-on and turn-off (measured with another lightwave converter) are shown in Fig. 15(d) and (e) respectively. The bias level is reached within 16 pre-bias bits. The disabling of the bias takes about 6 bits. This is faster than the maximum allowed transmitter enabling and disabling time specified in G.984.2 as 16 bits each at 1.25 Gb/s. Fig. 16 shows the measured performance of the CMFB loop. The CMFB loop compensates the temperature and the supply variations very well. V_{E} varies only about 50 mV, without CMFB V_{E} would vary about 1 V. V_{E} still depends on the supply voltage $(V_{\mathrm{DD}} = 3.3\ \mathrm{V} \pm 5\%)$ because a voltage divider (dividing V_{DD}) was used to make the V_{REF} voltage, an approach that is accurate enough for this purpose. Fig. 17 shows the DNL of one of the tested current DACs to be smaller than 0.3 LSB. Two

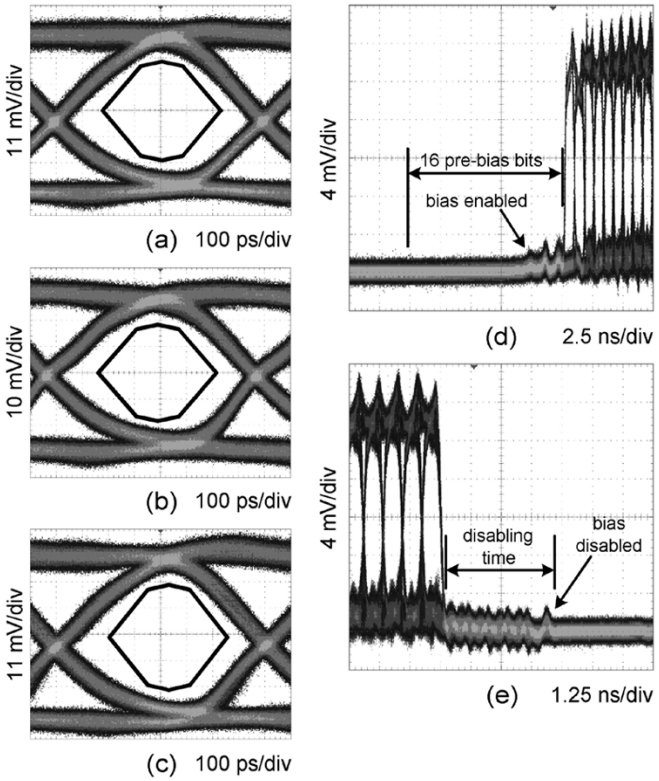


Fig. 15. Waveforms at 1.25 Gb/s: (a) eye diagram at room temperature; (b) eye diagram at $-40\,^{\circ}$C; (c) eye diagram at 85 °C; (d) burst turn-on; (e) burst turn-off.

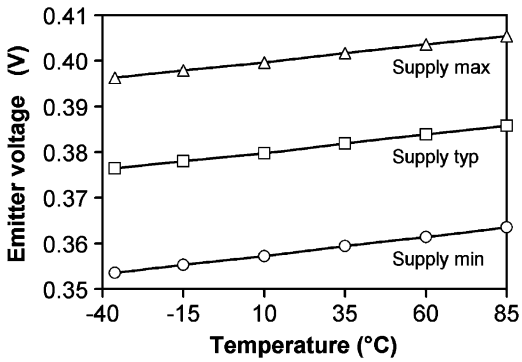


Fig. 16. CMFB: V_{E} as a function of the ambient temperature.

other 10-bit DACs showed a DNL smaller than 0.5 LSB. All tested DACs are monotonic as required.

B. Level Monitoring

Extensive Monte Carlo simulations evaluated the APC performance. The worst-case situation for the speed and accuracy of the LM circuitry occurs for a C_{PD} of 15 pF, and for the minimum target I_{PD} currents (1.25 μA for the "0" level, and 15.8 μA for the "1" level). For each Monte Carlo run, $I_{\mathrm{REF\_"0"}}$ and $I_{\mathrm{REF\_"1"}}$ is calibrated so that the APC loop regulates to the target photocurrents at room temperature and typical supply voltage, followed by an emulation of the normal APC operation for different temperatures ($-40/35/110\,^{\circ}$C) and supply values $(3.3\ \mathrm{V} \pm 5\%)$. Table III summarizes the results of these Monte Carlo simulations. The simulation bench contains the most critical blocks with respect to the speed and accuracy of the APC loop, i.e., the schematics of all the blocks shown in Fig. 10 except

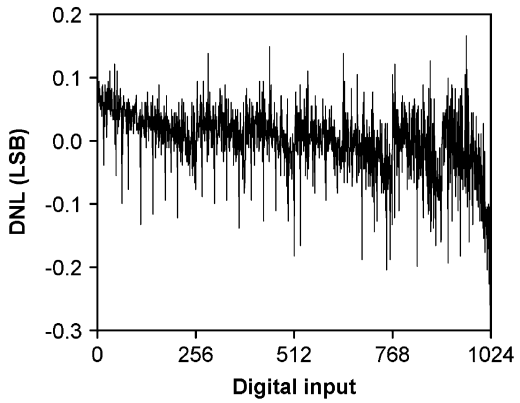


Fig. 17. DNL 10-bit current DAC.

TABLE III
MAXIMUM VARIATION OF THE AVERAGE OPTICAL POWER (P_{AVG}) AND MINIMUM EXTINCTION RATIO (ER) OVER 250 MONTE CARLO SIMULATIONS OF THE MOST CRITICAL BLOCKS IN THE LM FOR DIFFERENT CONTROL PATTERNS USED TO PERFORM THE LEVEL MEASUREMENTS

Control pattern @ 1.25 Gbit/s	maximum ΔP_{AVG}	minimum ER
32 "1" bits + 48 "0" bits	0.1 dB	10.4 dB
16 "1" bits + 32 "0" bits	0.6 dB	10.5 dB

for the $I_{\mathrm{REF\_"0"}}$ and $I_{\mathrm{REF\_"1"}}$ current DAC. The other blocks in the APC loop (such as the digital block, the laser driver, the laser module) were ideally modeled in VerilogA. These simulations show that the newly designed level monitoring circuitry is very fast and accurate, even in the worst-case conditions.

The launched optical power tolerance of a Mitsubishi FU-445SDF LD, driven by the BMLD chip, was tested over the full temperature range. For these tests the pattern detection was programmed to sample the current comparators at the end of a string of two successive bytes of 1's and 4 successive bytes of 0's. The bias level was calibrated to -13.5 dBm and the high level to -2.5 dBm. For this LD these levels correspond to a target I_{PD} current of 10.8 μA for the "0" level and 136.4 μA for the "1" level. The variation of the average emitted power over ambient temperature (-40 °C to 85 °C) and supply range ($3.3\ \mathrm{V} \pm 5\%$) was 0.75 dB, whereas the variation of the extinction ratio was only 0.35 dB. The tracking error of the laser module is the main contribution to the total optical power variation, and 1 dB tracking error was measured. Some mechanisms causing optical power variation have an opposite temperature dependence so that the actual variation is smaller than this tracking error.

This chip supports the PLM option. $I_{\mathrm{REF\_"0"}}$ is fixed for the higher average powers so that the extinction ratio becomes much higher than the minimum specified in [1]. The average power variation is 0.82 dB in PLM state 1 and 0.6 dB in PLM state 2. At 85 °C, the chip cannot provide sufficient current to drive the laser in the highest PLM state, so the temperature range was limited to -40 °C to 60 °C for this last measurement. This is because the laser module has a built-in series resistor of 19 Ω. Normally I_{BIAS} is fed directly to the diode or via a dedicated bias input. For this module however the bias input has a built-in inductor, which we must avoid. Otherwise the turn-on/off of the burst would be much too slow. So in this case the I_{BIAS} has to be provided via the "RF" I_{MOD} input (through the 19 Ω series resistor) thus causing an extra voltage drop up to 1.6 V at the maximum bias current, which cannot be tolerated by a 3.3-V dc-coupled laser driver.

A recent reference publication on fast and accurate LM circuitry requires 40 bits of 0's (32 ns) and 40 bits of 1's at 1.25 Gb/s [10]. This is significantly slower than the newly proposed circuitry, which requires only 32 bits of 0's (25.6 ns) and 16 bits (12.8 ns) of 1's at 1.25 Gb/s. A 0.35-μm CMOS transmitter at 155 Mb/s requires up to 31 bits of 0's (200 ns) and up to 12 bits (77 ns) of 1's [14]. A transimpedance amplifier (TIA) based approach in 0.8-μm BiCMOS for 155 Mb/s operation requires patterns that are 875 ns long [15]. A 0.5-μm CMOS chip (also for 155 Mb/s) regulates only the average optical power because no bias current is used [16]. At 1.25 Gb/s however a bias current is necessary and by consequence also a control of the "0" level.

A commercial BMLD for GPON is available on the open market [17]. This commercial component has a laser driver stage working up to 2.5 Gb/s, with a better eye diagram, less jitter, less power consumption etc. However, the APC of this commercial component only regulates the average power by controlling I_{BIAS} (I_{MOD} is constant). Over a wide temperature range (e.g., -40 °C to 85 °C), this results in very large changes of the extinction ratio. We evaluated this APC approach using the PI curves we measured for different temperatures of the LD used in our experiments. At high temperatures, I_{BIAS} is driven well above the threshold to compensate the decreasing slope efficiency of the laser characteristic, resulting in a too low extinction ratio. Based on these calculations we found that the extinction ratio becomes smaller than 10 dB at high temperatures. However, in a GPON the extinction ratio should be larger than 10 dB, so the combination of this commercial component with our LD does not comply with the ITU-T G.984.2 Recommendation for GPON over a wide temperature range [1]. Besides being compliant with the standard, our proposed APC has several other advantages such as support of the PLM mechanism, support of a very wide range of photocurrents (Table I), and aging is compensated as both I_{BIAS} and I_{MOD} are regulated.

V. CONCLUSION

A 1.25-Gb/s GPON compliant burst-mode laser transmitter has been presented and experimentally validated. The proposed laser driver operates over a wide range of operating conditions and its bias and modulation current are generated by custom designed 10-bit current DACs. The proposed level monitoring circuits are about two times faster than previous publications.

ACKNOWLEDGMENT

The authors would like to thank STMicroelectronics and Alcatel Bell for technical support as well as for their cooperation. The support of INVOMEC, IMEC, for performing the digital place-and-route is gratefully acknowledged.

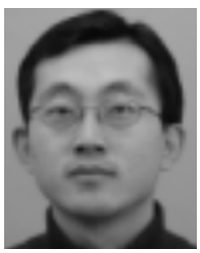
REFERENCES

[1] *Gigabit-Capable Passive Optical Networks (GPON): Physical Media Dependent (PMD) Layer Specification*, ITU-T Recommendation G.984.2, Mar. 2003.

[2] J. Bauwelinck, D. Verhulst, P. Ossieur, X. Z. Qiu, J. Vandewege, and B. De Vos, "DC-coupled burst-mode transmitter for a 1.25 Gb/s upstream PON," *Electron. Lett.*, vol. 40, pp. 501–502, Apr. 2004.
[3] H. M. Rein, "Multi-gigabit-per-second silicon bipolar IC's for future optical-fiber transmission systems," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 664–675, Jun. 1988.
[4] Y. G. Kim, F. D. Bien, J. J. Chang, M. A. Robinson, and M. Lee, "2.5 Gb/s/channel laser driver design for four-channel parallel optic transceiver using SiGe BiCMOS technology," *Electron. Lett.*, vol. 39, pp. 457–458, Mar. 2003.
[5] B. Gilbert, "Bipolar current mirrors," in *Analogue IC Design: The Current-Mode Approach*, C. Toumazou, F. J. Lidgey, and D. G. Haigh, Eds. London, U.K.: Peregrinus, 1990.
[6] J. A. Schoeff, "Inherently monotonic 12 bit DAC," *IEEE J. Solid-State Circuits*, vol. 14, no. 6, pp. 904–911, Dec. 1979.
[7] K. Lakshmikumar, R. Hadaway, M. Copeland, and M. King, "A high-speed 8-bit current steering CMOS DAC," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1985, pp. 156–159.
[8] J. Bauwelinck, W. Chen, D. Verhulst, Y. Martens, P. Ossieur, X. Z. Qiu, and J. Vandewege, "Low-output-impedance BiCMOS voltage buffer," *IEICE Electron. Express*, vol. 1, pp. 34–38, Apr. 2004.
[9] *Transmission Convergence Layer for Gigabit Passive Optical Networks*, ITU-T Recommendation G.984.3, Feb. 2004.
[10] J. Bauwelinck, D. Verhulst, P. Ossieur, X. Z. Qiu, J. Vandewege, and B. De Vos, "Current mode circuits for fast and accurate optical level monitoring with wide dynamic range," *IEICE Trans. Commun.*, vol. E87-B, pp. 2641–2647, Sept. 2004.
[11] T. Serrano-Gotarredona, B. Linares-Barranco, and A. G. Andreou, "Very wide range tunable CMOS/bipolar current mirrors with voltage clamped input," *IEEE Trans. Circuits Syst. I: Fund. Theory Applicat.*, vol. 46, no. 11, pp. 1398–1407, Nov. 1999.
[12] A. Demosthenous and J. Taylor, "High-speed replicating current comparators for analog convolutional decoders," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 47, no. 12, pp. 1405–1412, Dec. 2000.
[13] A. Rodriguez-Vazquez, R. Dominguez-Castro, F. Medeiro, and M. Delgado-Restituto, "High-resolution CMOS current comparators: Design and applications to current-mode function generation," *Analog Integrat. Circuits Signal Process.*, vol. 7, pp. 149–165, Mar. 1995.
[14] X. Z. Qiu, J. Vandewege, Y. Martens, J. Bauwelinck, P. Ossieur, E. Gilon, and B. Stubbe, "A burst-mode laser transmitter with fast digital power control for a 155 Mb/s upstream PON," *IEICE Trans. Commun.*, vol. E86-B, pp. 1567–1574, May 2003.
[15] M. Doci, C. Fiocchi, U. Gatti, A. Profumo, and G. Promitzer, "A digitally programmable burst-mode 155 Mb/s transmitter for PON," in *Proc. ESSCIRC*, Sep. 2000, pp. 212–215.
[16] E. Säckinger, Y. Ota, T. J. Gabara, and W. C. Fischer, "A 15-mW, 155-Mb/s CMOS burst-mode laser driver with automatic power control and end-of-life detection," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 269–275, Feb. 2000.
[17] *MAX3656, 155 Mbps to 2.5 Gbps Burst-Mode Laser Driver, Data Sheet*, Maxim Integrated Products, Inc., Sunnyvale, CA, 2003.

Johan Bauwelinck (S'02) was born in Sint-Niklaas, Belgium, in 1977. He received the engineering degree in applied electronics in 2000 from Gent University, Belgium, where he is currently working toward the Ph.D. degree.

He has been a Research Assistant in the INTEC_design laboratory since 2000. His research is focused on analog integrated circuits for burst-mode laser drivers in PON telecommunication systems.



Wei Chen was born in YanZhou, China, in 1974. He received the Bachelor degree of electrical engineering and Master degree of communication and signal processing from Beijing University of Aeronautics and Astronautics (BUAA), China.

From 2000 to 2002, he worked in Cellon China Group for 3G wireless communication research project. Since 2002, he has been working toward the Ph.D. degree in the INTEC_design laboratory, Ghent University. His research is focused on current digital-to-analog integrated circuits for burst-mode laser drivers of Giga-PON research project.

Dieter Verhulst (S'02) was born in Gent, Belgium, in 1978. He received the engineering degree in applied electronics in 2001 from Ghent University, Belgium, where he is currently working toward the Ph.D. degree.

He has been working at the INTEC_design laboratory in a PON research project with a focus on the high-speed digital in burst-mode laser drivers and clock phase alignment circuits.

Yves Martens was born in Brussel, Belgium, in 1976. He received the degree of civil electrical engineering from Ghent University, Belgium, in 1999. Since then, he has worked at the INTEC_design laboratory at the same University, working toward the Ph.D. degree on low-power high-performance digital circuitry for telecommunication systems (PON systems).

Peter Ossieur (S'02) was born in Brugge, Belgium, in 1977. He received the engineering degree in applied electronics from Ghent University, Belgium, in 2000. He received the Ph.D. degree in applied sciences, electronics, from the same university, in 2005.

He has been a Research Assistant in the INTEC_design laboratory since 2000. His research is focused on analog integrated circuits for burst-mode laser drivers and receivers in PON telecommunication systems and modeling of burst-mode communication.

Xing-Zhi Qiu (M'98) received the Ph.D. degree in electronics engineering from Ghent University, Belgium.

Since 1986, she has been with the INTEC_design laboratory. She is currently managing high-speed mixed analog/digital chip and subsystem design. She has accumulated 16 years of R&D experience in the field of hardware design for the physical layer, mostly developing advanced telecommunication systems and optical access network demonstrators. She is an author or co-author of 70 international publications.

Jan Vandewege (M'96) was born in Gent, Belgium, in 1949. He received the electronic engineering and the Ph.D. degrees from Ghent University, Belgium, in 1972 and 1978, respectively.

In 1985, he founded the INTEC_design laboratory, to train Ph.D. level electronic engineers in design of telecom and RF hardware and embedded software. He has authored or co-authored 134 international publications and 10 international patents in the field of telecommunication.