

Finally the output voltage V_{out} is the drain-source voltage of M_5

$$V_{out} = R_{DSM_5}(kI_B + I_2) \simeq M \frac{[k + (1 + aV_{in}/2)^2]}{[k + (1 - aV_{in}/2)^2]} \quad (9)$$

where M is a constant. Note that the approximation range can be tuned by means of parameter a via I_B . Alternatively, the resistor R_1 can be also implemented by diode connected transistors [1, 2], at the expense of an increase of power consumption. The number of transistors and power consumption employed in the design of Fig. 2 are less than half and 16 times lower, respectively, than the circuit in [2]. Moreover, this novel approach allows a direct implementation in voltage-mode circuits with efficient power consumption owing to the inherent class-AB operation and high dB range.

Measurement results: To verify the design of Fig. 2, measurement results from a practical prototype fabricated in a $0.5 \mu\text{m}$ CMOS technology have been obtained. The supply voltage employed was $\pm 750 \text{ mV}$, and the total occupied area excluding pads was 0.047 mm^2 . The current I_B was set to $5 \mu\text{A}$, and the factor $k=0.2$. The power consumption was less than $40 \mu\text{W}$. The transistor aspect ratios (W/L) employed were M_1 to M_3 (75/1.2), M_4 (50/0.6), and M_5 (7/1.2). Resistor R_1 was $2 \text{ k}\Omega$, and the capacitances were 1 pF . To avoid the initial charge trapped in the floating gates during fabrication, the technique described in [4] was employed. Fig. 3a shows the measured output voltage V_{out} using a linear scale in the Y-axis for an input range from -0.85 to 0.85 V . This fact is possible owing to the capacitive division at the input floating gates allowing an input range higher than the supply voltage. The output range is about 1 V . To provide more insight into the exponential behaviour Fig. 3b shows a dB scale of Fig. 3a for the same input range, where a large range of approximately 52 dB with errors less than 2 dB can be noted. To improve such figures it is possible to increment the bias current I_B in Fig. 2, but this increase will reduce the dB range. For example, injecting a current $I_B = 10 \mu\text{A}$ we obtain errors less than 1 dB in a range of 47 dB .

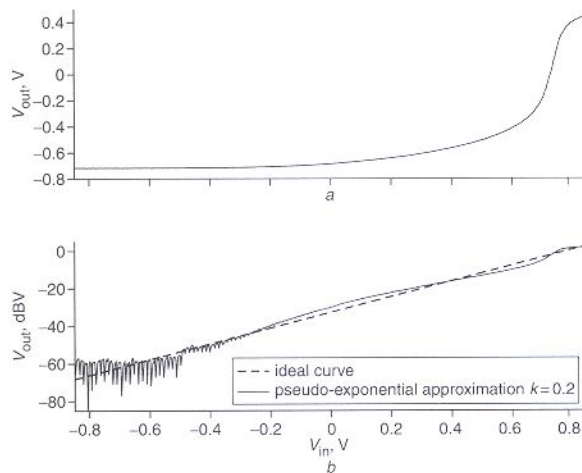


Fig. 3 Measurement results of pseudo-exponential circuit
a Output voltage for $I_B = 5 \mu\text{A}$ and $k = 0.2$
b Comparison between measurement results and ideal curve

Conclusion: A novel implementation of an exponential voltage to voltage converter is presented. The circuit features a rail-to-rail input range owing to the inclusion of floating gates. The proposed circuit is based on an alternative approximation that leads to a significantly large range. The terms of such an approximation were derived employing the inherent nonlinear currents of a class-AB transconductor. The EVVC is compact and power-efficient with a high dB range.

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High-speed active-input cascode current mirror

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A high-speed active-input cascode current mirror is presented. The proposed configuration combines a high output impedance with the high-frequency performance of a source- or emitter-driven active-input topology. Simulation results in a $0.35 \mu\text{m}$ SiGe BiCMOS are presented to demonstrate the validation of the proposed current mirror. A much higher (about 30 to 40 times) output impedance is achieved, with no degradation in the high-frequency behaviour compared to conventional emitter-driven active-input current mirrors, without increasing the power consumption. The proposed configuration can be applied to both bipolar and CMOS technology.

Introduction: In current-mode signal processing circuits current mirrors are often used to replicate current signals. It is not unusual that a wide range of current levels must be handled. Active-input current mirrors (AICMs) clamp their input node to a particular voltage so that the delay introduced by a high parasitic capacitance (C_P) at that node is significantly reduced, especially for low input currents [1]. AICMs are used for a wide range of applications, e.g. the processing of currents generated by silicon retinas [1] or photodiodes [2], or current-mode A/D converters [3].

A cascode AICM, shown in Fig. 1a, is described in [4]. A very high output impedance is demonstrated, however care must be taken to ensure the stability of the feedback loop, which is disadvantageous for high-speed operation [5]. The stability can be significantly improved by using a source- or emitter-driven topology, shown in Fig. 1b, which results in better high-frequency performance [1].

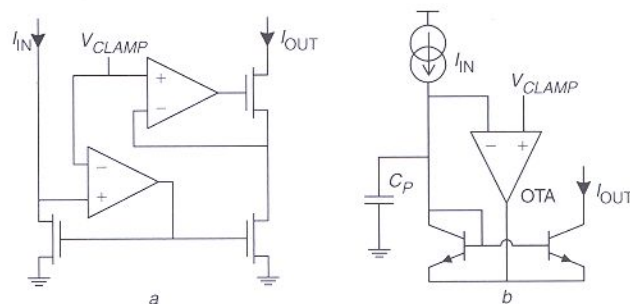


Fig. 1 Active-input regulated cascode current mirror, and conventional emitter-driven active-input current mirror

a Active-input regulated cascode current mirror

b Conventional emitter-driven active-input current mirror

A simple but very fast and efficient emitter-driven AICM, shown in Fig. 2a, was previously proposed by the author in [2]. This mirror, clamping the input node to $2V_{BE}$, has very good performance, however the output impedance may not be good enough for certain other applications. In this Letter we propose an active-input cascode current mirror (AICCM), shown in Fig. 2b, which combines high output impedance with very good high-frequency performance, despite a high parasitic capacitance at the input node.

Proposed active-input cascode current mirror: The proposed AICCM, shown in Fig. 2b, can be derived from the conventional emitter-driven AICM, shown in Fig. 2a, by splitting the transconductor transistors and the I_{BIAS2} current source in parallel parts and by removing the connection of the emitters of the current mirror. The bottom transistors now serve the dual purpose of transconductor and mirror transistors whereas the upper transistors now simply operate as cascode transistors. A much higher output impedance is obtained whereas the saturation voltage remains the same. Care must be taken to include the mismatch of the I_{BIAS2} current sources when analysing the accuracy of the AICCM. However, these are DC current sources so their size does not impact the speed of the mirror unless the output capacitance would be too high, which can be easily solved by adding a cascode transistor in the I_{BIAS2} sources. The concept can be used in CMOS as well, however by using the same technology as the previous design it was possible to make a straightforward comparison.

Simulation results: SPICE simulations of an implementation in a $0.35\ \mu\text{m}$ SiGe BiCMOS process have been carried out to show the improvement of the proposed AICCM, with respect to the previous work (Fig. 2a). We compared both circuits for the same power consumption. The sum of the I_{BIAS2} current sources in Fig. 2b equals the I_{BIAS2} current source (1 mA) in Fig. 2a and the transconductor transistors are also split in the same way.

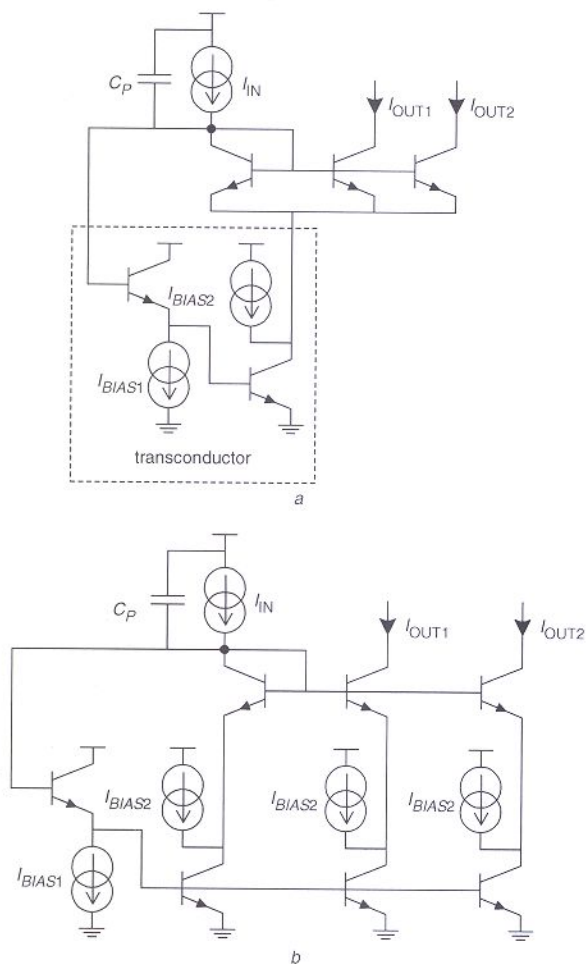


Fig. 2 Conventional active-input current mirror proposed in [2], and proposed active-input cascode current mirror

a Conventional active-input current mirror proposed in [2]
b Proposed active-input cascode current mirror

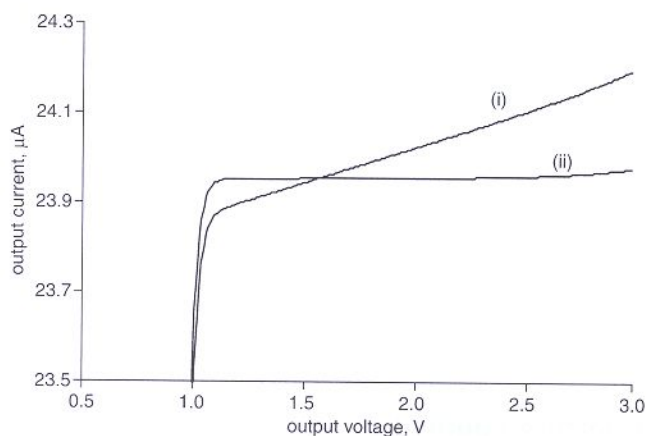


Fig. 3 I_{OUT} against V_{OUT} curve for $I_{IN} = 25\ \mu\text{A}$

(i) conventional emitter-driven AICM
(ii) proposed AICCM

Fig. 3 shows a typical I_{OUT} against V_{OUT} curve for $I_{IN} = 25\ \mu\text{A}$. It is clear that the proposed AICCM has a much better output impedance than the conventional AICM. The output impedance corresponding to curve (i) is $6.4\ \text{M}\Omega$, whereas the output impedance of curve (ii) is $256.6\ \text{M}\Omega$. Over an input current range from 10 to $5500\ \mu\text{A}$, the improvement varies between 32 and 44.

Fig. 4 shows a typical step response from 20 to $100\ \mu\text{A}$ with a $20\ \text{pF}$ input capacitance. Curves (ii) and (iii) coincide almost perfectly, implying no degradation in the frequency behaviour.

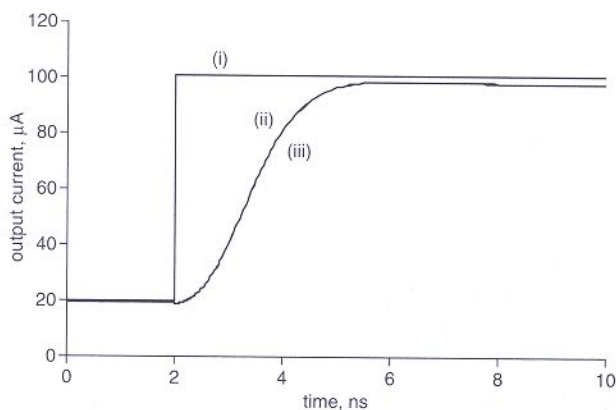


Fig. 4 Step response from 20 to $100\ \mu\text{A}$ for $C_P = 20\ \text{pF}$

(i) I_{IN}
(ii) conventional emitter-driven AICM
(iii) proposed AICCM

Conclusion: The proposed active-input cascode current mirror shows much higher (about 30 to 40 times) output impedance, with no degradation in the high-frequency behaviour compared to conventional emitter-driven active-input current mirrors, without increasing the power consumption. The proposed configuration can be applied to both bipolar and CMOS technology.

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Aperture coupled to stripline antenna element for integrated antenna arrays

K. Wincza, S. Gruszczynski and K. Sachse

A new stripline-fed aperture coupled antenna element is proposed. An additional slot in a ground plane allows achievement of efficient electromagnetic coupling with the radiating element and good return loss of the antenna fed by a stripline. The described radiating elements can be easily integrated with a feeding network designed in the most commonly used stripline technique when a large antenna array is to be developed.

Introduction: Patch antennas are widely used in modern telecommunications [1]. The main advantages of such radiating elements are: ease of designing large antenna arrays, lightweight structure and low manufacturing cost. Common microstrip patch antenna elements [2] can be easily integrated with a feeding network designed in the microstrip technique. The main advantage of this technique is the construction's simplicity. However, some microwave circuits of the feeding network are difficult to realise in a microstrip technique, e.g. 3 dB coupled-line directional couplers, being the key element of many feeding networks, cannot be straightforwardly designed in this technique. Another common technique in which feeding networks are designed is the stripline technique. Compared with the microstrip one, it provides many advantages for designers, but only a few strip antenna element apertures coupled to a stripline have been described in the literature. In [3] a stripline-fed antenna element is proposed in which vias around the coupling slot are placed to ensure a good return loss. A similar solution is proposed in [4], where a double-patch radiating element aperture is coupled to a highly asymmetric stripline using also shorting pins around the coupling slot. In other solutions, e.g. presented in [5], stripline-fed antennas with a slot as a radiating element are described. In this Letter we propose a new stripline-fed, fully planar aperture coupled antenna element designed in the stripline technique without the use of shorting pins or vias around the coupling slot. Such strip radiating elements can be easily integrated with feeding networks designed in the most commonly used stripline technique, constituting high performance fully planar large antenna arrays.

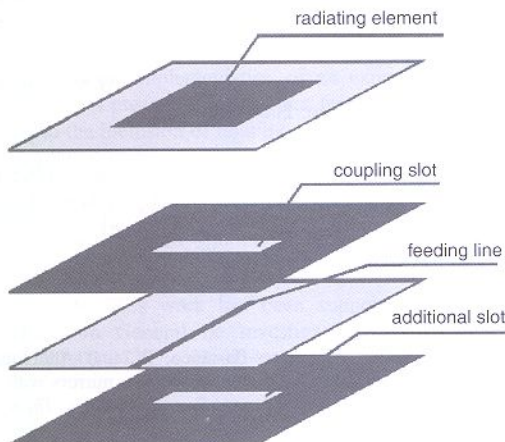


Fig. 1 New stripline-fed aperture coupled antenna element

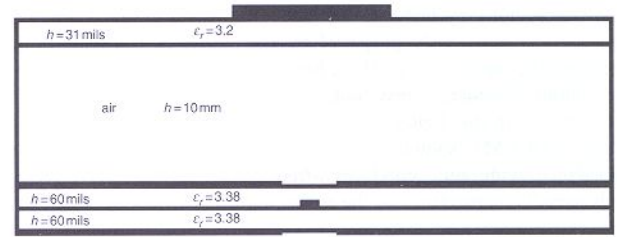


Fig. 2 Cross-sectional view of structure used for design of stripline-fed antenna elements

Proposed antenna element: The new stripline-fed antenna element is shown in Fig. 1. It consists of four metallisation layers separated by dielectric layers. In the top metallisation layer a radiating patch is etched. In a second layer, which is the upper ground plane of the stripline, a slot is inserted ensuring electromagnetic coupling between the feed line and radiating patch. The feed stripline is placed in the level of metallisation beneath the coupling slot. At the bottom ground plane an additional slot is inserted. This slot has the same dimensions as the coupling slot and is placed exactly underneath. This proposed modification ensures a good return loss of the antenna and a tight coupling between the stripline and radiating patch.

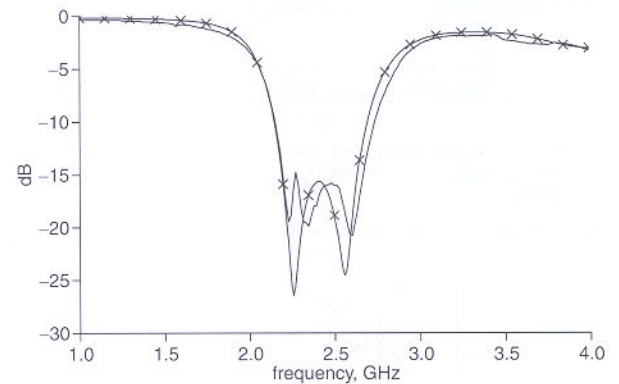


Fig. 3 Calculated and measured return loss characteristics of antenna element designed for centre frequency of $f_0 = 2.4$ GHz

× calculated
— measured

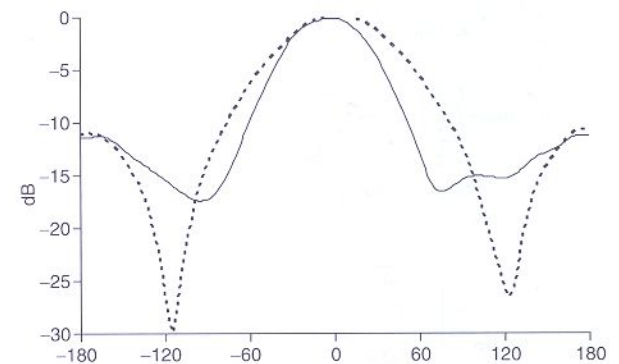


Fig. 4 Measured radiating patterns of antenna element for two principal cut-planes

— co-polar H-plane
- - - co-polar E-plane

Experimental results: To validate our concept two antenna elements for different frequency bands have been designed. Fig. 2 shows a cross-sectional view of the structure used for the presented designs. The patch was etched on a laminate with thickness $h = 31$ mils and dielectric constant $\epsilon_r = 3.2$. A 10 mm air spacer has been inserted between the radiating element and the upper ground plane to ensure appropriate bandwidth of the antenna. The feeding network consists of two layers of a laminate with $h = 60$ mils and $\epsilon_r = 3.38$, on which the network's strip pattern is etched. Fig. 3 presents calculated and measured return loss characteristics of the element designed for the centre frequency of $f_0 = 2.4$ GHz. The measured radiating patterns of