Voltage Controlled Oscillators for 40 Gbit/s Cascaded Bit-Interleaving PON

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***Abstract*—Technologies such as the Internet-of-Things and cloud services demand dynamic bandwidth allocation flexibility, which is not offered by the currently deployed solutions. The Bit-Interleaving PON (BiPON) and its cascaded extension the Cascaded Bit-Interleaving PON (CBI-PON) offer a solution that allows to increase bandwidths, reduce power consumption and have a much more flexible dynamic bandwidth allocation scheme. CBI-PON consists of multiple levels of BiPON with different line rates. For each of these line rates, clock-and-data recovery must be performed, which requires a set of different Voltage Controlled Oscillators (VCOs). This paper presents the VCOs designed for the CABINET chip, an implementation of a CBI-PON network device, allowing clock-and-data recovery for 40 Gbit/s, 10 Gbit/s and 2.5 Gbit/s line rates.**

I. Introduction

For more than two decades, the Internet has been significantly changing our society. The widespread availability of broadband access, followed by the global adoption of smartphones has made the Internet indispensable in our daily lives. Over the past few years, the number of users has only increased and content has become of higher and higher quality, such as (ultra) high definition video streaming.
Due to these trends, there is a crucial need for higher bandwidths in the metro/access networks in order to provide the required quality of service in the future.
Moreover, besides the demand for higher bandwidths, technologies such as the Internet-of-Things and cloud services give rise to new challenges for our Internet connections. For example, dynamic bandwidth allocation as implemented in the current networks does not have the flexibility required by these upcoming technologies.
However, the power consumption attributed to communication networks has been estimated to be approximately 1.8 % of the total global power consumption in 2012 [1]. Taking into account the environmental impact of the current electricity production, an important goal of next-generation networks should be significant power consumption reductions.

In the light of these future requirements, the GreenTouch Consortium developed the Bit-Interleaving PON (BiPON) protocol, introduced in [2], [3], [4], to tackle the issues regarding dynamic bandwidth allocation flexibility and power consumption that the currently deployed solutions are facing. We further developed the concept of the bit-interleaving PON and designed a cascaded extension: the Cascaded Bit-Interleaving PON (CBI-PON) and designed an Application-Specific Integrated Circuit (ASIC) called CABINET to implement the functions of the different devices used in a CBI-PON.

This paper starts with a short introduction to the concept of CBI-PON in Section II. In Section III the need for multi-rate clock-and-data recovery (CDR) in the CABINET ASIC is clarified, while Section IV presents the Voltage-Controlled Oscillators used in the multi-rate CDR. The CABINET implementation is shown in Section V. Section VI shows the measurements of the implemented VCOs on the CABINET chip. Finally, the conclusion is presented in Section VII.

II. Cascaded Bit-Interleaving PON

A. Bit-interleaving PON

The bit-interleaving PON differentiates from traditional PON protocols by the time-domain multiplexing (TDM) that is used to transmit and receive information on the network. Traditional PON protocols use a packet-based TDM, while the BiPON protocol uses a bit-based TDM, as shown in Figure 2. This allows the Optical Network Units (ONUs) to subsample the incoming data stream and operate at lower frequencies than is traditionally the case, resulting in lower power consumption. For a 10 Gbit/s BiPON, power reduction factors from 35× to 180×, were reported in [3].
Moreover, every BiPON frame was designed to incorporate a header containing payload information which directly enables the much-desired dynamic bandwidth allocation flexibility.

B. Cascaded BiPON

In an effort to further reduce the power consumption of next-generation metro/access networks, an extension of BiPON was developed, where multiple levels of Bit-Interleaving PONs are cascaded. A general overview of such a network is shown in Figure 1.

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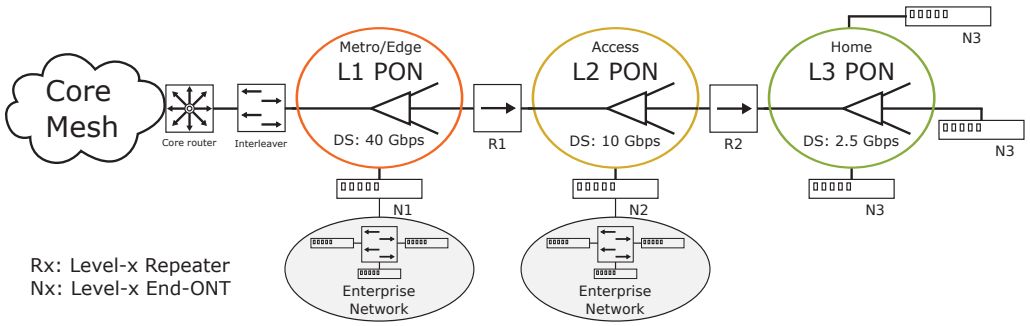

Figure 1. Cascaded Bit-Interleaving PON

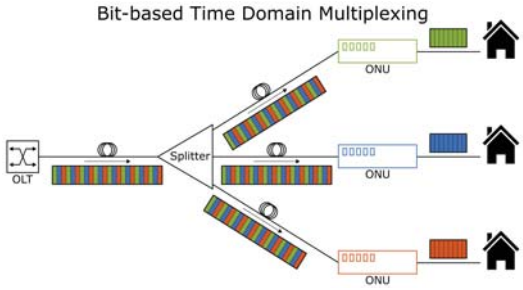

Figure 2. Bit-based TDM

This particular implementation is conducted using 3 levels of Bit-Interleaving PONs. The different levels L1, L2 and L3 operate at a line rate of respectively 40 Gbit/s, 10 Gbit/s and 2.5 Gbit/s. L1 and L2 each contains CBI Repeaters and CBI End-ONTs, while L3 only contains CBI End-ONTs. Each CBI device always does a 1:4 subsampling when receiving data, which means there is always only 1 out of 4 incoming bits that is recovered.

III. Multi-Rate Clock-and-Data Recovery

In order to reduce the deployment costs of a CBI-PON, L1, L2 and L3 Repeaters and ONUs should be implemented using the same ASIC. We have developed such an ASIC called CABINET, which is presented here.

As mentioned in Section II, the L1, L2 and L3 levels in the CBI-PON are Bit-Interleaving PONs operating at different line rates (i.e. 40 Gbit/s, 10 Gbit/s and 2.5 Gbit/s).

This means the clock-and-data recovery circuits used in CABINET should be able to recover data at these 3 different line rates. However, the on-chip processing speed of the recovered data is limited. Therefore, when receiving 40 Gbit/s, the recovered data is deserialized to 8 streams of 1.25 Gbit/s. This is not necessary when receiving 10 Gbit/s and 2.5 Gbit/s, which led to the decision of decoupling these two cases. For each case, a dedicated CDR was designed. During operation, the appropriate CDR is enabled depending on the configuration of the CABINET. This decoupling is also beneficial for the power consumption, which is now lower when receiving lower rates. The used architecture is presented in Figure 3.

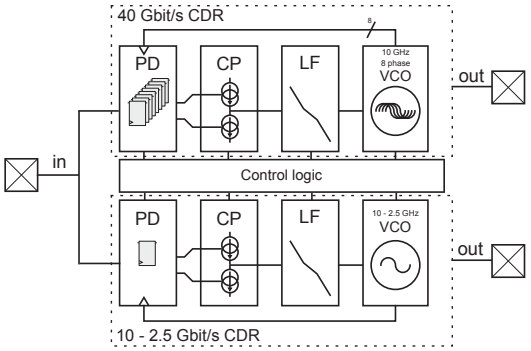

Figure 3. Dual-CDR architecture for different rates

Both CDRs are architecturally comparable, and use the same building blocks with the main exception being the Voltage-Controlled Oscillator (VCO). This paper continues to describe the implementation of the two VCOs that were designed for the two different CDRs.

IV. Voltage-Controlled Oscillators

Today, two main oscillator architectures are in use: LC oscillators and ring oscillators. LC oscillators use a resonant LC-tank, while a ring oscillator consists of a loop of delay cells that satisfies the Barkhausen criterion [5].
LC oscillators typically achieve lower phase noise, but are relatively large due to the inductor of the LC tank. Furthermore, they are known for their limited tuning range. On the other hand, ring oscillators consume only a small area and typically have large tuning ranges. Unfortunately, this is typically accompanied with a higher phase noise.

Since the phase noise requirements for CDRs are not too demanding, ring oscillators are a good choice for this application. Furthermore, ring oscillators inherently provide multiple clock phases, which is beneficial for the 40 Gbit/s CDR.

A. 40 GHz Voltage-Controlled Oscillator

As explained in Section III, the digital logic processing frequency limitation calls for a deserializing operation to 8 1.25 Gbit/s data streams. This operation requires 8 clock phases, which immediately fixes the VCO architecture to a 4 stage ring oscillator with differential delay cells, as shown in Figure 4.

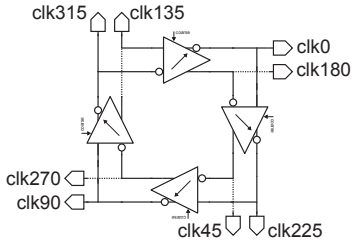

Figure 4. 40 Gbit/s VCO Architecture

The delay cell used in this VCO is shown in Figure 5. Due to the limited supply voltage in the used 40nm CMOS, tail currents were avoided to maximize the output voltage swing. A cross-coupled common source amplifier with resistive load was used, to avoid the input capacitance of the PMOS which is present in the typically used CMOS inverters. This helps to maximize the oscillation frequency.

Coarse tuning is provided by the digitally controlled resistive load, while fine tuning is implemented by means of varactors. The combination of these two mechanisms allows the desired oscillation frequency to be reached over temperature and process corners.

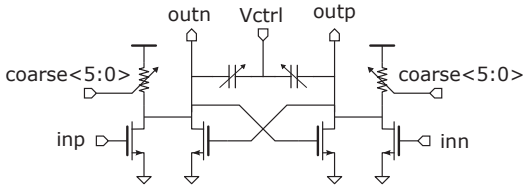

Figure 5. 40 Gbit/s VCO Delay Cell

B. 10 GHz and 2.5 GHz Voltage-Controlled Oscillator

Since no deserialization is needed for 10 Gbit/s and 2.5 Gbit/s, the VCO architecture is simplified to a 3 stage, single-ended architecture. However, two of these 3 stage rings are coupled to provide a differential output in the case of 10 Gbit/s operation, as is shown in Figure 6. To reduce power consumption for 2.5 Gbit/s operation, only one of the two rings is enabled, and the coupling of the two rings is disabled. The core VCO still oscillates at 10 GHz, which is then divided by 4 to 2.5 GHz. The divider also provides the differential output. This configuration is shown in Figure 7.

The delay cell used for this VCO is shown in Figure 8. As for the 40 Gbit/s case, it is a resistively loaded common source amplifier. Furthermore, the tuning mechanism is very comparable, providing coarse tuning by means of a tunable resistive load.

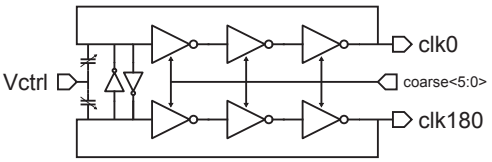

Figure 6. 10 Gbit/s VCO Architecture

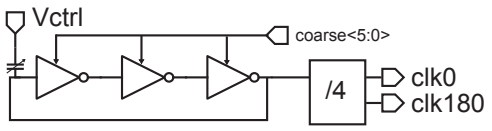

Figure 7. 2.5 Gbit/s VCO Architecture

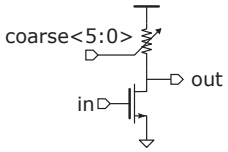

Figure 8. 10 Gbit/s VCO Delay Cell

However, fine tuning is not implemented on the delay cell level, but on the level of the core VCO. This is possible because only one of the three generated phases is used, which means the delay of the used cells can vary as long as the total delay of the ring is according to the desired oscillation frequency. Implementing the fine tuning on the core VCO level offers the advantage that the used varactor can be bigger, which leads to better manufacturability and less variations on the varactor. Moreover, this simplifies the layout of the VCO, since the control voltage must only be routed to one varactor instead of three.

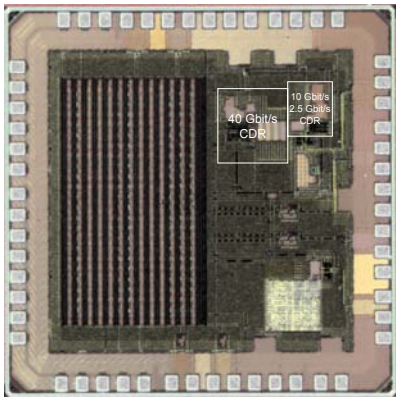

Figure 9. Photograph of the CABINET ASIC

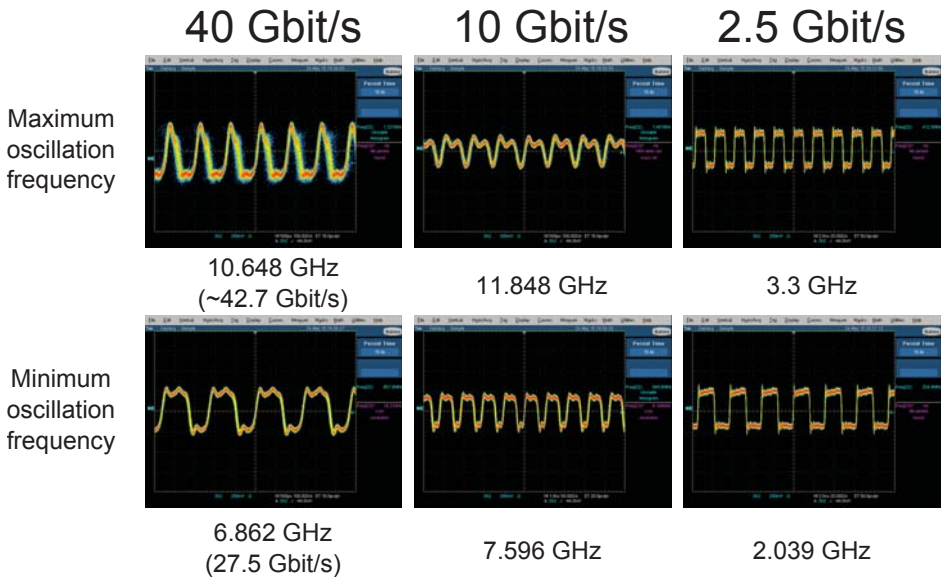

Figure 10. VCO Measurement Waveforms

V. CABINET Implementation

In Figure 9 a photograph is shown of the CABINET ASIC with the CDRs highlighted. The ASIC dimensions are about 1.85mm $\times$ 1.85mm.

VI. Measurement Results

The CABINET chip provides a test output where a divided version of the on-chip VCO clock is available for measurement. This test output allows us to verify the frequency range of the designed VCOs. The different waveforms are presented in Figure 10. Table I summarizes the VCO measurements.

Table I
VCOs Measured Frequency Range

	40 Gbit/s	**10 Gbit/s**	**2.5 Gbit/s**
Maximum	10.648 GHz	11.848 GHz	3.3 GHz
Minimum	6.862 GHz	7.596 GHz	2.039 GHz

A. CBI-PON Power Consumption

The low power consumption achieved for the CBI-PON is partly attributed to the fact that different CDRs and VCOs have been used for the multiple input line rates. The subsampling nature of the CDR allows the circuits to operate at lower frequencies, saving significant power. Furthermore, one could use the 40 GHz VCO for the 10 Gbit/s and 2.5 Gbit/s case. This would require using power-hungry clock dividers. By using a dedicated VCO, power consumption is reduced instead of increased for the lower speeds.
Compared to the GreenTouch 2010 defined reference network architecture, the power reduction is estimated at 80$\times$ for a CBI Repeater, while for an ONU it is estimated at 6$\times$ [6].

VII. Conclusion

In this paper, the Cascaded Bit-Interleaving PON was shortly introduced, clarifying the need for two different VCOs to implement the clock-and-data recovery circuits on the CABINET chip. Subsequently, the architecture of the two designed VCOs was presented, as well as the implementation of their respective delay cells. Finally, the frequency tuning range measurements were presented for 40 Gbit/s, 10 Gbit/s and 2.5 Gbit/s operation of the CABINET ASIC.

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