Design Trade-offs for Cost-effective Multimode Fiber Channel Equalizers in Optical Data Center Applications

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Abstract: A 10-Gb/s transmission over 1-km standard multimode fiber for data center applications is case-studied in terms of the design considerations for low-complexity and cost-effective equalizers which can increase the reach of multimode fiber links.
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1. Introduction

In recent years we have seen burgeoning global Internet traffic with tens of billions of connections per day to videos of YouTube, songs of iTunes and active users of Facebook. Energy-efficient data centers (DC) are in the core of these applications which require high-speed and great-scalability interconnection. Conventional electronic interconnections in data centers will suffer from huge energy consumption and cabling complexity due to the unabated growth computing density of modern data centers. Optical fiber links have become an integral part of overall system design providing optimized performance and higher reliability. [1]. Advances in optical technology make fiber links a more practical and affordable candidate for applications of ultra-high throughput and short reach interconnection. Multimode fiber (MMF) is competitive for these short haul multi-gigabit links owing to its high bandwidth compared to copper cable and low cost compared to single-mode fiber (SMF). The viability of MMF interconnects for 100-Gb/s and beyond in data centers have been well documented [2, 3]. However, few documents have contributed to dispersion compensation optimizations in such applications which can be employed to dramatically mitigate the inter-symbol interference (ISI) as data rate and distance increase .

In this paper, we investigated the trade-offs and feasible diversity for practical implementation of linear equalizers (LE) to extend the reach of multimode fiber links. The first generation of 100-Gb/s multimode fiber links were based on a parallel lane architecture with 10 lanes at 10-Gb/s [4] thus a 10-Gb/s line rate was chosen as a case study for this work. The method can be extended for next generation 4×25-Gb/s MMF links and beyond. A feedforward equalizer (FFE) is generally a cost-effective alternative for MMF links compared to decision feedback equalizers (DFE) because of the linearity of most mode dispersion.

2. System link model

Fig. 1 shows the considered MMF communication system model in Matlab. A 10-Gb/s nonreturn-to-zero (NRZ) pseudorandom binary sequence (PRBS) of length 2^9-1 is used as transmitted signal. As the small-signal modulation response of a typical 10-Gb/s channel vertical cavity surface emitting laser (VCSEL) shows no giant relaxation resonance peak at high bias current [5] which guarantees high bandwidth, the VCSEL is substituted by a second order low pass filter with a bandwidth of 0.75 times the bit rate. The shaped NRZ signal propagates through the linear dispersive optical fiber characterised by the following Gaussian impulse response and corresponding frequency response as in [6]:

$$h(t) = \frac{1}{\sqrt{2\pi}\alpha T} e^{-[t^2/(2(\alpha T)^2)]} \quad (1)$$

$$H(f) = e^{-[(2\pi\alpha T f)^2/2]} \quad (2)$$

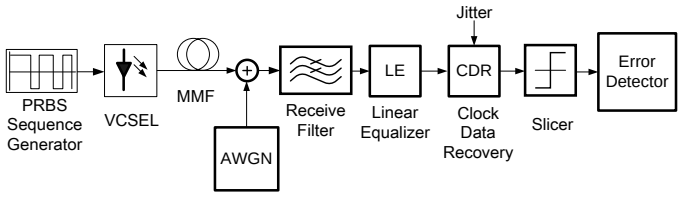

Fig. 1 MMF fiber link simulation block diagram

The described MMF fiber channel has a 3dB bandwidth of $f_{3\,dB} = \frac{0.1329}{\alpha T}$. For given baud time T (=100ps), we can consider various channel bandwidths by changing α and then, indirectly control the fiber reach as the modal

bandwidth remains constant for a certain wavelength. For instance, OM3 fibers operating at 850 nm wavelength has a modal bandwidth distance product of 2000 Mhz • km according to the 10GBASE-SR standard. Linear equalization is performed on the incoming signal corrupted by additive white Gaussian noise (AWGN) from the channel and timing jitter from the clock recovery circuit, in the back end, an error detector calculates the bit error rate (BER) .

3. Equalizer architecture and circuit implementation

The linear equalizer (LE) architecture shown in Fig. 2 is the simplest and most common type of electronic equalizer. Appropriately delayed and scaled versions of the received waveform are combined by the feedforward equalizer (FFE) to produce the corresponding output y(t) :

$$y(t) = \sum_{i=1}^{n} u_i \cdot x(t - [i \cdot \Delta t]) \quad (3)$$

where u_i are equalizer coefficients optimized by the least mean square (LMS) algorithm, n is the number of equalizer taps, x(t) is the input at time t, and Δt is the time delay between two adjacent taps . Typically, the time delay is a fraction of the bit period, such equalizer is known as the fractional spaced equalizer (FSE). The ratio K = Δt / T is referred as oversampling rate and K = 1 as the FFE or the baud spaced equalizer. The sampler output y_k is processed by the slicer to approximate an estimate of the transmit data after y(t) is sampled at the data rate. Timing jitter of the clock and data recovery (CDR) impacts the optimal sampling instance represented by τ_0, which could influence the performance of the whole system model. A continuous-time analog implementation of the linear equalizers is the preferred approach for MMF links as this avoids the challenging high speed ADC. Optimization of the physical length and tap coefficients in this tapped delay line LE topology is crucial to optimize the performance and to reduce the circuit complexity.

The transversal filter implementation of adaptive equalizers, sometimes referred to as a tapped-delay-line structure is of particular interest [7]. We can realize different configurations of linear equalizers at the receiver side with the tapped-line-structure in 45nm CMOS technology for MMF links shown in Fig. 3. Although the active delay line design is challenging to meet the bandwidth requirements at low-power consumption for a 10-Gb/s data stream, it relaxes the chip area and design freedom of impedance match. The variable gain amplifier (VGA) based on a modified Gilbert cell was employed in [8]. Here we aim not to discuss the circuit details but to give a rough estimation of the power consumption in the various equalizer configurations. A relatively large size is chosen for the input transistor of the VGA such that it dominates the output capacitance of the delay cell and determines the time delay. The benefit of this is that we can obtain an equalizer with different lengths by simply replicating and fine-tuning the circuit in the dotted rectangle in consideration of the similar surroundings. In order to meet the required delay of 25-, 33-, and 50-ps, corresponding to the T/4-FSE, T/3-FSE and T/2-FSE respectively, at most five unit delay cells are cascaded increasing the power needed.

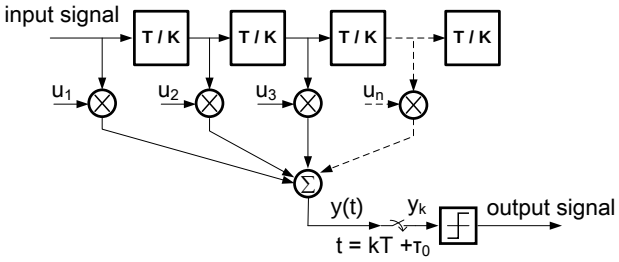

Fig. 2 Architecture of linear equalizer (LE)

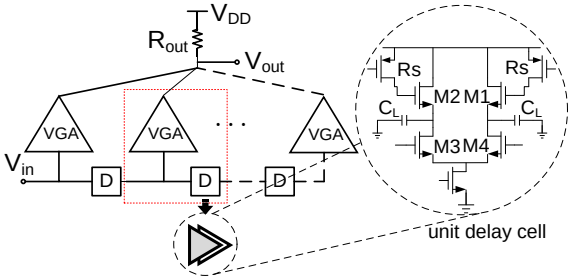

Fig. 3 Schematic of the linear equalizer

4. Simulation and discussion

Simulations of the foregoing fiber link model have been carried out to determine the optimal length of the equalizer for DC interconnection applications. To compare the performance of various equalizer configurations, we focused on BER simulations which measured the parameters that have physical meanings to the communication system design. Due to the time-consuming of Monte Carlo simulation, we lower the typical 10^{-12} BER performance requirement for such links. Odd taps are chosen for simulation because of the symmetrical nature of dispersion. Eye diagrams for 700m MMF link under different equalization schemes are shown in Fig. 4. Fig. 5a shows that a 3-tap FFE is the most attractive selection for the symbol-spaced FFE to minimize the ISI in terms of power efficiency and circuit complexity for a 500m-1km MMF channel while no significant improvement can be achieved by increasing the number of taps. Fig. 5b shows the required Signal-to-Noise Ratio (SNR) for BER of 10^{-9} over 1 km MMF channel against different FSEs. In most simulations, a FSE of varying oversampling rate has superior performance

over its symbol-spaced counterpart at the cost of more taps. There is an optimal length for the FFE to minimize the total dispersion implying that a longer length does not necessarily outperform a shorter one [9], which also applies to

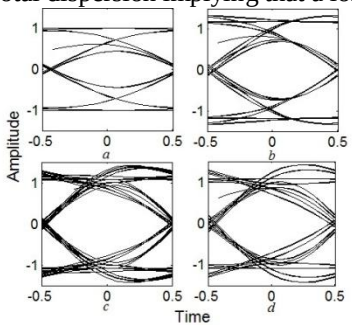

Fig. 4 Eye diagrams for 700m equalized MMF link
a: without equalization b: 3-tap FFE
c: 5-tap T/2-FSE d: 5-tap T/3-FSE

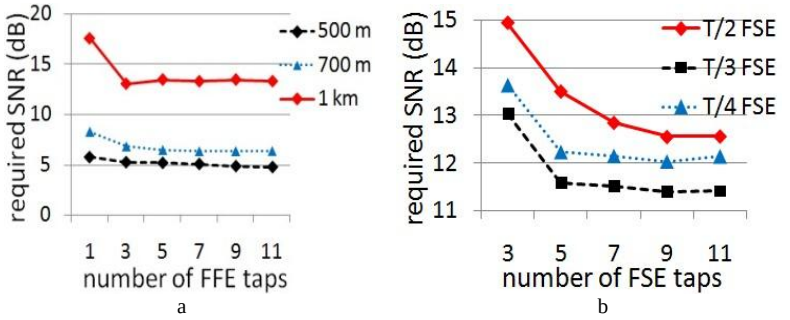

Fig. 5 Simulated SNR sensitivity (10-9 BER) for various FFE and FSE configurations
a: required SNR vs. FFE number of taps after 0.5-1 km MMF channel
b: required SNR vs. FSE number of taps for various K after 1 km MMF channel

a FSE as demonstrated analytically and numerically in [6]. Another advantage of a FSE is its insensitivity to timing phase errors in contrast to a FFE which will dramatically improve the performance on severely phase-distorted channels. Fig. 6 shows the simulated BER bathtub curves for a 1 km MMF channel with 12 dB input SNR. It is obvious that a 5-tap T/3 FSE outperforms a 3-tap FFE achieving a 0.38 unit interval (UI) timing margin at a BER of around 1E-6. The accuracy of the time delay can cause the degradation of BER performance which is depicted in Fig. 7. A ±4 ps time delay distortion deteriorate the BER performance of T/3(≈33ps) FSE up to 1.5dB at an input SNR of 5.5 dB. The approximate power consumption values from circuit level simulations are present in Fig. 8. A 5-tap T/3 spaced equalizer seems to be a good compromise considering performance and complexity at a cost of a 6% higher power consumption compared to a 5-tap T/4 FSE.

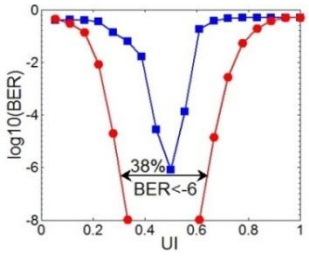

Fig. 6 Simulated BER bathtub curve for 1 km MMF

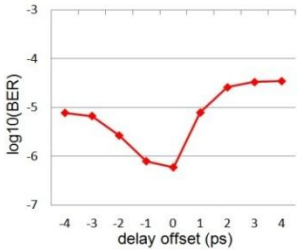

Fig. 7 Simulated BER vs. delay offsets

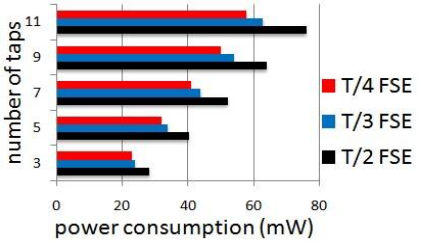

Fig. 8 Power consumption of various LEs

5. Conclusion

This work investigated the design methods for energy-efficient linear equalizers for high bandwidth optical interconnects in data centers through system and circuit level simulations. In the given communication system settings, five-tap T/3 spaced equalizer can be optimal considering the trade-offs among overall performance, power consumption and implementation complexity.

6. References

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