Embedded passive components for improved power plane decoupling

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***Abstract*— In this paper, a detailed power integrity study is described that compares the behavior of surface-mount devices and embedded components for power decoupling. Through measurements and simulations, it is found that when the layer count of the board is low, there is no significant difference between both technologies. When the number of layers increases, the short connection for the embedded components is clearly superior to the surface-mount capacitor. The resonance frequencies for the embedded capacitor do not change significantly with the increased layer count. The case with the surface-mount capacitor however, shows a large increase in parasitic inductance due to the long vias through the board.**

Keywords—power integrity, embedded passives, decoupling

I. INTRODUCTION

Power distribution in complex printed circuit boards is implemented using power planes in combination with decoupling capacitors to reduce the power distribution impedance. The performance of the decoupling capacitors is degraded by the parasitic inductance (and resistance) in series with the capacitance [1]. This inductance is a result of the effective series inductance (ESL) of the component itself in combination with the line inductance of the connection between the capacitor and the power planes. Embedding the decoupling capacitor in between the power planes minimizes the inductance of the interconnection and thus increases the bandwidth of the power delivery network.

The goal of this study is to compare the power decoupling network impedance (Z_{PDN}) of a power plane decoupled with embedded capacitors to Z_{PDN} of a power plane decoupled with surface-mount (SMD) capacitors (Fig. 1). A dedicated test vehicle is designed for this purpose and is described in section II of this paper. Section III discusses the measurement results, which form the basis of further modeling and simulations in section IV.

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II. COMPONENT EMBEDDING TECHNOLOGY

The Embedded Component Packaging technology from AT&S directly integrates the components in the core layers of the PCB [2]. The technology can be used for the embedding of both active and passive components. In this study, only the latter option will be applied. The main characteristics of the technology are the use of openings in the prepreg layers matching the location of the components and the microvia interconnections to the contact pads of the embedded component. The plated Cu microvia interconnection eliminates the need for solder or conductive adhesives, thus avoiding the associated failure modes. The thickness of the components (150 µm) and their pad metallization (copper) need to be compatible with the lamination and metallization process steps, respectively. A broad range of embeddable passive components are currently available and manufacturers are continuously improving their product range with respect to available values, tolerances, and temperature and power ratings.

In principle, a standard PCB process flow starts with a double sided core, which is structured in the subsequent process steps and built up to a multilayer construction. In the case of embedding components, a so called “embedded core” is produced in the first phase of the process flow. The main process steps for embedding of components are printing of adhesive, assembly of components, pressing and drilling of vias and plated through holes.

The HF-RTV-PI test vehicle is used to compare the power

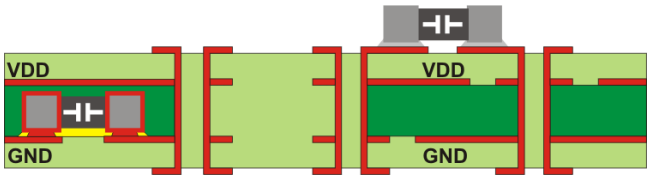
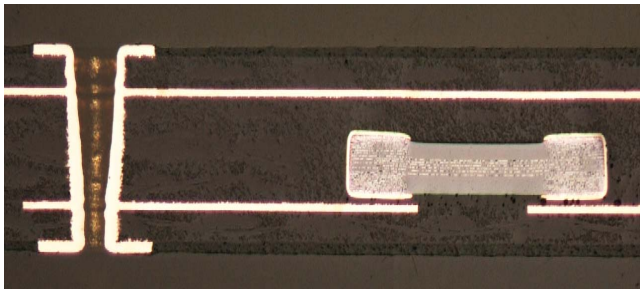
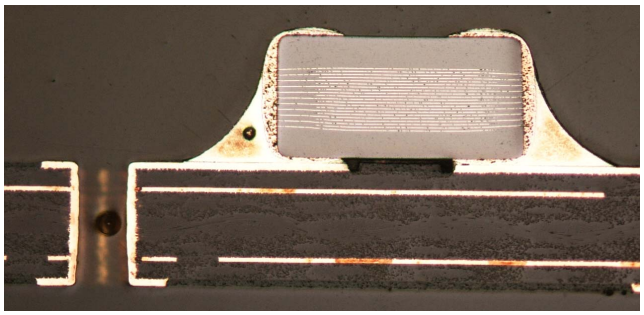


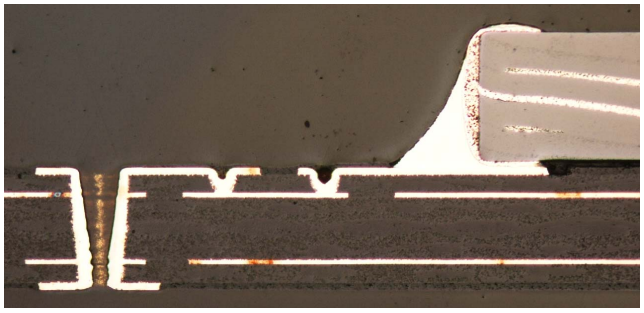
Fig. 1. Comparison of a surface-mounted decoupling capacitor (right) to a decoupling capacitor integrated using the Embedded Component Packaging technology from AT&S (left)



(a) Embedded decoupling capacitor



(b) Surface-mount decoupling capacitor



(c) Surface-mount decoupling capacitor with additional microvia interconnections

Fig. 2. Different configurations for power plane decoupling on the HF-RTV-PI test vehicle

decoupling network impedance for planes decoupled with embedded passive components to planes using surface-mount decoupling devices on top. Four different types of power plane decoupling configurations are implemented: a reference plane without decoupling components, a power plane using embedded decoupling capacitors, one using surface-mount decoupling capacitors, and finally a power plane with added microvia chains to simulate additional build-up layers. Fig. 2 shows cross sections of these configurations. As can be seen from the pictures, a four layer board is used, where the two internal layers are used as power planes. The size of the power planes is 10 cm by 10 cm and the distance between the planes is 220 µm for all configurations.

By dividing the tolerated voltage ripple by the maximum transient current, the target impedance for the power decoupling network can be calculated. The actual impedance of the power delivery network, Z_{PDN}, has to be smaller than this target impedance over the complete frequency content of the transient currents. The selection of the components was performed using a dedicated PI simulation program, with a target impedance of 0.04 Ω. The most significant restriction was the availability and thickness of embeddable decoupling capacitors. Capacitances larger than 100 nF are currently only available in a thickness of 450 µm, which is too thick for the embedding process. The final selection included thirty 10 nF capacitors and five 100 nF capacitors. The size of all components is 0402 (1 mm x 0.5 mm) with a thickness of 150 µm for the embeddable components. Due to the lack of components with higher capacitance, Z_{PDN} shows a peak of 0.2 Ω around 2.6 MHz.

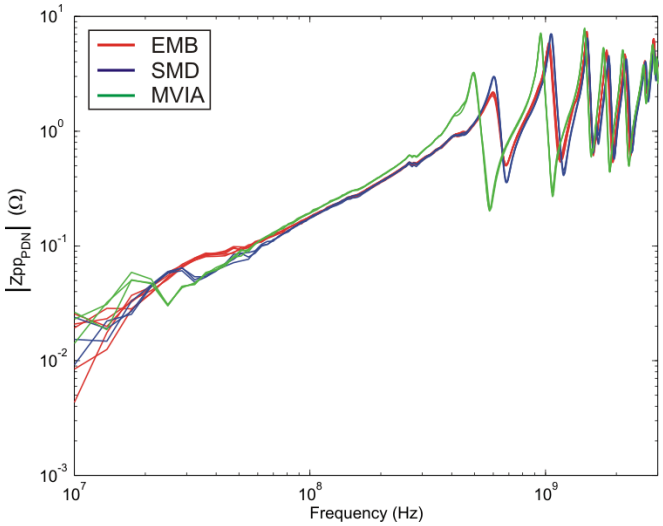
In order not to increase the complexity of the board, the number of layers is limited to four: 2 core layers with the power planes and a build-up layer on each side. However, boards where power integrity is a concern, often contain many core layers and 2 or 3 microvia build-up layers. To mimic this type of stack-up, a microvia daisy chain was added resulting in a comparable increase in interconnection length between the planes and the surface-mount component.

The extraction of the input impedance from the S-parameters requires a 2-port simulation or measurement. The reason for this is that due to the low values of the power plane impedance, the reflection coefficient S_{11} is close to 1 and the dynamic range of the VNA is limited at these values. The solution is to use a 2-port measurement and extract the power plane impedance from S_{21}. In theory, the two probes could be placed on the same contact pad, using only a single pair of vias to the power planes. In this configuration, however, the via loop inductance is placed in series to Z_{PDN}, and will have an influence on the extracted value of the impedance. To prevent this, a dedicated probe pad, with additional via pair, was added to the design.

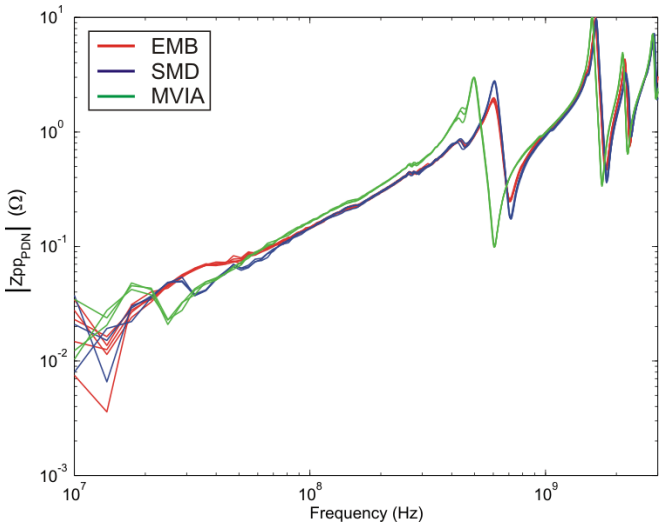
For manufacturability, the embeddable components need to be grouped in groups of 8 or 9. This is acceptable for global decoupling purposes, but for local decoupling close to the chip, or for terminating resistors, the placement of single components inside a cavity is required. Apart from the groups of 8 or 9 components, also single components and groups of 2 components are incorporated in the design. These groups are placed pseudo-randomly across the power plane. The probe contacts are added on three different locations, to demonstrate the distributed behavior of the planes.

III. MEASUREMENTS

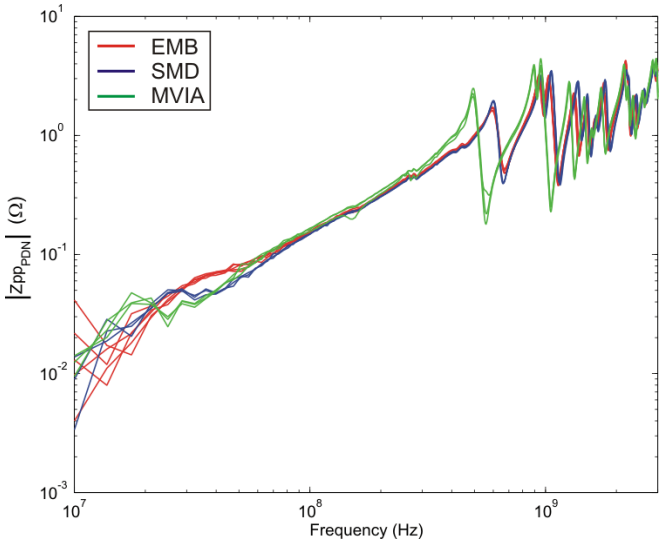
The goal of this power integrity study is to verify if embedding the decoupling capacitors in between the power planes can improve the decoupling behavior. The HF-RTV-PI test vehicle was designed for this purpose, allowing the direct comparison between embedded and surface-mount capacitors. The measurements were performed using an Agilent PNA 8364B vector network analyzer in a frequency range from 10 MHz up to 3 GHz. The test structures are contacted using coplanar microwave probes (Picoprobe 50A-GS/SG-500-P) and a dedicated PCB probe table. Fig. 3 shows the measurement results for the three different configurations: embedded decoupling capacitors (EMB), surface-mount decoupling capacitors (SMD) and surface-mount decoupling capacitors with additional microvia connections (MVIA).



(a) Middle of top edge (50.0 ; 90.0)



(b) Centre of board (50.0 ; 50.0)



(c) Lower right corner (70.0 ; 18.0)

Fig. 3. Magnitude of Z_{PDN} for the different probe contact locations on the HF-RTV-PI test vehicle. Coordinates indicate the position of the measurement port in mm, with the origin in the lower left corner and the dimensions of the board equal to 100 mm x 100 mm.

The difference in power decoupling network impedance between the embedded and surface-mount components is very small for the four-layer test board. The board resonances only affect Z_{PDN} at frequency above 1 GHz and are, as expected, clearly dependent on the location of the probe pads. The additional microvia connections increase the parasitic inductance and thus result in an increase in power decoupling network impedance. The difference remains small and thus the added bandwidth negligible. The scattering of the results at low frequencies is due to the fact that measurements are taken at the low frequency limit of the VNA.

Boards of higher complexity, i.e. layer count, are believed to benefit more from embedding decoupling capacitors. This hypothesis will now be verified using modeling and finite-element method simulations.

IV. Simulation and Modeling

Modeling the frequency-dependent behavior of a power/ground plane pair with added decoupling capacitors requires the calculation of an N-port impedance matrix. Each connection from the power plane to a component; whether it is a decoupling capacitor, a voltage regulator module or an IC; can be regarded as a port. The distributed impedance between two ports on the board is calculated using a Green's function of the 2D-Helmholtz equation [3]:

$$Z_{ij}(\omega) = j\omega\mu \frac{h}{w^2} \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\varepsilon_n^2 \varepsilon_m^2}{k_{mn}^2 - k^2} f(x_i, y_i) f(x_j, y_j) \quad (1)$$

$$f(x_i, y_i) = \cos\left(\frac{m\pi x_i}{w}\right) \sin c\left(\frac{m\pi t_{x_i}}{2w}\right) \cos\left(\frac{n\pi y_i}{w}\right) \sin c\left(\frac{n\pi t_{y_i}}{2w}\right) \quad (2)$$

w	Width of the power plane
h	Spacing between the planes
ε_n,ε_m	1 for m,n = 0, and $\sqrt{2}$ otherwise
k	Propagation constant
k_{mn}	Wave number
x_i,y_i	Coordinate of port i
t_{xi},t_{yi}	Dimensions of port i

This analytical expression provides the impedance matrix for each pair of ports with Z_{ii} being the self-impedance at each port and Z_{ij} the transfer-impedance between ports. Consider a component drawing current at one port and a decoupling capacitor at the second port. With Z_L being the equivalent impedance of the parasitic inductance and the capacitance of the decoupling capacitor, the input impedance seen by the component becomes

$$Z_{in} = Z_{PDN} = Z_{11} - \frac{Z_{12} Z_{21}}{Z_L + Z_{22}}. \quad (3)$$

This analytical model is used to verify simulations of power planes with different decoupling configurations. The simulations are performed in Comsol Multiphysics and thus based on the finite-element method. To limit the simulation time, the comparison between the model and the simulation was performed for a 5 cm by 5 cm power plane pair, with the

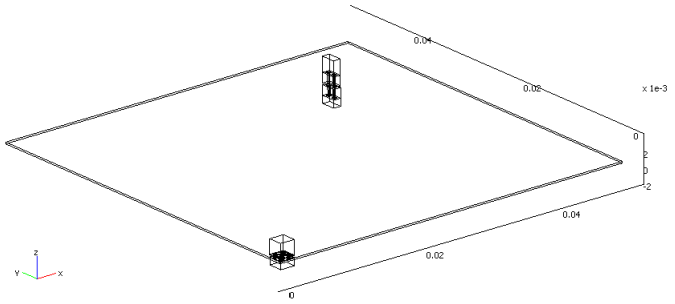


Fig. 4. 3D model of a 5 cm by 5 cm power plane pair with a 220 µm thick dielectric (ε_r = 3.9). The excitation and measurement port are near the origin (2e-3;2e-3;2.2e-4), while the decoupling capacitor is located at (0.04;0.04;2.2e-4)

probe structure close to the corner of the plane. The layout of the FEM model is shown in Fig. 4.

The first simulation was run to calculate the impedance of the bare board (Z_{11}). As can be seen from the formula above, the self-impedance Z_{11} is dependent on the dimensions of the power plane pair (5 cm x 5 cm x 220 µm), the location of the port (2e-3;2e-3;2.2e-4) and the size of the port (500 µm x 500 µm). The second step was to add the port structure for the SMD capacitor. The layout was again similar to HF-RTV-PI, with two PTHs going to the top of the four layer board. And finally, the simulation was also performed with an embedded decoupling capacitor, eliminating the need for the second PTH. In both cases, the decoupling capacitor was an ideal 1 nF capacitance, so the parasitic inductance was only related to the interconnect method. Fig. 5 shows the results of these simulations, with very good correspondence between the simulations and the model.

The difference between the parasitic inductance for the embedded capacitor and the SMD version is very small (0.24 nH vs 0.27 nH, respectively). This is due to the low layer count of the board. To get a more realistic comparison, the number of layers of the surrounding board was increased. The new simulated build-up consists of a core with 12 layers of 200 µm (except the power plane pair separation which was kept at 220 µm) with three build-up layers of 100 µm on each side, resulting in an 18-layer board, 2.82 mm thick. The power plane pair was situated in the middle of the core (layer 9 and 10).

Fig. 6 compares the results for the 4-layer board to the 18-layer board, both with a 1 nF decoupling capacitor. The resonance for the embedded capacitor does not change significantly with the increased layer count. The case with the surface mount capacitor, however, shows a large increase in parasitic inductance due to the long vias through the board. Here the advantage of embedding the component in between the power planes is very clear.

V. Conclusion

This study compares the decoupling performance of surface-mount components to embedded components. Measurements of a dedicated test vehicle did not reveal a significant difference in power decoupling network impedance due to the low layer count of the test board. Simulations of

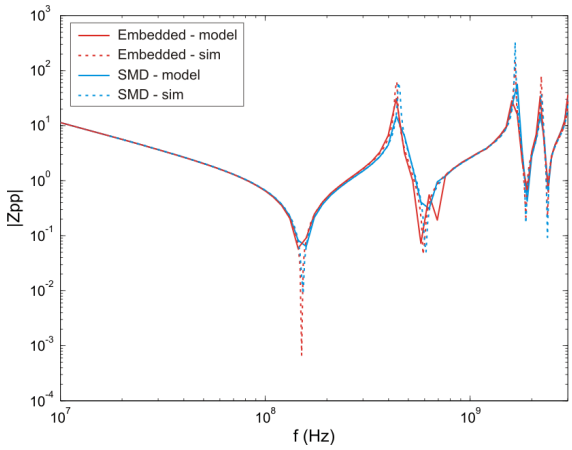


Fig. 5. Simulation results for a 5 cm by 5 cm power plane pair with a 220 µm thick dielectric (ε_r = 3.9). The excitation and measurement port are near the origin (2e-3;2e-3;2.2e-4), while the decoupling capacitor is located at (0.04;0.04;2.2e-4).

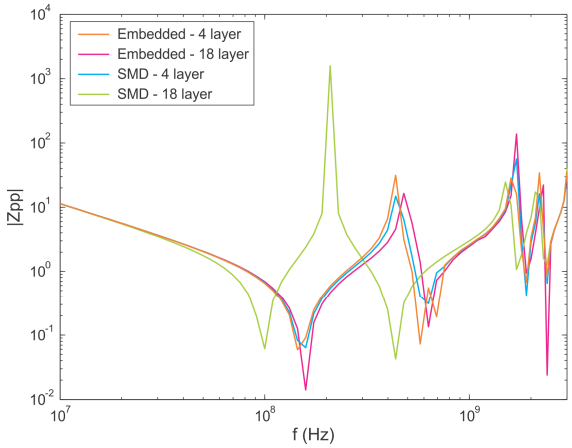


Fig. 6. Simulated power decoupling network impedance for embedded and surface-mount decoupling capacitors for a 4- and 18-layer board

similar configurations confirmed this result and were also applied to corroborate the hypothesis that boards with a higher layer count benefit more from embedding decoupling capacitors.

Embedding decoupling capacitors in between the power planes is certainly valuable for the power integrity, although the benefit strongly depends on the complexity of the board. Combined with the overall reduction in length of the signal path offered by embedding active and passive components, a noticeable increase in performance can be obtained.

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