

# A Photonic Interconnect Layer on CMOS

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**Abstract** We propose and demonstrate a photonic interconnect layer consisting of heterogeneous microdisk lasers and microdetectors integrated with a nanophotonic silicon waveguide circuit. The photonic layer is fabricated using waferscale processes and a die-to-wafer molecular bonding process.

## Introduction

Many applications need an intimate integration of electronics circuits and photonic devices. Several groups have demonstrated flip-chip bonding of VCSEL or detector arrays on CMOS-circuits. However, such a process does not allow for a high integration density, is not compatible with waferscale processes and does not allow for additional functionality such as multiplexing, filtering or optical sensing circuits. People also have proposed to include optical circuits into the silicon transistor layer. However this consumes a lot of expensive space within this layer, and therefore is not compatible with applications requiring a dense optical interconnect network. Therefore, in the EU-funded project PICMOS, we proposed to build a photonic layer that can be integrated on top of the electronic circuits, as an additional interconnect layer, conceptually equal to the standard Cu-based interconnect layers. This paper focuses on the fabrication of this photonic layer. Once completed, it can be integrated with the CMOS-wafer through a wafer-to-wafer bonding process. The targeted application was on-chip optical interconnect, requiring ultra-low power devices with very small footprint.

## Fabrication of the photonic layer

Silicon wire waveguides with dimensions of 500nm x 220nm were chosen as the basic waveguiding platform for the photonic interconnect layer. This waveguide platform allows for very compact structures, such as 3 $\mu$ m bends with negligible loss and a center-to-center pitch of <1.5 $\mu$ m (for an interchannel crosstalk below 20dB/cm). Especially this last parameter is important for dense interconnect structures, since one can show that, if the size of the transmitter and receiver is kept below 10x10 $\mu$ m<sup>2</sup>, this parameter ultimately determines the global achievable data density per square cm. The silicon wire waveguides were fabricated in the IMEC CMOS pilot line using 248nm DUV lithography and an ICP-based etching process [1], on a 200mm SOI wafer with a 220nm silicon top layer and a 1 $\mu$ m buried oxide layer (Fig. 1a). In a next step 1 $\mu$ m deep ebeam markers were defined and subsequently a 1 $\mu$ m thick P-FOS SiO<sub>2</sub> top cladding layer was deposited. Then this SiO<sub>2</sub> layer was planarized and thinned

down to 200nm by project partner Tracit using a chemical mechanical polishing process (CMP)(Fig. 1b). The thickness of the remaining SiO<sub>2</sub> layer has to be controlled within +/-10% since it will determine the coupling strength between the III-V optoelectronic devices and the silicon wire waveguides. The short range roughness following the CMP process has to be reduced below 1nm to make the molecular bonding process possible.

Following the planarization process, the waveguide wafers are ready for integration with the III-V material. Separate InP-based epitaxial structures were grown for the sources and the detectors. The layers for the sources were growing by INL using an MBE process and contain a tunnel junction to reduce the losses in the device (see [3] for more details). The top surface of the MBE-grown layers has a very low roughness (<1nm) and, in combination with a 10nm ECR deposited SiO<sub>2</sub> layer, allows for direct molecular bonding without further planarization process. The epitaxial layers for the detector were grown using an MOCVD process by TU/e. MOCVD grown layers typically have a larger roughness (>2nm), which required deposition of a thicker SiO<sub>2</sub> layer that was subsequently planarized using a CMP process.

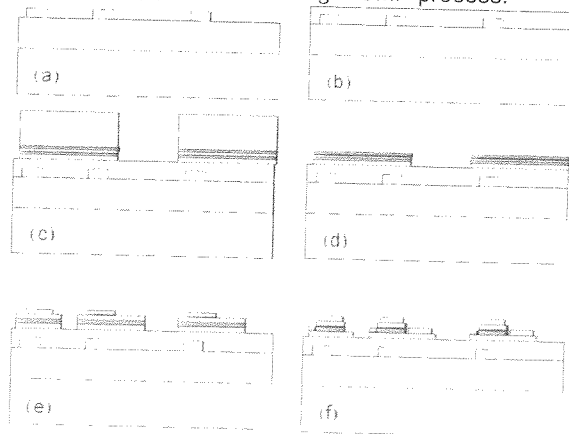
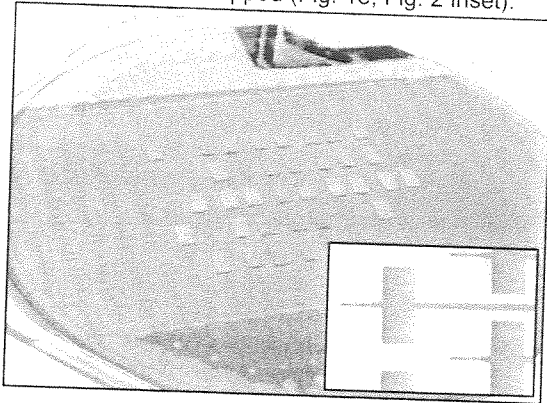


Fig. 1 Photonic layer integration process

Following a cleaning and chemical activation process, 9 x 5 mm<sup>2</sup> large dies of the source and detector epitaxial wafer were bonded on top of the silicon waveguide wafer using a molecular bonding process (Fig. 1c, Fig. 2) by the CEA-LETI team [2]. The temperature during this process was kept below 220°C. The size of the III-V dies is determined by the

application and can vary from  $1\text{mm}^2$  to several  $\text{cm}^2$ . Since the dies are unstructured before bonding, precise alignment is not required, allowing for a fast pick-and-place process.

In the next step, the InP substrate of the dies and an InGaAs stop layer were removed using a wet chemical etch process leaving a III-V epitaxial layer stack varying from  $500\text{nm}$  to  $1\mu\text{m}$  (Fig. 1d). Following a back-side decontamination process, the wafers were reintroduced in the CEA-LETI 200mm CMOS pilot line and a  $150\text{nm}$   $\text{SiO}_2$  mask layer was deposited using a  $220^\circ\text{C}$ . The mesa-structures for the photodetectors and the sources were defined into this mask layer using ebeam-lithography. The deep markers defined in the first step of the process were used as alignment reference. The hard mask was then etched and the resist was stripped (Fig. 1e, Fig. 2 inset).



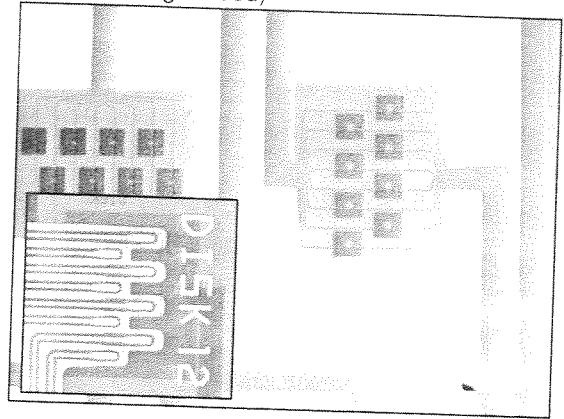
**Fig. 2** 200mm SOI wafer with bonded III-V dies on top. Inset: pattern for detector defined in  $\text{SiO}_2$  hardmask using ebeam litho and hard mask etching in CEA-LETI CMOS pilot line

Following this step, the 200mm wafers were diced for further processing because at the moment no tools were available for InP-etching on 200mm wafers. The source and detector mesa's were etched by partners INL and TU/e respectively and finally the structures were planarized and contacts were defined by IMEC (Fig. 1f).

### Results

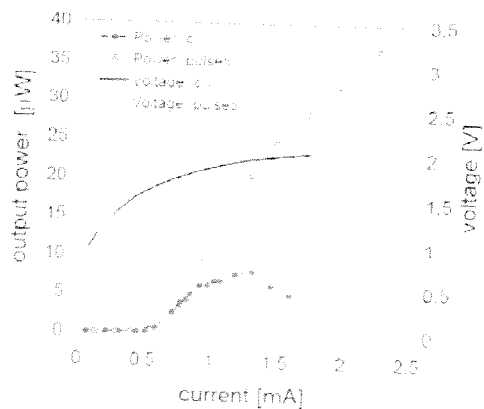
Fig. 3 shows a picture of an array of 8 microdisk lasers before and after (inset) metallisation. Each microdisk laser is individually coupled to underlying silicon wire waveguides, which are subsequently brought together and as a parallel bus wired to a similar array of 8 photodetectors. The  $7 \times 9 \text{mm}^2$  size cells contained in total 144 microdisk lasers and 264 micro detectors, connected through silicon wire waveguides. The second output of the microdisk lasers was connected to a diffraction grating, for easy characterisation of the sources. Fig. 4 shows the operating characteristics for a microdisk laser with  $7.5\mu\text{m}$  diameter. The threshold current is approximately  $550\mu\text{A}$ . Due to the high thermal resistance, the total output power under continuous wave operation was limited. We believe this can be

overcome in future generation devices through the definition of a thermal via through the bonding layer. Under pulsed operation, output powers above  $100\mu\text{W}$  were measured (power coupled into silicon wire waveguide, single sided)



**Fig. 3** Arrays of 8 heterogeneously integrated InP microdisk lasers coupled to SOI-waveguide circuits before and after (inset) deposition of the metal contacts.

For the individual detectors we measured a responsivity of  $0.3\text{A/W}$ , including the coupling from the silicon wire waveguide. The dark current measured at a  $4\text{V}$  reverse bias voltage was  $1.6\text{nA}$ . Preliminary measurements also showed operation of a complete link, with light generated from the microdisk sources detected by the microdetectors.



**Fig. 4** Operating characteristics of  $7.5\mu\text{m}$  diameter microdisk laser

### Conclusion

We proposed and fabricated a photonic interconnect layer through waferscale processes and a fast die-to-wafer bonding process. Operation of electrically contacted microsources, microdetectors and a full optical link were demonstrated.

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- This work was supported by the EU through the IST project PICMOS*

- 6.2.3 Study of precise optical modulation using Mach-Zehnder interferometers for advanced modulation formats** ..... 73  
Tetsuya Kawanishi, Takahide Sakamoto, Akito Chiba, Masayuki Izutsu (National Institution of Information and Communications Technology, Japan)
- 6.2.4 Advanced Modulation Formats for Electronic Predistortion of Intra-channel Nonlinearities at 40 Gbit/s** ..... 75  
Stephan Hellerbrand, Norbert Hanik (Munich University of Technology, Germany); Christian Weber, Klaus Petermann (Technical University of Berlin, Germany)

### Session 6.3 – Novel Integration Technology I

Chair: Piero Gambini (Avago Technologies, Italy)

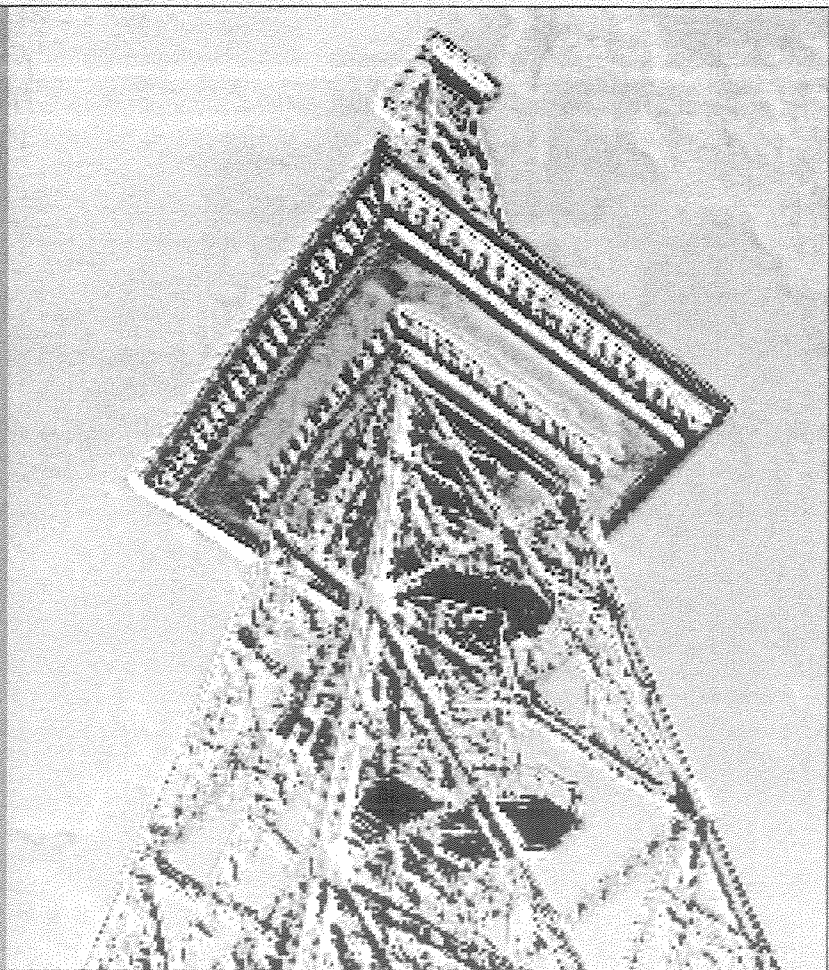
- 6.3.1 Invited: A Photonic Interconnect Layer on CMOS** ..... 77  
Dries Van Thourhout, Joris Van Campenhout, Roel Baets (Ghent University – IMEC, Belgium); Pedro Rojo-Romeo, Phillippe Regreny, Christian Seassal (Institut des Nanotechnologies de Lyon, France); Chrystelle Lagahe (Tracit Technologies, France); Xaveer Leijtens, Pietro Binetti, Richard Notzel, Meint Smit (TU/e, The Netherlands); Lea Di Cioccio, Jean-Marc Fedeli (CEA-DRT/LETI, France)
- 6.3.2 160 Gb/s optical time-division demultiplexing by four-wave mixing in a 5 cm length ultra-high nonlinear As<sub>2</sub>S<sub>3</sub> waveguide** ..... 79  
Mark Pelusi, Vahid Ta'eed, Steve Madden, D Choi, Barry Luther-Davies (Centre for Ultrahigh bandwidth Devices for Optical Systems – CUDOS, Australia); Benjamin Eggleton (University of Physics, Australia)
- 6.3.3 Wavelength Converter with +5 dB Parametric Gain Using Direct-Bonded QPM-Zn: LiNbO<sub>3</sub> Ridge Waveguide** ..... 81  
Takeshi Umeki, Masaki Asobe, Yoshiki Nishida, Osamu Tadanaga, Katsuaki Magari, Tsutomu Yanagawa, Hiroyuki Suzuki (NTT Photonics Laboratories, Japan)
- 6.3.4 First Demonstration of PPLN+RSOA-based Tunable All-Optical NRZ-to-RZ Format Conversion** ..... 83  
Jian Wang, Junqiang Sun, Qizhen Sun, Xinliang Zhang, Dexiu Huang (Huazhong University of Science and Technology, P.R. China); Martin Fejer (Stanford University, USA)
- 6.3.5 Fabrication of 300-nm-period nanostructure in a bulk fused silica** ..... 85  
Mykhaylo Dubov, Vladimir Mezentsev, Ian Bennion, David Nikogosyan (Aston University, United Kingdom)
- 6.3.6 Vertically Coupled GaInAsP/InP Microring Lasers Fabricated by Using Full Wafer Bonding** ..... 87  
Helmut Heidrich, Michael Hamacher, Ute Troppenz (Fraunhofer Institute for Telecommunications, Germany); Dimitris Syvridis, Dimitris Alexandropoulos, Spiros Mikroulis (National and Kapodistrian University of Athens, Greece); Kevin Williams, Chyng Wen Tee (University of Cambridge, United Kingdom); Viorel Dragoi (EV Group E. Thallner GmbH, Austria); Marin Alexe (Max Planck Institute of Microstructure Physics, Germany); Dana Cristea, Cristian Kusko, Mihai Kusko (National Institute for Research and Development in Microtechnologies, Romania)



September 16 – 20, 2007  
Berlin, Germany

# 33<sup>rd</sup> European Conference and Exhibition on Optical Communication

Volume 3  
Proceedings  
Wednesday,  
September 19,  
2007



**Bibliografische Information der Deutschen Nationalbibliothek**

Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliografie; detaillierte bibliografische Daten sind im Internet über <http://dnb.d-nb.de> abrufbar.

ISBN 978-3-8007-3042-1  
(5 Bände incl. CD-ROM)

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Druck & Bindung: druckmuck@digital e.K., Berlin

2007-09