ADDRESSING STATIC AND DYNAMIC ERRORS IN BANDPASS UNIT ELEMENT MULTIBIT DAC'S

J. De Maeyer, P. Rombouts and L. Weyten

Ghent University, Electronics and Information Systems.,St.-Pietersnieuwstr. 41,9000 Gent,Belgium

ABSTRACT

This paper describes a general model for static as well as dynamic errors in multibit unit element DAC's. Apart from the static mismatch there are two other error terms arising from switching imperfections. Based on the model, some bandpass mismatch shaping techniques are presented. These address both the static mismatch as well as the switching imperfections. The techniques can significantly improve the in band noise.

1. INTRODUCTION

In the past it was shown that discrete time implementations of multibit DAC's using unit elements become highly linear when static mismatch shaping is applied [1, 2]. However, with the increasing speed demands, continuous time $\Sigma\Delta$ DAC's (e.g. current steering DAC's) become more and more popular. Here, the imperfect switching characteristics, rather then the static mismatch of the elements are likely to limit the DAC performance [3, 4]. However, until now little has been done to address these dynamic errors. In this paper we start by explaining a model that incorporates both static as well as dynamic errors. The model will be used to introduce several DAC structures that bandpass shape both errors.

2. DYNAMIC ERROR MODEL

Fig. 1 show a multibit current steering DAC. It consists of N nominally matched current sources. At each point in time kT the input of this DAC is denoted as $D(k)$. Each element i is driven by a selection signal $S_i(k)$. It is the task of the element selection logic (ESL) to properly select these $S_i(k)$, under the the constraint that $\sum_{i=1}^{N} S_i(k) = D(k)$.

Let us now consider one element i. Its input sequence is $S_i(k) = \{0, 1, 0\}$. The output waveform of an ideal unit element is a rectangular pulls spreading from kT to $(k+1)T$. The height of this pulse is the unit element current I_n. Instead of using a continuous time model, we will perform our analysis using a discrete time model using charge like in [3,4]. The charge dumped by an ideal element i is $S_i(k)TI_n$ and the total charge dumped by the DAC equals $D(k)TI_n$.

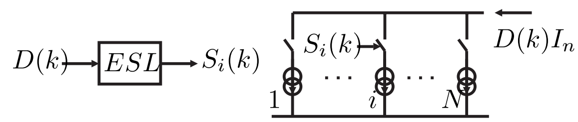

Fig. 1. Multibit DAC using N unit elements.

In practice however, the output waveform of element i will much more resemble the waveform of fig. 2. It clearly deviates from the ideal rectangular pulse. Therefore the amount of charge dumped by the DAC will be different. This difference is the DAC error, referred to as $e(k)$.

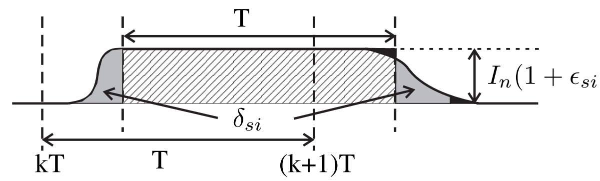

Fig. 2. Typical output waveform of a current source. The nominal rectangular pulse (hatched rectangular) is positioned such that the two gray shaded surfaces are the same (the black shaded surfaces compensate each other).

To derive an expression for this $e(k)$, we start by discussing the two aberrations of the output waveform from the ideal one. First, there is the static error: once an element is fully turned on it dumps a current $I_n(1 + \epsilon_{si})$, instead of I_n. We can define ϵ_{si} as the sum of two terms. The first, is the mean value of ϵ_{si} over the different elements, called ϵ. The second is ϵ_i, which contains the variation in ϵ_{si} from element to element. The DAC error as a result of these static errors is given by (1) [1, 2]. From this it is observed that the term $e_0(k)$ is proportional to the input $D(k)$, causing an acceptable gain error. The second term $e_1(k)$ is the well known static mismatch error term.

$$e_s(k) = \sum_{i=1}^{N} e_{si} S_i(k) = \underbrace{\epsilon D(k)}_{e_0(k)} + \underbrace{\sum_{i=1}^{N} e_i S_i(k)}_{e_1(k)} \quad (1)$$

J. De Maeyer is supported by a fellowship of the Fund for Scientific Research - Flanders (F.W.O.-V., Belgium.)

Secondly, there is the dynamic error: an element does not switch instantaneously (e.g. as a result of turn-on (off) delay, finite rise (fall) time, ...), see fig. 2. This causes an error charge denoted as δ_{si}. For each output waveform a nominal pulse with height I_n and length T can be positioned such that this δ_{si} is the same for switching the element on or off, see fig. 2. Similar to ϵ_{si}, δ_{si} consists of two terms. The first is δ, the mean value of δ_{si} over the different elements. The second term is δ_i and is called the dynamic mismatch. The dynamic errors only contribute to the DAC error if an element is switched, hence the dynamic DAC error is:

$$\begin{aligned} e_d(k) &= \sum_{i=1}^{N} \delta_{si} \mid S_i(k) - S_i(k-1) \mid \\ &= \underbrace{\delta \sum_{i=1}^{N} \mid S_i(k) - S_i(k-1) \mid}_{e_2(k)} \\ &\quad + \underbrace{\sum_{i=1}^{N} \delta_i \mid S_i(k) - S_i(k-1) \mid}_{e_3(k)} \end{aligned} \tag{2}$$

In contrast to the error term $e_0(k)$ caused by the mean value ϵ_{si}, the error term $e_2(k)$ caused by the mean value of δ_{si} does not depend in a linear way of the input. Therefore the total DAC error $e(k)$ is given by:

$$\begin{aligned} e(k) = \sum_{i=1}^{N} \epsilon_i S_i(k) &+ \delta \sum_{i=1}^{N} \mid S_i(k) - S_i(k-1) \mid \\ &+ \sum_{i=1}^{N} \delta_i \mid S_i(k) - S_i(k-1) \mid . \end{aligned} \tag{3}$$

In [3] a similar model was used, but $e_3(k)$ was not taken into account. In [4] the same model was presented.

3. TACKLING THE ERROR TERMS

The energy of the total DAC error needs to be as small as possible in the frequency band of interest. This can be achieved if the ESL properly selects the $S_i(k)$. Until now the presented ESL techniques only address the error $e_1(k)$ (static mismatch shaping) [1, 2]. One exception is the modified mismatch shaping technique of [3]. Here both $e_1(k)$ and $e_2(k)$ are low pass shaped.

In [4] we proposed a general way to tackle all $e_i(k)$. It is based upon the restriction that $S_i(k)S_i(k-1) = 0, \forall k$. Then it is possible to simplify $e_2(k)$ and $e_3(k)$ to (4). Hence, $e_2(k)$ now depends linearly on the input value D(k) and any set of selection signals $S_i(k)$ that shape the static mismatch will automatically shape the dynamic mismatch as well.

$$\begin{aligned} e_2(k) &= \delta \cdot (D(k) + D(k-1)) \\ e_3(k) &= \sum_{i=1}^{N} \delta_i S_i(k) + \sum_{i=1}^{N} \delta_i S_i(k-1). \end{aligned} \tag{4}$$

In physical terms the restriction means that an element needs to perform the full transition of fig. 2 every time it is selected. Both return-to-zero (RZ) and dual-return-to-zero (DRZ) achieve this by dividing the clock period into two phases. During one phase the element is turned on to be turned off during the other. This returning to zero increases however the jitter sensitivity and the slew rate requirements on the analog output stage. DRZ avoids these problems by using twice as many elements.

The operation on two phases of the clock in the case of RZ and DRZ actually requires a double-frequency system-clock. The use of such a clock can be avoided and **the restriction still be satified if no element is turned on during two or more consecutive clock periods**. Then, to be able to fulfill the input code $D(k)$, it is necessary to have twice as many unit elements as the maximum input code of the DAC. In [4] some low pass shaping techniques were presented based on these observations. However, to the authors' knowledge no (static and dynamic) mismatch bandpass shaping techniques were presented yet.

4. BANDPASS SHAPING

4.1. DAC performance limited by dynamic errors

Most of the existing mismatch shaping techniques only address $e_1(k)$. However, the dynamic errors $e_2(k)$ and $e_3(k)$ can severely degrade the performance if they are not addressed [3, 4]. To illustrate this a 3 bit DAC was simulated, using the a vector quantizer structure (VQ) [1]. An example is shown in fig. 3, the loopfilter $H(z)$ is chosen such that the mismatch transfer function MTF ($\frac{1}{1-H(z)}$), has one or more zeros in the frequency band of interest. For a bandpass shaping DAC [1] proposes $H(z) = \frac{-z^{-1}+z^{-2}}{1+z^{-2}}$.

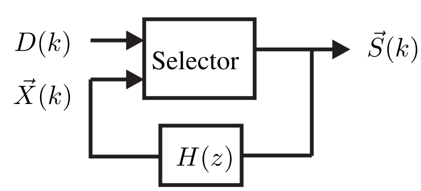

Fig. 3. A typical vector quantizer structure.

A simulation of the spectrum of the ideal DAC and a DAC with a static mismatch (ϵ_i) of 0.1 % is shown in fig. 4. It illustrates the effectiveness of the VQ in shaping the static mismatch energy out of the signal band. The case where the DAC exhibits both static (ϵ_i) and dynamic mismatch (δ_i) of

0.1 % and 0.01 % resp. and where δ is 0.1 % is shown in fig. 4 as well. This clearly shows the need for a good compensation of both the static and the dynamic errors. This paper presents several techniques to do this, by fulfilling the restriction and by properly selecting the selection signals $S_i(k)$. To be able to fulfill the input code all the DAC's consists of twice as many elements as the maximum input code.

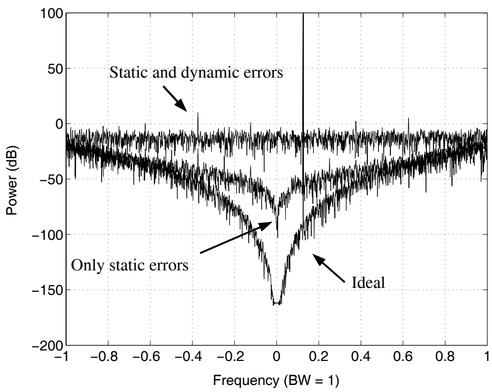

Fig. 4. Spectrum of a bandpass DAC in the signal band for an ideal DAC, a DAC with only static mismatch and a DAC with static and dynamic errors.

4.2. Realization with a vector quantizer

The restriction set in section 3 can be realized by setting an extra constraint to the general VQ of fig. 3: the selector may only turn on elements that were off during the previous clock period. Although the situation might seem similar to the low pass mismatch shaping DAC, it is not. In the low pass situation the VQ quantizer without the extra constraint will cycle as quickly as possible through the unit elements. Hence, the extra constraint is automatically satisfied [4]. However, in the bandpass case the VQ chooses more than once the same element during more then one clock period. Therefore the extra constraint could affect the effectiveness or stability of the shaping procedure of the vector quantizer. Therefore it is important to select an appropriate loop filter $H(z)$. In general $H(z)$ equals $\frac{-az^{-1}+z^{-2}}{1+z^{-2}}$. We noticed that the shaping and the stability is improved if a is given a small value (e.g. $a = 0.05$).

A simulation example of a DAC using the proposed VQ is shown in fig. 5, the DAC has the same static and dynamic errors as in section 4.1. The figure illustrates that both static and dynamic mismatch noise are second/fourth order shaped.

4.3. Realization with a 2 path transformation

Another way to ensure the restriction is dividing the DAC elements into two DAC's, see fig. 6. The input of each DAC

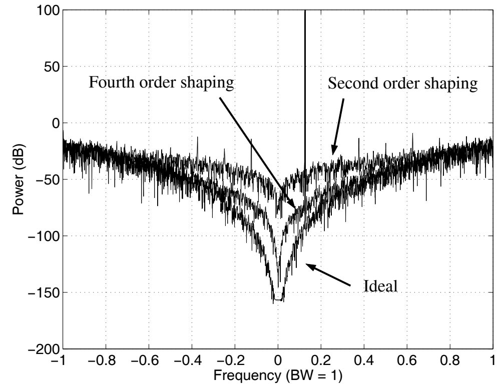

Fig. 5. Spectrum of a bandpass DAC in the signal band for a 2nd and 4th order bandpass shaping VQ.

path is obtained by a 2 path transformation of the overall input $D(k)$. As both DAC's are working alternately, no element is turned on during two or more consecutive clock periods. The selection signals $S_i(k)$ are generated by applying a high pass mismatch shaper in each DAC, with e.g. an MTF of $(1 + z^{-1})$. This high pass MTF can be implemented using a VQ or the more hardware efficient high pass DWA [3] in the case of second order shaping. Due to the 2 path transformation the MTF of the overall DAC equals the ideal bandpass MTF of $(1 + z^{-2})$ [3].

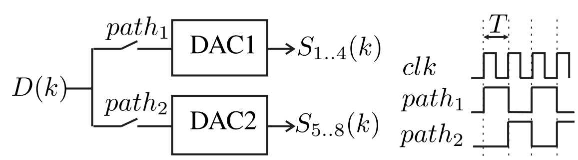

Fig. 6. Two path realization of the restriction.

In general, however, the two DAC's have an unequal gain. Therefore, the input signal $D(k)$ will be amplitude modulated with a Nyquist rate (f_N) signal. This causes (mirror) frequencies $f_m = f_0 + f_N$ folding back to f_0. In the frequency domain this corresponds to substituting z by $-z$. For bandpass DAC's with central frequency equal to $\frac{f_s}{4}$ ($z \approx j$) the mirror frequencies are situated around $z \approx -j$. In a non-complex DAC the noise energy around $z = -j$ is low for the same reasons as it is low around $z = j$. So, noise folding is not a problem here. However, an attenuated version of the negative frequency component of a signal with frequency $\frac{f_N}{4} - f_1$ (i.e. $\frac{3f_N}{4} + f_1$) will occur at $\frac{f_N}{4} + f_1$, causing a mirror signal.

The spectrum of a simulated DAC using the proposed technique with a first and second order high pass shaper in each DAC is shown in fig. 7. The static and dynamic errors are the same as in section 4.1. The figure illustrates that both the static and dynamic mismatch noise is second/fourth order shaped. It also shows the mirror signal. For many applications this mirror may be tolerable [5].

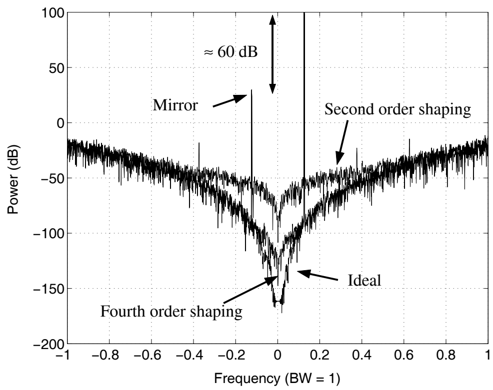

Fig. 7. Spectrum of a bandpass DAC in the signal band for the 2 path transformation of two 1st and 2nd order high pass shaping DAC's.

4.4. Realization with a hardware efficient tree structure

The tree structure of [2] with twice as many unit elements is a hardware efficient structure that automatically achieves low pass shaping of the total DAC error [4]. For bandpass shaping something similar can be done by modifying the tree of [2]. The proposed tree is shown in fig. 8. Compared to the normal tree structure only the leaf nodes (marked S_{l1}) are modified. In this layer the element selection is a VQ structure as described in section 4.2. It is actually this layer that ensures that no element is turned on during two or more consecutive clock periods as required by the restriction. To be able to do this, the inputs ($y_{1\ldots4}$) of the 2 element DAC's (elements S_{l1}) may at maximum be 1 (see section 4.2). This is automatically ensured by the selection logic of S_{l3} and S_{l2}, if the number of unit elements is twice the maximum input code D.

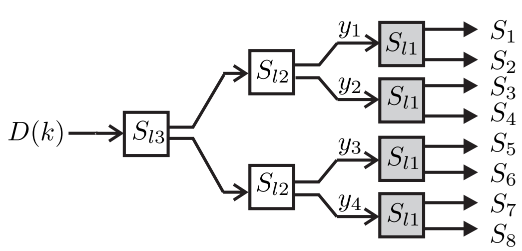

Fig. 8. The proposed tree structure for an 8 element DAC, the input $D(k)$ is at maximum 4.

A simulation example of a DAC using the proposed modified tree is shown in fig. 9, again the DAC has the same static and dynamic errors as in section 4.1. For the vector quantizers in layer 1 the same filter as in section 4.2 was chosen. The modified tree structure is more hardware efficient as the selection logic is distributed over different layers and because of the very easy sorting algorithm (comparison of two values) in the VQ structures of layer 1.

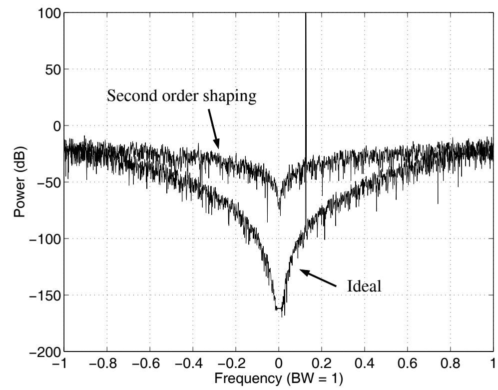

Fig. 9. Spectrum of a bandpass DAC in the signal band for the proposed bandpass shaping tree.

5. CONCLUSIONS

This paper described a model for the static and dynamic errors in multibit DAC's. Based on this it was shown that addressing both errors can be done by using twice as many unit elements. Several techniques to achieve bandpass mismatch shaping are presented. First, a vector quantizer is presented. This structure is considered to be hardware expensive, but it achieves 2nd and 4th order shaping. Next, a 2 path transformation of two high pass DAC's was introduced. It too achieves 2nd and 4th order shaping, while the 2nd order situation can be made hardware efficient when high pass DWA is used in each path. However, a mirror signal appears in the spectrum. Finally a hardware efficient structure achieving 2nd order shaping was obtained by using a modified version of the tree structure.

6. REFERENCES

[1] R. Schreier and B. Zhang, "Noise-shaped multibit D/A convertor employing unit elements," *Electronics Letters*, vol. 31, no. 20, pp. 1712–1713, Sept. 1995.

[2] I. Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," *IEEE Trans. Circuits Syst.-II*, vol. 44, no. 10, pp. 808–817, Oct. 1997.

[3] T. Shui, R. Shreier, and F. Hudson, "Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 331–338, Mar. 1999.

[4] J. De Maeyer, P. Rombouts, and L. Weyten, "Addressing Static and Dynamic Errors in Unit Element Multibit DACs," *Electronics Letters*, vol. 39, no. 14, pp. 1038–1039, Jul. 2003.

[5] S. Bazarjani and W. M. Snelgrove, "A 160-MHz Fourth-Order Double-Sampled SC Bandpass Sigma-Delta Modulator," *IEEE Trans. Circuits Syst.-II*, vol. 45, no. 5, pp. 547–555, May 1998.