SOI thickness uniformity improvement using wafer-scale corrective etching for silicon nano-photonic device

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Spectral response of high-index contrast silicon nano-photonic devices are very sensitive to small dimensional variations. The change in the device dimension is mainly caused by thickness/height and width of the device. While the later can be controlled by using high resolution patterning technology, such as e-beam lithography or advanced optical lithography. However, thickness or height of the device is largely dictated by the wafer manufacturing process. In this paper, we present our recent work on thickness non-uniformity improvement using Gas Cluster Ion Beam-Location Specific Processing where the thickness non-uniformity over a 200 mm is reduced by 50% by using this process.

Introduction

High-refractive index silicon-on-insulator based photonic integrated circuit platform have matured over the past years. Various active and passive functionalities have been demonstrated with good performance figures close to commercial requirements. However, silicon photonics, despite taking advantage of high volume CMOS compatible fabrication is struggling to become a main-stream integrated circuits platform. One of the main reasons for such failure is its extreme sensitivity of the device to small variations in device dimension, or in other words less tolerant to fabrication non-uniformity/variability. For example, one nanometer in thickness variation would result in about two nanometer shift in the device spectral response and one nanometer width variation would result in one nanometer shift in device response. These variations could be fatal in lot of applications, such as, optical filters in optical communication network [1]. We have already demonstrated that by using high resolution fabrication process width variation within a 200 mm wafer could be reduced to 2-3 nm [2]. In this work, we address the issue of thickness variation control over a 200mm wafer using location specific processing where we demonstrate that by using corrective etching thickness non-uniformity could be reduce by over 50%.

Thickness correction process

Thickness non-uniformity over the wafer is dictated by the wafer manufacturing process. A typical non-uniformity specification for a 220 nm thick Si layer over a 200 mm SOI is 10%, i.e. 22 nm over the wafer. This non-uniformity is simply not acceptable for many

applications. In this work, we use Gas Cluster Ion Beam (GCIB) process to correct the thickness variations by using location specific processing (LSP) [3]. Figure 1 shows a schematic of a GCIB system. The GCIB tool generates clusters by passing high pressure process gas thru a proprietary nozzle into a low pressure beamline. The clusters are ionized and accelerated, creating a directional, energetic chemical beam. The beam is fixed in position and the wafer is scanned in front of it. SOI thickness uniformity improvement is achieved by utilizing an etch process gas and adjusting the scanner velocity across the wafer so that local etch amounts can be varied, producing precise thickness control.

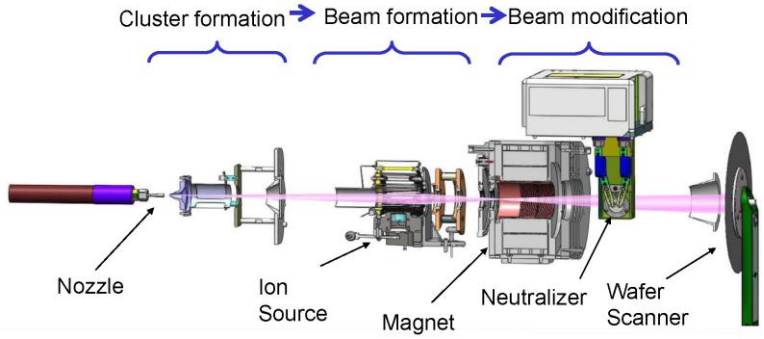


Figure 1 Schematic of GCIB system

Since the thickness control is achieved by removing material from the surface the final thickness of Si depends on the lowest etch rate achievable by the GCIB process and the minimum thickness of the uncorrected wafer. In order to decouple these two factors from the achievable target thickness we propose a route where the Si thickness of the incoming wafer is increased by using epitaxial growth. Figure 2 shows the proposed route to achieved desired Si thickness after thickness uniformity correction using GCIB process.

During the correction process high energy radicals increases the surface roughness and amorphisation occurs at the Si surface during this thickness correction process. Even though these two side-effects are detrimental to device performance in terms of additional loss we have explored ways to recover the surface quality through post correction treatments discussed in the following section.

Thickness correction and device fabrication

Figure 3 show experimental result of the thickness uniformity improvement using GCIB-LPS. Figure 3a shows the thickness uniformity after increasing the thickness of Si from 220 to 245 nm, which has a 3sigma non-uniformity of 3.2 %. After correcting the thickness non-uniformity while targeting a thickness of 220 nm we have improved the thickness non-uniformity to 0.6% (Table 1).

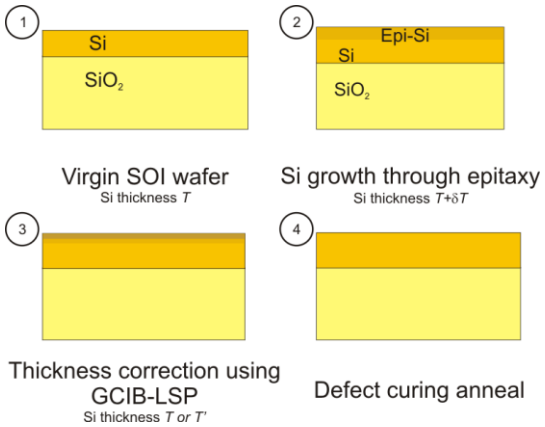
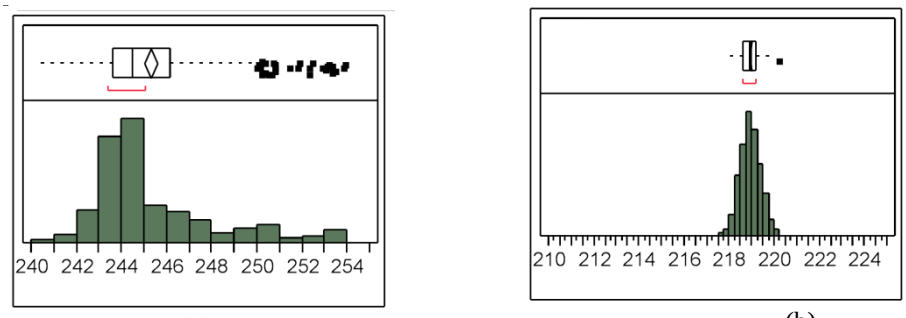


Figure 2 Thickness correction process flow route.

Table 1 Wafer statistics

	Pre-correction	Post-correction
Mean (nm)	245	219
Range (nm)	13.5	2.5
3sigma (%)	3.2	0.6

As mentioned earlier the correction process creates surface defects. After correction process some of the wafers were thermally annealed at 900C for 10min in N2 atmosphere. After annealing the wafers were patterned with 450 nm wide spiral photonic wire waveguide of different length (1-7 cm) to access the propagation loss and two identical racetrack ring resonators placed 25 um apart to access device uniformity. Patterning is done by using 193nm optical lithography and dry etching process [4]. We also patterned shallow etched grating fiber-chip couplers for in and out coupling of light though the waveguides [5].



(a) (b)

Figure 3 Thickness distribution (a) after epi targeting 245 nm Si and (b) after thickness correction targeting 220 nm.

Propagation loss and device characterization

After device fabrication, propagation loss of photonic wires were characterized using a SLED and optical spectrum analyzer. TE polarized light is coupled in and out though the grating couplers. Figure 4a shows the propagation loss of photonic wire waveguides. As mentioned earlier waveguides after correction had very high loss of ~50 dB/cm while

wafers that went through thermal annealing exhibited a loss of 4dB/cm compared, which is over a 10 fold decreases and only 1dB more than untreated photonic wire loss of same dimension. This reduction in loss can be attributed to reducing in surface defect; amorphous layer.

Figure 4b shows the spectral response of race track ring resonator from three nominally identical dies placed ~100 mm apart. We observed a non-uniformity of ~1.8 nm over this distance scale and 0.2 nm within a die. Even though this is a limited measurement this is a good indication of the uniformity. And requires detailed full wafer measurement, which is the primary focus in the work.

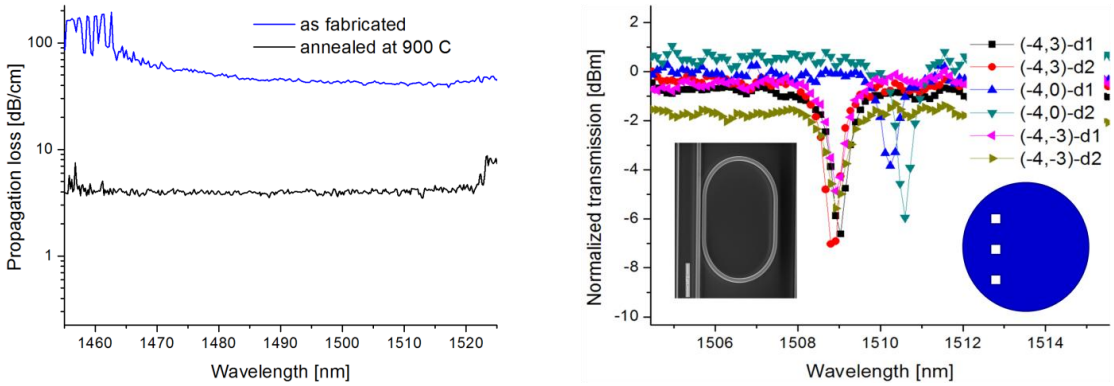


Figure 4 (a) Propagation loss of 450 nm Photonic wire as fabricated (after LSP) and after defect curing anneal. (b) ring resonator uniformity over a distance scale of 100 mm

Summary

We have demonstrated Si thickness uniformity improvement using GCIB corrective etch process. The uniformity of a virgin 200 mm SOI wafer was improved by 50 %. The damage created during the corrective etch is cured by thermal annealing by which the loss was reduced from 50 dB/cm to 4 dB/cm. We have achieved a short range (intra die) non-uniformity of ~0.2 nm and long range (inter die) non-uniformity of ~1.8 nm.

Reference

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