Novel Modeling Strategy for a BCI set-up applied in an Automotive Application

An industrial way to use EM simulation tools to help Hardware and ASIC designers to improve their designs for immunity tests.

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Abstract- **Electronics suppliers of automotive industry use BCI (Bulk Current Injection) measurements to qualify immunity robustness of their equipment whereas electronics components manufacturers use DPI (Direct Power Injection) to qualify immunity of their component. Due to harness resonances, levels obtained during a BCI test exceed standard DPI requirements imposed by automotive suppliers onto components' manufacturers. We propose to use BCI set-up modeling to calculate the equivalent DPI level obtained at the component level during equipment testing and to compare results with DPI measurements realized at IC level.**

Keywords-component: BCI; modeling; IC immunity; DPI

I. INTRODUCTION

The BCI (Bulk Current Injection) [1] test is probably the most severe immunity test used by automotive suppliers to test and qualify their electronic equipment. During IC sourcing, the EMC design engineers specify EMC requirements imposed on the component to fulfill the needed product performance. In terms of immunity robustness, a standard value of 30dBm is generally required for a DPI (Direct Power Injection) [2] test at component level for pins connected to the harness. But due to harness resonances and harness terminations specific to an application, this value could be too low or too high. During ASIC (Application Specific Integrated Circuit) development with tight planning milestones, automotive suppliers and component manufacturers also need to know how DPI measurements fit to levels observed during a BCI test to precisely identify the frequency bands where improvements are absolutely necessary. BCI set-up modeling is also helpful to simulate different product or load box configurations and predict final immunity behavior.

For Continental Automotive France, this study is in continuation of Work Package 1 of French Aerospace Valley labeled EPEA (EMC Platform for Embedded Applications) project. Continental's purpose was to promote a direct approach to build a global immunity model from injection probe to the pin of the component using unique S-parameter measurements. For Melexis NV and Ghent University (Belgium), this work fits within the framework of a research project called GoldenGates on EMC-aware modeling and design funded by IWT –Flanders (Agency for Innovation by Science and Technology).

II. BCI SET-UP DESCRIPTION

A. Automotive application

The chosen application is a Stand Alone cylinder Pressure Sensor (SAPS) used in engine management (figure 1).

Figure 1. Stand Alone cylinder Pressure Sensor

The sensing element is embedded into a specific mechanic and connected to an ECU (Engine Control Unit) by means of multi-wire harness. The SAPS contains an ASIC developed by Melexis according to Continental's specifications which amplifies the signal coming from sensing cell, formats and transmits the measurement to the ECU.

B. *BCI test set-up*

The BCI test set-up is illustrated by figure 2. The real set-up has been simplified to focus only on specific signals.

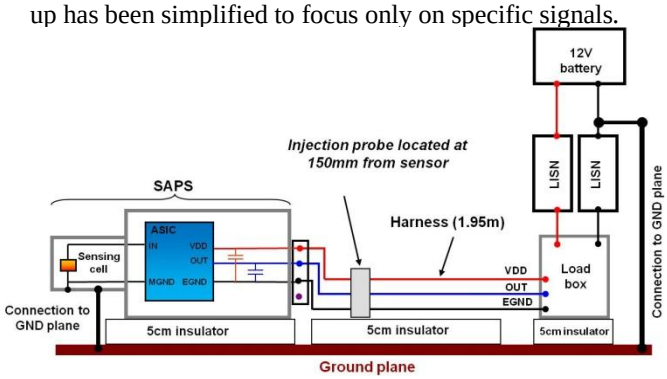

Figure 2. BCI test set-up

The SAPS and its harness are lying on 5cm thick insulator. The harness is terminated by a load box representing the ECU input. Power is provided by a 12V battery thru two LISNs (Line Impedance Stabilizer Network) to the load box which provides 5V power called VDD to the sensor. Monitoring of measurement called OUT is done by means of an optical converter and optical fibers which are not represented in figure2. VDD and OUT signals are referenced to the electrical ground of the ECU called EGND.

The BCI injection probe is placed at 150mm from the sensor. As in a vehicle the SAPS will be screwed into the engine, so the sensor's body is connected to the test table, which is connected to the GND of the battery.

In this configuration, the sensing cell reference pin called MGND is connected to the sensor's body and accordingly to the ground plane. The sensing cell active pin called IN is also connected to the ASIC. Summarizing, the ASIC receives amongst others signals an electrical GND (EGND) which is the reference of output signal (OUT) and also a mechanical GND (MGND) which is the reference of the sensing cell input (IN).

Figure 3. Picture of real BCI test set-up

III. BCI SET-UP MODELING

The BCI set-up modeling has been realized thanks to a close cooperation between Continental, Melexis and Ghent University. The ASIC and its test boards were designed by Melexis. Ghent University developed the harness and sensor body models. Simulations of the full BCI set-up were done by Ghent University using Agilent's ADS and by Continental using CST Studio Suite 2011.

A. *BCI test set-up modeling principles*

As described in Figure 4, the BCI set-up modeling considers several components:

ASIC: The device was modeled by its S-parameters in accordance with future IEC62433-4 ICIM-CI [3] (Integrated Circuit Immunity Model-Conducted Immunity) standard. Measurements have been performed by Ghent University with an Agilent 4-port PNA-X Vector Network Analyser on a special test board developed by Melexis. Thanks to careful board design, using very short traces, S-parameters measurements did not require extensive de-embedding. In contrast to DPI test boards, the test board did not include coupling capacitors and decoupling inductors so that external bias tees and DC blocks had to be used. As the ASIC MGND is connected to the reference GND, a 4-port measurement is necessary: IN, OUT, VDD and MGND, using EGND as reference. EM Simulation tools as ADS or CST Studio Suite 2011 are able to import Touchstone files.

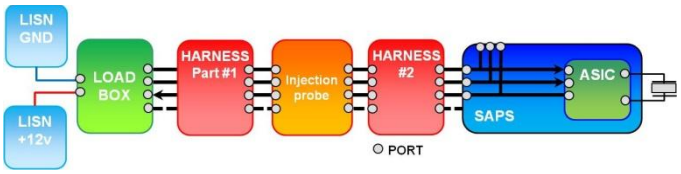

Figure 4. BCI test set-up modeling

SAPS body: This mechanical component has been modeled from a CAD model imported into CST Microwave Studio (MWS). Geometries and design have been simplified to reduce the calculation time. CST MWS allows creating S-parameters file in Touchstone format with measurement ports adequately placed on the design. S-parameters extraction has been made by Ghent University by defining 9-ports: IN_A, OUT_A and VDD_A at connector side, IN_B, OUT_B and VDD_B at ASIC side and IN_C, OUT_C and VDD_C at the input of sensor to investigate the efficiency of input filtering.

Harness: This part was modeled in two parts to take into account the position of injection probe which could be located at 150, 450 or 750 mm from the sensor. The 4-wire harness (VDD, EGND, OUT + an optional wire) has been described as a multi conductor transmission line (MTL) via a quasi-TM RLGC modeling technique, based on the use of a Dirichelt-to-Neumann boundary operator [4]. S-parameters have been extracted by Ghent University in Touchstone format to allow importing them in another EM simulator. CST Cable Studio also allows harness modeling from geometric parameters (cross section) and material characteristics. This modeling takes also in account the ground plane and the 5cm insulator.

Injection probe: The probe was modeled as a simple circuit element being a constant current source coupled to ideal transformers. Current source output impedance has been fixed to 100 Ohms which is the load used during the calibration of the BCI equipment. Current source peak value equals square root of 2 x RMS value of injected current (0.5 A for 111 dBµA injected as example). More advanced probe models, including

losses, can be found in literature, e.g. [5], but the simple model used here – not including losses – is acceptable, as it leads to worst-case results.

Load box: A circuit representation was used for this element. A load box is specific for each car manufacturer. Typical load boxes are second-order passive filters. Connection wires to LISN were not taken into account.

LISN: We used a standard first order circuit model with 5 µH inductance in parallel with 50 Ohms resistor in series with a 100 nF capacitor.

Note that the complete BCI set-up model has been reduced to a first order model as our interest is not to have a precise model of each element but to quickly estimate a worst case situation during a BCI testing to be able to correct the ASIC design or to modify the ASIC environment.

S-parameters were initially measured from 10MHz to 400MHz to cover all BCI frequency bands (150 KHz to 400 MHz). Between 150 KHz to 10 MHz, the use of an impedance analyzer to measure the S-parameters is more appropriate than the use of a VNA. The S-parameters measurements have been also extended to 3GHz to allow investigations at frequencies where Radiated Immunity plays a role.

B. BCI test set-up modeling

Figure 5 shows the final model as built with CST Studio Suite.

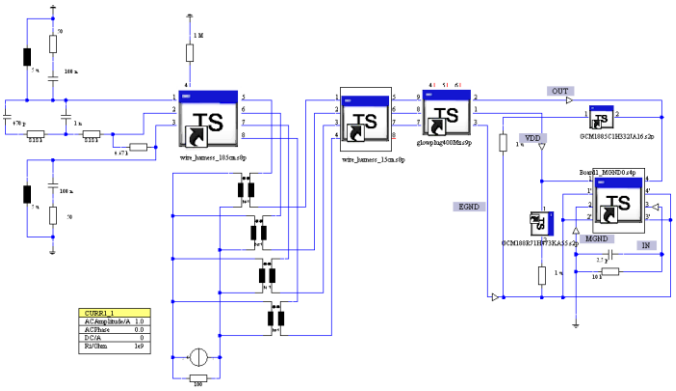

Figure 5. BCI test set-up modeled under CST studio

Probes are positioned on signals VDD, EGND, IN, OUT and MGND to measure RF voltages and RF currents on each pin of the ASIC. Note that for VDD and OUT, probes are placed before decoupling capacitors to be in accordance with the procedure required for DPI measurements on Melexis test board. Passive components' models are generally available on the manufacturer's website.

Note that the load box mechanics as well as the connecting wires between load box and LISN are not taken into account in the model. This will have some consequence in a resonance frequencies' calculation but our goal is more to describe a method than to create a precise model.

The main interest of the BCI set-up modeling is to intend to compare the immunity of an Integrated Circuit during the BCI test which is a pure common-mode and multi-pin aggression with the IC's immunity during a DPI test which is a pure differential-mode and mono-pin aggression.

IV. ELECTROMAGNETIC SIMULATION

As mentioned previously, probes will measure RF voltages and RF currents on each pin of the ASIC. According equivalent circuit given in figure 6, the equivalent DPI power P_{DPI} could be calculated at the four pins by following formula:

$$P_{DPI} = |V_{DPI}|^2 / 400$$

with $V_{DPI} = (50*I_{RF}) + V_{RF}$, where V_{RF} is the RF voltage measured by the probe and I_{RF} is the RF current flowing into the pin also measured by the probe.

DPI power is expressed in dBm (0 dBm = 1 mW)

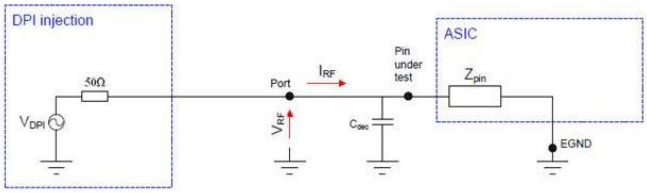

Figure 6. Equivalent circuit of DPI

A. BCI test set-up: voltages and currents calculation

The calculated voltages resulting from an AC simulation are given in figure 7. As GND reference for CST studio is the ground plane, meaning MGND in this case, differential voltages have been calculated compared to electrical ground EGND.

We observe that differential voltage between mechanical and electrical grounds is much over 1 Volt almost over the full BCI frequency band. 1 Volt is the maximum acceptable voltage between both grounds for nominal ASIC operation. Of course as the sensing cell input IN is linked to MGND by means of a small capacitor, the IN voltage will follow the MGND one.

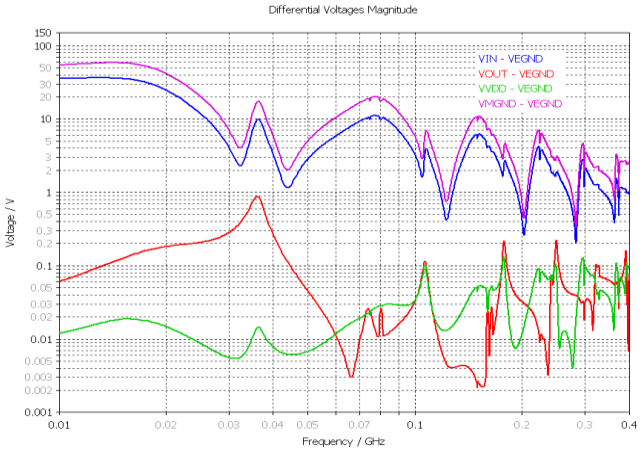

Figure 7. Calculated differential voltages (magnitude)

The result is sufficient to state this configuration could not withstand BCI requirements without additional capacitors between both grounds.

The calculated currents resulting from an AC simulation are given in figure 8.

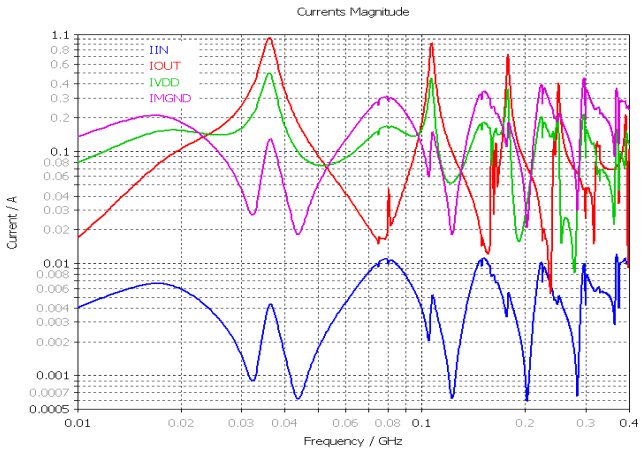

Figure 8. Calculated currents (magnitude)

We clearly observe the resonance of the harness on the OUT signal. As illustrated by figure 9, the termination of OUT signal is high impedant at the load box side when its termination is low impedant (4.7 nF capacitor) at the sensor side. The wire will act as a quarter-wavelength antenna. The length of the harness equals a quarter-wavelength at ~37,5 MHz. At this frequency and periodically at (2n+1)*37,5 MHz, n=0,1,2,…., the current flowing into the pin is at its maximum. When the harness length equals an half-wavelength at ~75 MHz and periodically at n*75 MHz, n=0,1,2,…, the opposite phenomenon occurs, i,e, the current flowing into the pin is at its minimum.

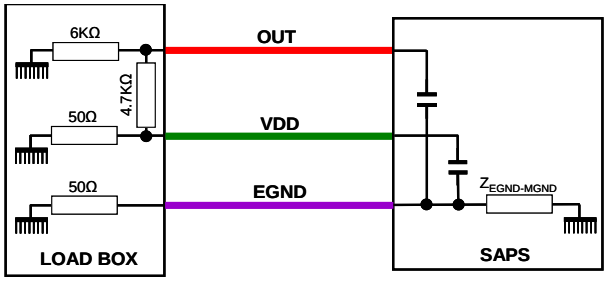

Figure 9. View of impedances on harness' wires

Figure 9 also clearly puts forward the common-mode impedance mainly constituted by $Z_{EGND-MGND}$ at ASIC level.

Resonances are different for VDD, EGND and consequently for IN signal. Their termination is low impedant (50 Ohms) at the load box's side and at the sensor side. The wire harness will act as a half-wavelength antenna. The current's maximum at the sensor side will be now at n*75 MHz, n=0,1,2,….while the current's minimum will be at (2n+1)*37.5 MHz, n=0,1,2,…. But as at the load box side, OUT is linked to VDD thru a 4.7 KOhms pull up resistor, VDD will also follow the OUT signal creating a mix of both signals.

B. BCI test set-up: equivalent DPI level calculation

Equivalent DPI level calculation is done thru a standard commercial calculator. We just need to export each voltage and current calculation in frequency-magnitude-phase format or frequency-real-imaginary part format.

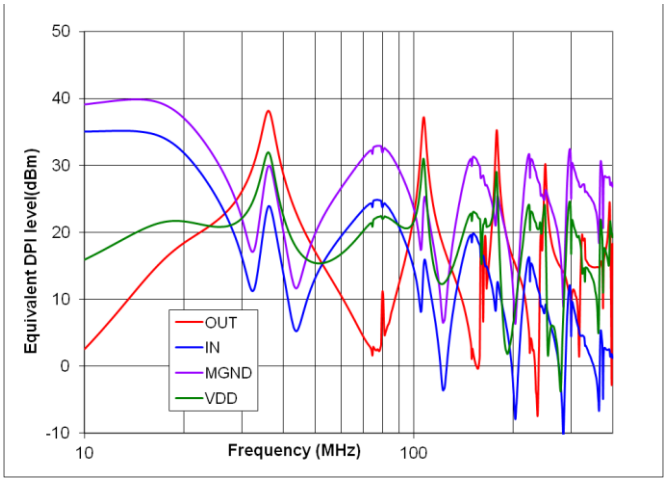

Figure 10. Calculated equivalent DPI level (magnitude)

Equivalent DPI level calculation shows in figure 10 that with an maximum injection level of 111 dBµA, the 30dBm Continental's requirement for external pins is not fulfilled for VDD (32 dBm max) and OUT (38dBm max) pins due to the harness resonance. The calculated levels are still more critical for MGND (40 dBm max) and IN (35 dBm max). As they are considered as local pins - means not connected to the harness - their immunity requirement is quite less (12dBm).

C. BCI test set-up: influence of the load box

To reduce harness resonance on the OUT signal, the load box was modified. A 4.7 nF capacitor has been now placed between OUT and EGND.

We clearly observe in figure 11 the influence of the added capacitor on the equivalent calculated DPI level on OUT pin and consequently on the other pins. Now, for the same injection level of 111dBµA, the 30dBm requirement on OUT (30 dBm max) and VDD (24 dBm max) pins is quite sufficient.

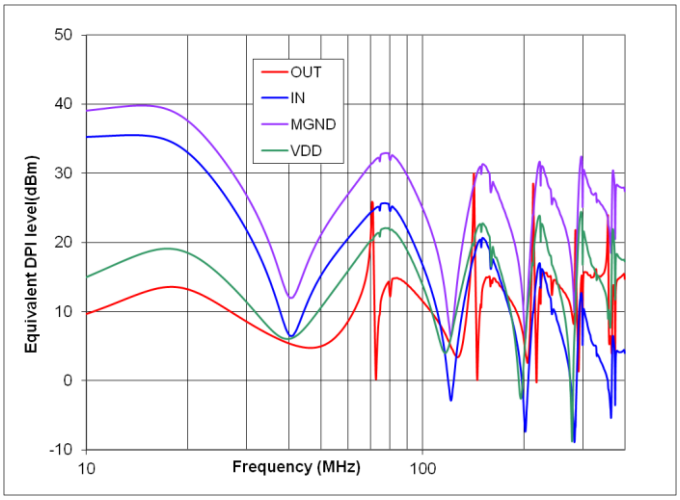

Figure 11. Calculated equivalent DPI level (magnitude)

D. BCI test set-up: Improvement proposal

Now, an improvement is proposed, that also was simulated and tested. This solution, described in figure 12, consists of adding a 470 nF capacitor between electrical and mechanical grounds and ferrite beads (470 Ω@100 MHz) on the OUT and VDD signals. The 470 nF capacitor between EGND and MGND clearly intends to reduce the common mode impedance.

The modification is easy to implement into the circuit simulator.

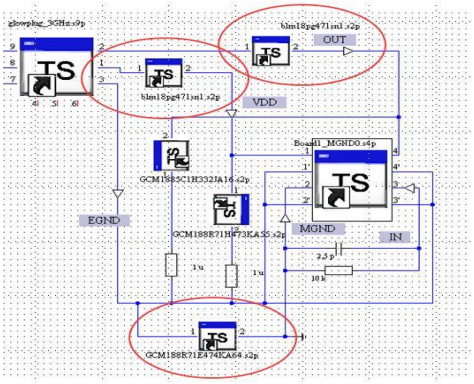

Figure 12. Improvement proposal implementation

The equivalent DPI level calculation shows (figure 13) a great improvement:

- Up to 80 dB level decrease for MGND and IN pins at lower frequencies and up to 30 dB at higher frequencies. We may observe that due to itself resonance frequency, the 470 nF capacitor between grounds is mainly efficient for low frequencies.
- Up to 5dB decrease for OUT and up to 10dB for VDD signal due to ferrite beads.

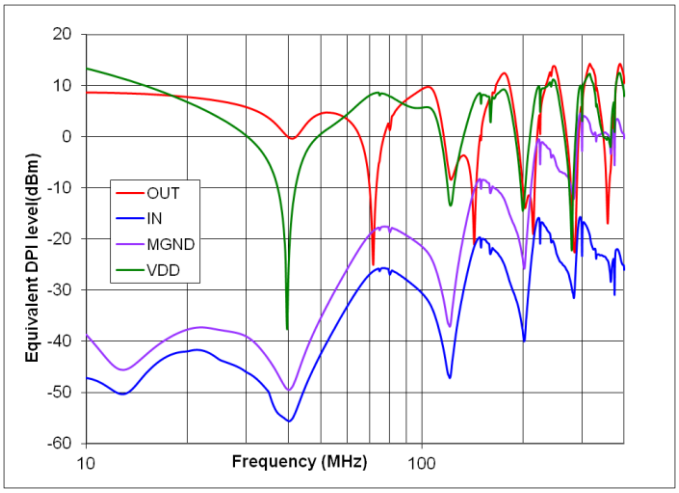

Figure 13. Calculated equivalent DPI levels of improved design (magnitude)

E. Correlation with measurements

The BCI measurement realized on the improved solution and showed figure 14 shows failure points mainly between 250MHz and 350MHz. We are interested to know if this result was predictable using the calculated equivalent DPI levels.

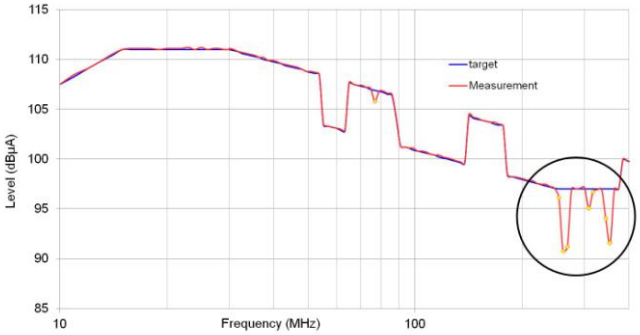

Figure 14. BCI measurement of improved design

Before any comparison with DPI measurements, the following comments should be stated:

- As showed in figure 14, the BCI injection level is frequency dependant while the equivalent DPI calculation was made with a constant current source (111dBµA). As our BCI set-up model exhibits a purely linear behavior with the injection current level, the correction factor to be applied on calculated equivalent DPI level is simply achieved by applying the same scaling factor for each individual frequency,
- To make a correct comparison of transmitted powers, we must take care that, for each signal, the impedance seen at probing point during BCI simulation be the same as the impedance seen at DPI injection point on board. That means S-parameters measurements have to be realized on the board used for DPI measurement.

Figure 15 shows the comparison between DPI measurements on the OUT pin and its equivalent DPI level calculated by using the BCI model. Failures during the BCI test are indicated by a yellow square.

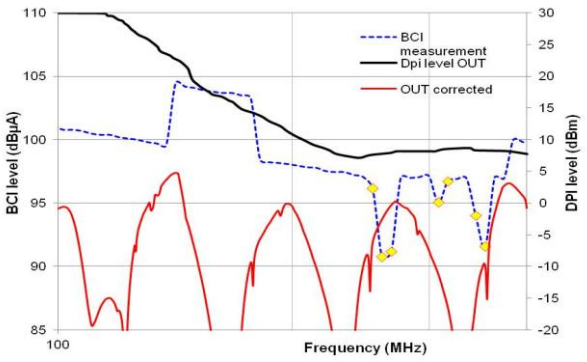

Figure 15. Modeled BCI / DPI measurement comparison

We observe that failures occur in this area where the OUT pin's immunity is at its lowest and this in particular when a maximum equivalent DPI level is observed due to harness resonance. We expected to clearly see a BCI failure occurring when equivalent calculated DPI level (red curve) goes above DPI level (black curve) but this did not happen.

Differences between measurements and simulation results could be easily explained:

- Gap in frequencies: the harness resonance frequency shifts due to the lack in the model of physical connections between load box and LISN. Also, neither the length of the load box neither the length of the SAPS body to reference ground has been taken in account. The comparison shown by figure 16 between measured currents and calculated current on the harness wire shows 17 MHz shift in quarter wavelength frequency.

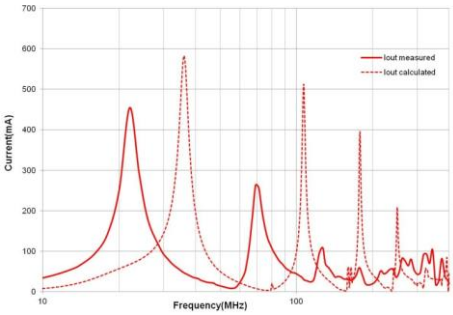

Figure 16. Measured current vs calculated current on harness' wire

- Gap in levels: the model of the injection probe is very simple. The comparison shown in figure 16 between measured currents and calculated currents on harness wire shows also some discrepancies. Note, however, that our model of the injection probe leads to worst-case results at the resonance frequencies.
- We have reduced the comparison to the OUT pin only because its immunity level is weak in the considered frequency band (< 10 dBm). But some coupling inside the IC is possible and IC local pins, a priori not considered in the model, with low immunity as VDDA can also be a path for the incoming perturbation.

In any case, the comparison between calculated equivalent DPI level and DPI measurements is sufficient to conclude that an improvement of the ASIC's output stage in 250-350MHz range is necessary.

V. CONCLUSION

We have presented a simple method to be used by electronics industrials and automotive suppliers, allowing predicting IC behavior during a BCI test on equipment. This method leverages IC's S-parameter measurement, incorporated as Touchstone data in a modeled environment. The use of EM simulation tools now offer accurate PCB, cable and enclosure full-wave models which may be imported in a classic circuit calculator, allowing the user modular set-ups with controllable complexity.

The knowledge about the component's (ASIC's) behavior obtained from the modeling results, is essential for component manufacturers, hardware and ASIC engineers to assess its EMC-performance. Full advantage of the modeling results can be taken when proposing redesigns at circuit or module level.

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