Input Current Distortion of CCM Boost PFC Converters Operated in DCM

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***Abstract*— Power factor correction (PFC) converters for the higher power range are commonly designed for continuous conduction mode (CCM). Nevertheless, operation in the discontinuous conduction mode (DCM) occurs for light load in a zone, close to the crossover of the line voltage. This zone will gradually expand with decreasing load to finally encompass the entire line cycle. Whereas in CCM the parasitic capacitances of the switches only cause switching losses, in DCM they are a source of converter instability, resulting in significant input current distortion. In this paper, this source of input current distortion is analyzed and a solution is proposed. Experimental results are obtained using a digitally controlled boost PFC converter, designed to operate in CCM for 1kW.**

I. Introduction

For single phase power factor correction (PFC) converters, two main approaches are followed for the converter and control design. For low power applications, PFC converters are often operated in the discontinuous conduction mode (DCM) as they behave more or less as voltage followers [1]–[3]. As a result, no input current controller is required. On the other hand, higher power applications ask for operation in the continuous conduction mode (CCM) [4]–[9], since in DCM the device stresses and the conducted emissions become too high. An input current controller is now required, since the input current does not inherently track the input voltage.

For PFC, a boost converter is the most commonly employed topology. It is shown in Fig. 1 together with its typical two-loop control scheme. With this topology, a power factor near unity can be achieved when operating in CCM. Nevertheless, operation in DCM occurs for light load in a zone, close to the crossover of the line voltage [10], [11]. This zone will gradually expand with decreasing load to finally encompass the entire line cycle. When this occurs, the input current waveform is distorted due to the change in converter dynamics [10]–[13] or to errors on the input current samples when digital control is applied [11].

This paper deals with another cause of input current distortion, the influence of parasitic capacitances of the switches on the converter waveforms in DCM. Whereas in CCM these parasitic capacitances only cause switching losses, in DCM they cause oscillations in the converter waveforms. When input current control is applied, these oscillations may be a source of converter instability, resulting in significant input current distortion. This source of input current distortion will be analyzed and some possible solutions will be discussed. The theoretical analysis and a possible solution will be verified by experimental results, using a digitally controlled boost PFC converter, designed to operate in CCM at nominal power.

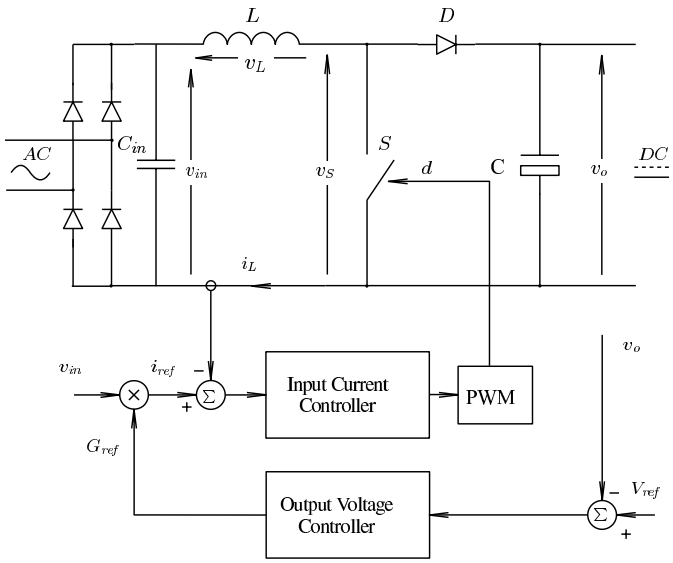

Fig. 1. The boost PFC converter, together with its control loops.

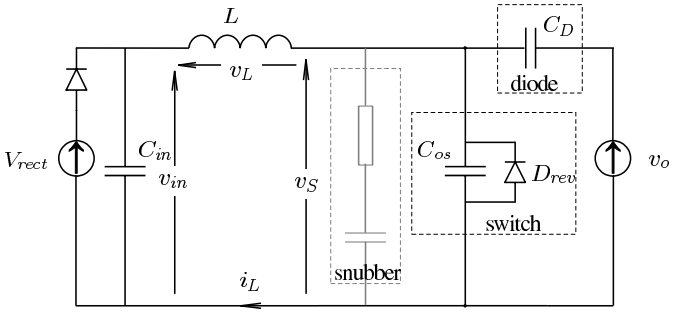

Fig. 2. Black: Equivalent network for the boost converter when both diode D and switch S are blocked; Gray: snubber

II. Influence of Parasitic Capacitances on the Boost Converter Waveforms

In this section, after a short study of the waveforms of a boost converter in the case of ideal switches, the effect of the parasitic capacitances of the switches on the converter

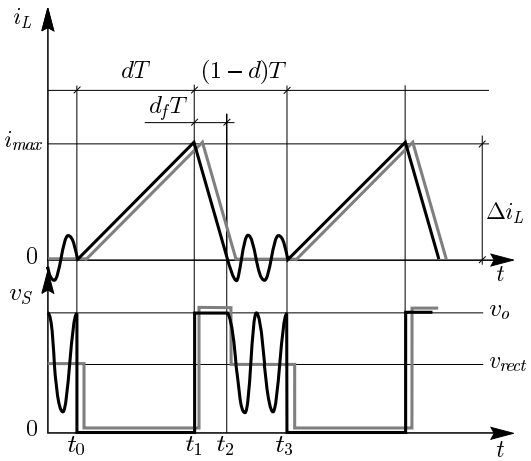

Fig. 3. Theoretical inductor current and switch voltage in DCM, high input voltage, black: ideal switches, gray: real switches

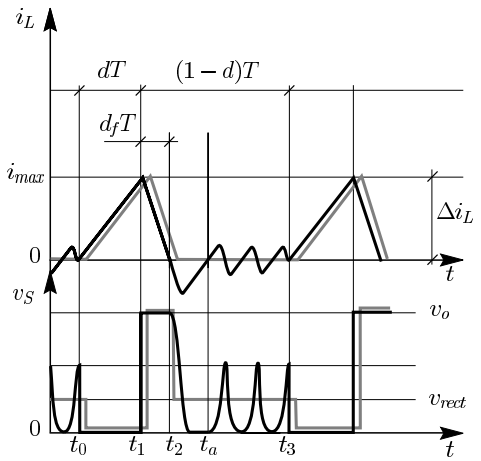

Fig. 4. Theoretical inductor current and switch voltage in DCM, low input voltage, black: ideal switches, gray: real switches

waveforms will be discussed. The converter is shown in Fig. 1, together with its control scheme, typically used for PFC.

A. Converter waveforms for ideal switches

In continuous conduction mode, the switch voltage v_S (Fig. 1) is either zero or equal to the output voltage v_o, corresponding to a closed or open switch S, respectively. As a result, the voltage across the inductor L will be alternately positive and negative, leading to a triangular inductor current waveform.

At reduced load, the inductor current may become zero before the end of the switching period (at t_2, Figs. 3 and 4, gray traces), resulting in discontinuous conduction mode. Assuming that both switch S and diode D are ideal, the switch voltage v_S adopts the value of the input voltage v_{in} as soon as the inductor current i_L reaches zero. During the remainder of the switching period ([t_2, t_3]), the switch voltage and the input voltage are equal while the inductor current is zero (Figs. 3 and 4).

B. Converter waveforms for real switches, high input voltage

For most applications in this power range, MOSFETs or IGBTs are employed as switching devices. One of their inherent parasitic elements, which has an important influence on the waveforms in DCM, is the output capacitance C_{os} (C_{oss} for MOSFETs, C_{oes} for IGBTs). The value of this capacitance is not only dependent on the type and the rating of the switch, but is also a non-linear function of the switch voltage v_S. Another component whose parasitic capacitance causes similar effects is the output diode D. Its parasitic capacitance C_D is generally lower than the parasitic capacitance C_{os} of the switch.

At the instant t_2, where the inductor current reaches zero in DCM, the converter can be represented by the network of Fig. 2 (black lines), with as initial conditions: $v_{in} = v_{rect}$, $v_S = v_o$ and $i_L = 0$A. As the voltages across the capacitances of this circuit are not in equilibrium, this results in oscillation. If the input capacitor C_{in} has a small value compared to the capacitances C_{os} and C_D, the switch voltage remains at v_o during [t_2,t_3] and the input voltage oscillation can be approximated by:

$$v_{in} = v_o - (v_o - v_{rect}) \cos\left(\omega_{n,1}(t - t_2)\right), \qquad (1)$$

with $\omega_{n,1}$ the angular frequency of the oscillation. Note that the input voltage may become twice as high as the output voltage for low v_{rect}, leading to a high voltage stress across the bridge rectifier diodes (Fig. 1). Therefore, the capacitance value of the input capacitance C_{in} is chosen to be at least an order of magnitude larger than the combined capacitance of C_{os} and C_D.

If C_{in} is much larger than C_{os} and C_D, the input voltage v_{in} is constant and equal to v_{rect}. Hence, the oscillation in the interval [t_2, t_3] is dominated by the inductor L and the capacitances C_D and C_{os}. Assuming that C_D and C_{os} are linear capacitances, the switch voltage v_S and inductor current i_L can be approximated by (Fig. 3):

$$v_S(t) = v_{rect} + (v_o - v_{rect}) \cos\left(\omega_n(t - t_2)\right) \qquad (2)$$

$$i_L(t) = -\frac{v_o - v_{rect}}{Z_n} \sin\left(\omega_n(t - t_2)\right), \qquad (3)$$

with

$$\omega_n = \frac{1}{\sqrt{LC_n}} \qquad \text{and} \qquad Z_n = \sqrt{\frac{L}{C_n}}. \qquad (4)$$

The capacitance C_n in these expressions is equal to the parallel connection of the switch capacitance and the diode capacitance. The natural impedance Z_n is much larger than the parasitic resistances of the network, so the oscillation will be hardly attenuated. The oscillation is ended when the switch is turned on again (t_3). For low duty-ratios, this interval may take several oscillation cycles.

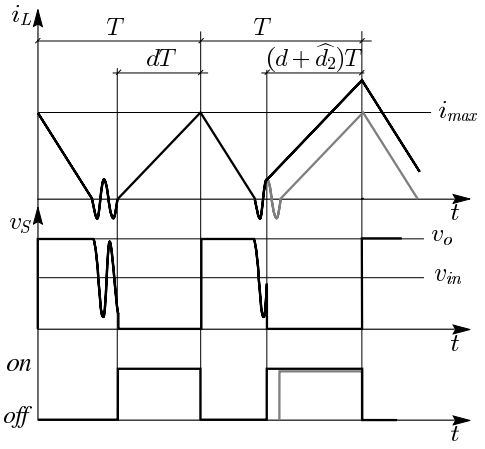

Fig. 5. Positive duty-ratio step, yielding a positive input current step

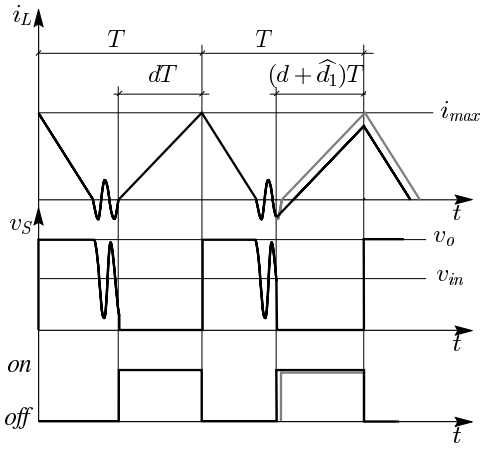

Fig. 6. Positive duty-ratio step, yielding a negative input current step

C. Converter waveforms for real switches, low input voltage

The converter waveforms in the case of low values of the input voltage v_{in}, are presented in Fig. 4. In (2), the switch voltage v_S, will exhibit negative values if the input voltage is lower than half the output voltage. If no reverse diode D_{rev} (Fig. 2) is integrated in the converter circuit, this may cause a breakdown of the switching device. Therefore, a reverse diode should be integrated in the circuit if the switch cannot withstand negative voltages and if it does not contain one intrinsically.

If a reverse diode is present and for a large input capacitor C_{in}, at t_2 the switch voltage swings down to 0V as $v_{in} < \frac{1}{2}v_o$ (2) (a non-linear capacitance results in a different condition). From this moment awards, the switch voltage will be clamped to zero, allowing the energy stored in the inductor L to flow to the input capacitor C_{in}. As a result, the input voltage v_{in} will rise until the current becomes positive again (t_a). The value of the input voltage at this instant is not equal to the rectified voltage v_{rect}, as the energy stored in the input capacitor C_{in} and the combined parasitic capacitance C_n at t_2 is now completely stored in the input capacitor C_{in} at t_a. The resulting input voltage can be calculated using an energy balance

$$\frac{1}{2}C_{in}v_{in}^2 = \frac{1}{2}C_{in}v_{rect}^2 + \frac{1}{2}C_n v_o^2, \tag{5}$$

yielding

$$v_{in} = \sqrt{v_{rect}^2 + \frac{C_{os}}{C_{in}}v_o^2}. \tag{6}$$

The non-linearity of the switch and diode capacitances can be expressed by replacing the second term in the right hand side of (5) by the total energy stored in the switch and output diode capacitances at the instant t_2. The resulting increase of the input voltage is important for low values of the line voltage only, since the second term in the right hand side of (5) is not depending on the input voltage.

An oscillation is now initiated at t_a, which is ended at the start of the on-time of the next switching period (t_3). Assuming a linear switch capacitance C_{os}, the switch voltage and inductor current can be approximated

$$v_S = v_{in}\left[1 - \cos\left(\omega_n(t - t_a)\right)\right] \tag{7}$$

$$i_L = \frac{v_{in}}{Z_n}\sin\left(\omega_n(t - t_a)\right), \tag{8}$$

which means that the switch voltage will oscillate between 0V and twice the value of the input voltage v_{in} at the instant t_a. In (7) and (8), ω_n and Z_n are given by expression (4). Due to the non-linearity of the switch and diode capacitances, the oscillation will not be sinusoidal (see Fig. 4).

III. Consequences for averaged input current waveforms

While in the previous section, the converter waveforms for a boost converter operated in DCM with a constant duty-ratio and constant rectifier voltage were discussed, in this section, the consequences of these waveforms, on the averaged input current waveforms of a boost converter, operated as PFC converter, are studied.

In the case of ideal switches, the input current averaged over one switching cycle is proportional to the square of the duty-ratio for DCM [11],

$$\langle i_L \rangle = \frac{v_{in}}{2L} \cdot \frac{v_o}{v_o - v_{in}} \cdot d^2 T, \tag{9}$$

so an increase of the duty-ratio will cause an increase of the input current, while a lower duty-ratio will lead to a lower averaged input current. Nevertheless, in the case of real switches, a positive step in the duty-ratio does not inherently lead to a positive step in the inductor current i_L. After all, though a step $\widehat{d_2}$ leads to an increase in inductor current (Fig. 5), a different step $\widehat{d_1}$ can result in a lower inductor current (Fig. 6). Consequently, the gain of the duty-ratio-to-input-current transfer function is depending on the magnitude of the step in the duty-ratio, and, due to the parasitic nature

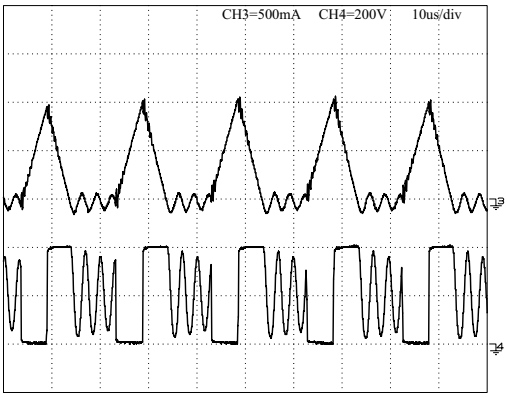

Fig. 7. Input current (upper trace) and switch voltage (lower trace) for high input voltage, experimental results

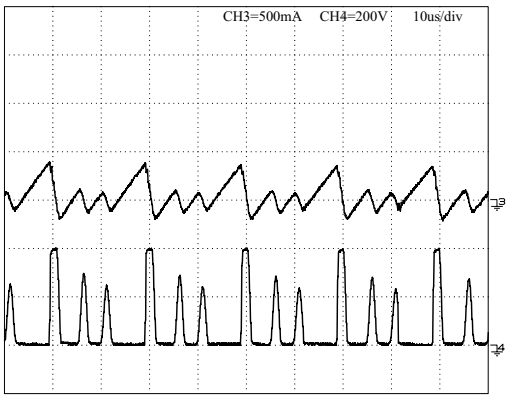

Fig. 8. Input current (upper trace) and switch voltage (lower trace) for low input voltage, experimental results

of the oscillation, unpredictable. Moreover, this gain can be both positive or negative at every moment, depending on the instantaneous value of the input current at the beginning of the on-time of the switch. This effect results in unpredictable inductor current behavior, causing inductor current loop instability and, as a result, input current distortion.

On the other hand, the variation of the input voltage can also result in averaged input current distortion, even when the duty-ratio remains constant (voltage follower operation), or varies very slowly (due to a low current controller gain). The reason is that the fraction of the switching cycle where the inductor current flows, $(d + d_f)$, not only depends on the duty-ratio, but also on the input voltage [11]

$$d + d_f = \frac{dv_o(t)}{v_o(t) - v_{in}(t)}. \tag{10}$$

As a result, the length of the time interval $[t_2,\ t_3]$ will vary as a function of the input voltage, and consequently, the phase of the oscillation at the start of the on-time of the next switching cycle (t_3) will change during a grid cycle. Hence, the oscillation during the switch off-time in DCM may cause severe distortion in the averaged input current waveform.

IV. Possible solutions

In section III. the effect of the input current oscillation on the averaged input current waveform and the input current control loop stability has been demonstrated. As the average input current depends strongly on the instantaneous input current at the beginning of the on-time of the transistor, any solution, resulting in a lower amplitude of the oscillation of the inductor current, will diminish this effect. Expression (3) reveals that this amplitude can be reduced by choosing switches, switch S and diode D, with a low parasitic capacitance, yielding a minimal value of C_n. To achieve this, a switch should be chosen which is as small as the application allows, since the switch output capacitance is closely related to the maximum switch current for a given switch type. As the converter is designed for CCM operation at a higher power level, demanding a high input current, large switching devices are needed. Since the parasitic capacitance of a switch is proportional to its current rating, this reduction is limited.

Another possibility to reduce the amplitude of the oscillation is to add a snubber. Among the numerous possible topologies for snubbers, a simple resistive snubber is chosen to demonstrate the principle (Fig. 2, gray lines). The capacitance value of the snubber capacitor must be chosen large enough to influence the oscillation, which means larger than the combined capacitance of the switch and diode parasitic capacitances. On the other hand, the switching losses, in DCM as well as in CCM, will increase drastically when the snubber capacitance is chosen too large. When adding the snubber to the circuit, the energy of the oscillation will now be dissipated in the resistor, causing the amplitude of the input current oscillation to fall quickly. As a result, in most cases the inductor current i_L will be zero when the switch starts conducting again, so the input current will not be distorted. Nevertheless, the first negative peak in the inductor current is hardly attenuated by the snubber. Consequently, some input current distortion will exist near border mode operation.

V. Experimental results

For the experimental verification of the waveforms obtained in previous sections, a 1kW boost PFC converter (Fig. 1) with following characteristics has been used

$$\begin{cases} V_g = 230\text{V}, & f_g = 50\text{Hz}, & f_{sw} = 50\text{kHz} \\ V_o = 400\text{V}, & C = 470\mu\text{F}, & L = 1\text{mH} \end{cases} \tag{11}$$

This converter operates in DCM during the entire line cycle when it is operated at 97W input power or lower [11]. The switch employed is an IRF840 MOSFET and the output diode is a RURP3060.

In Fig. 7, the instantaneous input voltage is near 200V, which gives large oscillations of the switch voltage. The oscillation is nearly sinusoidal as the switch output capacitance is quite linear in this voltage range. At low input voltage (72V for Fig. 8), the switch voltage will reach 0V, so the oscillation

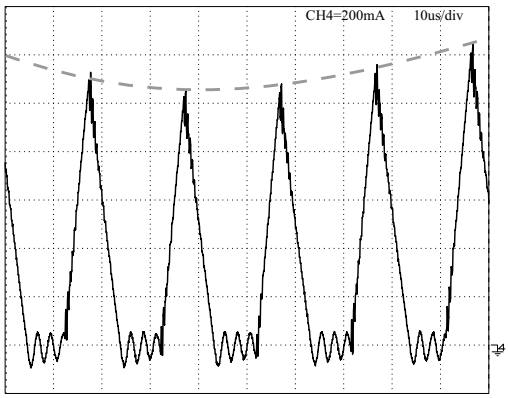

Fig. 9. Input current waveform without snubber

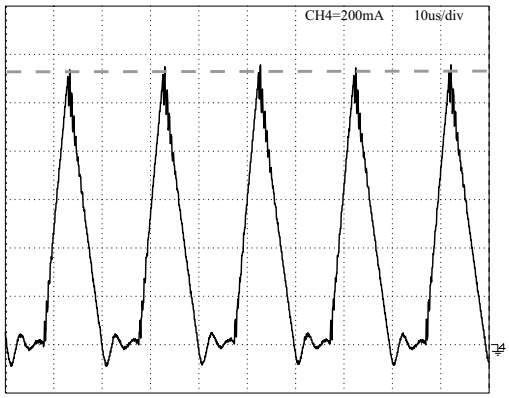

Fig. 10. Input current waveform with snubber

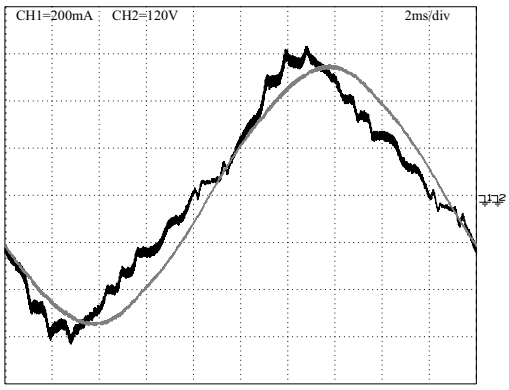

Fig. 11. Input current (black) and input voltage (gray) waveforms **without** snubber, controller designed for CCM

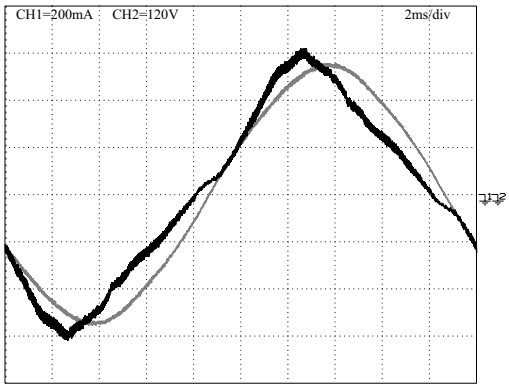

Fig. 12. Input current (black) and input voltage (gray) waveforms **with** snubber, controller designed for CCM

is not sinusoidal anymore, as the switch output capacitance changes drastically in this range. The period where the switch voltage is clamped to zero, is also observed in Fig. 8.

In Figs. 9 and 10, the detailed input current waveforms are depicted for the converter without snubber and with snubber respectively. While in the current in Fig. 9 fast changes are observed, the input current in Fig. 10 exhibits only very slow changes. For the influence of these oscillations on the averaged input current waveforms, three different experiments are performed. For the first experiment the regular CCM input current controller is used. As the gain of the duty-ratio-to-input-current in DCM is much lower than the gain in CCM, the total loop gain is low, so the controller is too slow to correct the input current oscillation. The resulting waveform is shown in Fig. 11, displaying bulges where the on-time of the switch starts with a positive input current and dips where the on-time starts with a negative input current. In Fig. 12 the experiment is repeated for a converter with snubber. The waveform is now smooth, although it is still not sinusoidal, due to the low gain of the control loop. Therefore, the control parameters are adapted to DCM operation. When no snubber is applied, the loop becomes instable as the total loop gain is now higher (Fig. 13). The input current now jumps from the top of the input current oscillation to the lowest point and back in only few switching cycles. The waveform for the converter with snubber (Fig. 14), is nearly sinusoidal.

A final experiment was done to find the influence for control algorithms where no input current controller is employed in DCM, such as voltage follower operation [3]. When assuming a large output capacitor, the output voltage can be assumed to be nearly constant and the output voltage controller will maintain a constant duty-ratio when operating at constant output power. Nevertheless, an important amount of input current distortion is observed in Fig. 15, as the instantaneous input current at the beginning of the on-time of the switch is varying periodically with the input voltage. Fig. 16 shows that here again the use of a simple snubber can solve the problem.

VI. CONCLUSION

When power factor correction converters designed for operation in the continuous conduction mode, are operated at reduced load, discontinuous conduction mode will appear during part of the line cycle or even the entire line cycle. As these converters are designed for CCM operation, they often use an averaged input current controller. Due to the parasitic capacitances of both the switch and the diode, the input

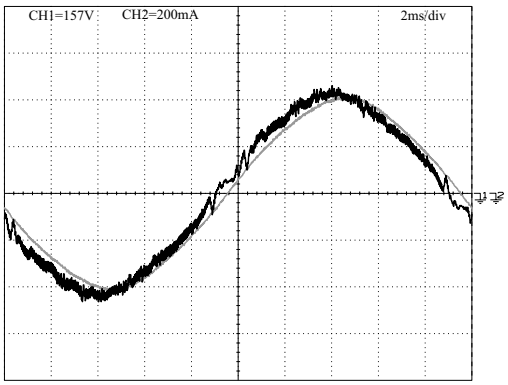

Fig. 13. Input current (black) and input voltage (gray) waveforms **without** snubber, controller designed for DCM

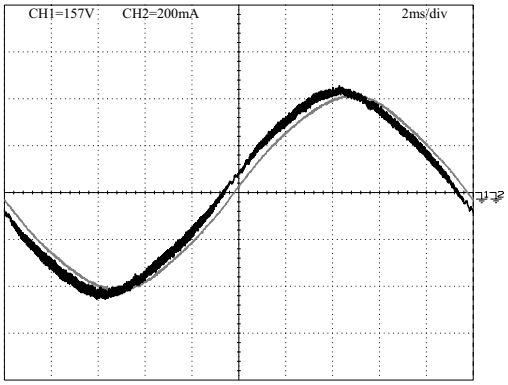

Fig. 14. Input current (black) and input voltage (gray) waveforms **with** snubber, controller designed for DCM

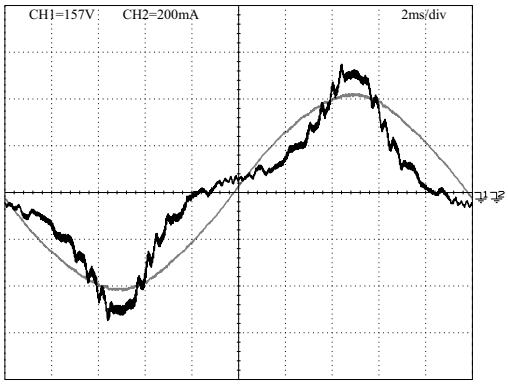

Fig. 15. Input current (black) and input voltage (gray) waveforms **without** snubber, constant duty-ratio

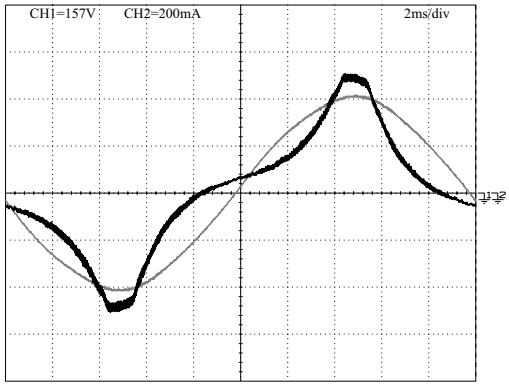

Fig. 16. Input current (black) and input voltage (gray) waveforms **with** snubber, constant duty-ratio

current waveform in DCM is distorted, yielding input current distortion when averaged input current control is applied. This source of input current distortion was analyzed in this paper and experimental waveforms were shown to confirm this analysis. As possible solution, the use of a snubber, consisting of a resistance and a capacitor, has been proposed. Experimental results have demonstrated the usefulness of this snubber, as the input current distortion was decreased substantially.

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