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ParaFPGA 2011 - High Performance Computing with Multiple FPGAs: Design, Methodology and Applications

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Abstract. ParaFPGA 2011 marks the third mini-symposium devoted to the methodology, design and implementation of parallel applications using FPGAs. The focus of the contributions is mainly on organizing parallel applications in multiple FPGAs. This includes experiences from building a supercomputer with FPGAs, automatic and dedicated balancing of different tasks on heterogeneous FPGA constellations and designing optimal interconnects between collaborating FPGAs.

Keywords: multiple FPGAs, load balancing, dynamic reconfiguration, parallel processing

Introduction

FPGAs are on the rise in high-performance computing. In recent years, their configurability, flexibility and compute capabilities have thoroughly increased, while these devices maintain a low-power profile. This makes multi-FPGA systems quite attractive for high-performance, highly parallel and green computing. Since 2007, the mini-symposium ParaFPGA attracts contributions which demonstrate use of FPGAs as parallel computing blocks either in a stand-alone system or as accelerator in an HPC environment.

The first mini-symposium [1] was mainly oriented towards mapping compute intensive and real-time applications onto FPGAs. Many aspects of the reconfigurability and the generation of massive parallel operations were demonstrated in seven different applications.

The second mini-symposium [2] juxtaposed FPGAs and GPUs. In particular, the flexibility of the hardware allowed to extract more parallelism in applications which are not embarrassingly parallel.

In this third edition of the mini-symposium ParaFPGA, the focus has shifted from parallel processing within an FPGA to parallel computing with multiple FPGAs, arranged in a cluster, grid, star or 3-D torus network. The added performance comes at a price of increased communication, load balancing and resource allocation.

1. Contributions

In *A Framework for Self-Adaptive Collaborative Computing on Reconfigurable Platforms* [3], different accelerator cores on three identical FPGAs are dynamically combined to solve a computationally intensive problem. The system is able to reconfigure itself when resources are removed or when more powerful components appear. The architecture consists of three FPGAs running embedded Linux in a switched Gigabit Ethernet network. The boards communicate using a lightweight to TCP/IP-based message protocol. A case study on the design of adaptive least mean square filters demonstrates the feasibility of the approach, its advantages and limitations.

In *Accelerating HMMER Search Using FPGA Grid* [4], four PCs equipped with an FPGA board are placed into a grid and communicate using the GLOBUS toolkit over a gigabit network. The FPGAs have two different sizes and fabrics. The system is used to accelerate profile HMM (Hidden Markov Model) searches of biological sequence databases. Two types of parallelism are exploited: 1) the profile HMM is compared with N different sequences simultaneously and 2) the search space of the Viterbi algorithm is explored in parallel. A more than hundredfold speed up is obtained compared to a CPU execution. In addition, the workload is tuned for maximum speed up by balancing the load taking into account the transfer delay and FPGA capabilities.

The Center for High-Performance Reconfigurable Computing at the University of North Carolina, Charlotte, has built a parallel computer with 64 FPGAs interconnected by a 3-D torus network. Spirit, the result of a five-year project, uses MPI message passing over a dedicated AIREN network to interconnect the on- and off-chip nodes. In the paper *Reconfigurable Computing Cluster* [5] an overview is given of the hardware and software architecture, design effort, system resilience and lessons learned.

Multi-FPGAs communicate use a dedicated interconnection framework. In *From mono-FPGA to multi-FPGA emulation platform for NoC performance evaluations* [6] a system is presented to generate, explore and validate arbitrary Network on Chip designs. Starting from a high level description of the topology, communication channels and link types, a synthesizable VHDL code of the interconnection network is generated. The performance of the emulated platform takes into account the resource allocation, number of communication channels and timing constraints. Different alternative NoCs are tested using embedded traffic generators.

Fast dynamic reconfiguration is the topic of the paper *A Dynamically Reconfigurable Pattern Matcher for Regular Expressions on FPGA* [7]. The idea is to reconfigure the FPGA for allowing different implementations depending on the changing parameters of a set of basic blocks. The generation of the parameterizable configurations as well as the dynamic calculation and programming of the parameters is discussed. Using this method, the specialization of an FPGA can be modified in the order of microseconds.

2. Conclusion

ParaFPGA 2011 introduced new ways to manage multiple FPGAs and to improve the reconfiguration techniques.

The versatility and increasing capabilities of these logic circuits will maintain and strengthen FPGAs as key contenders in the world of parallel computing accelerators.

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