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# Design of an integrated analog controller for a Class-D Audio Amplifier

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***Abstract*—An integrated analog controller for a self-oscillating class-D audio power amplifier is designed in a 0.35 $\mu$m CMOS technology for a 3.3 Volt power supply. It is intended to be used with an external output stage and passive filter, for medium power applications of upto a few 100 Watts. The controller was optimized with regard to its loop gain to suppress the distortion of the output stage. In typical commercially available output stages, the distortion is dominated by dead time effects and the THD can be as low as 20 dB.**

**The controller uses self-oscillation to generate the carrier. To control the self-oscillation a second order phase shift network is embedded in the loop. To increase the loop gain a fifth-order loop filter is added. For a switching frequency of 400kHz the controller achieves a loop gain of 51 dB, nearly flat over the audio band. For reasons of flexibility, the order of the controller is made programmable, as well as the dead time and the delay in the loop. Full spice simulations of the controller combined with an external 120 Watt output stage indicate that a THD of upto 80 dB (better than 0.01%) can be obtained even under the worst case condition of a dead time of 50 ns.**

***Index Terms*—Class D amplifier, dead-time distortion, self-oscillating, CMOS design**

## I. Introduction

CLASS-D audio amplifiers are known to be very efficient. This is because the power transistors are used as switches, which in theory implies that there are no Joule losses. This way power efficiencies well above 90 % can easily be achieved [1], [2]. Figure 1 depicts a quite general topology of such a class-D audio amplifier with analog control. The structure consists of a linear loop filter $H_{loop}$ and a comparator, which decides the digital code $D$ based on the loop filter output. This digital code $D$ controls which of the transistors in the output power stage is on or off. As a result the output voltage $V_{out}$ of the output stage is a pseudo-digital signal: either high ($V_{CC}$) or low ($-V_{CC}$). Then an output filter is used to reconstruct the actual output signal $V_{load}$ at the load. In practice the output filter is a second order passive, lossless LC-network serving two purposes: (a) recovery of the audio information by attenuating the switching residual, thereby (b) reducing EMI and losses. The figure shows a single-ended power stage (so-called half bridge) which consists of the power transistors $M_1$ and $M_2$, but also fully differential (full H-bridge) output stages are commonly used. The full H-bridge structure has advantages in terms of EMI and maximum power, but requires 4 power transistors.

In this work the focus is on the design of an integrated circuit for the analog controller for a class-D amplifier. The power

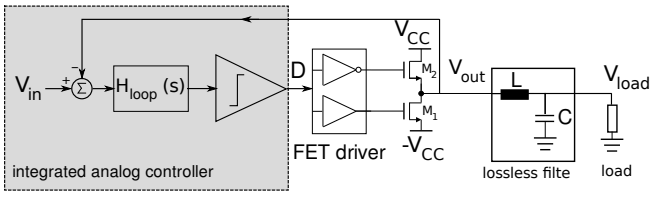


Fig. 1. Topology of a Class-D audio amplifier with analog control.

transistors, as well as the FET drivers are external circuits. This has the advantage that the same controller can easily be used for different power stages, operating at different power levels. In order to be compatible with typical commercially available power transistors the switching frequency is chosen to be 400 kHz.

One of the most important aspects in the design of the controller is the choice of the modulation scheme. In this work we use a controlled self-oscillation to generate the switching signal. The overall controller is optimized to achieve a high loop gain over the overall audio band. This is needed to reduce the non-idealities (distortion) in the output stage. The main non-ideality is so-called dead-time distortion.

## II. Design Of The Controller For The Phase Shift Based Self-Oscillating Amplifier

### A. Dead time distortion

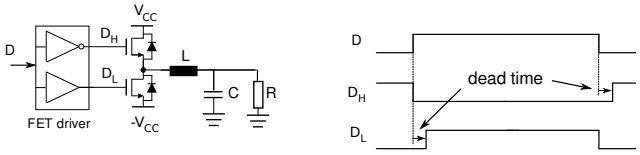


Fig. 2. Output stage and its appropriate drive signals.

In theory, both switch transistors $M_1$ and $M_2$ switch perfectly synchronously, but in practice the switching event takes some time. Since it must be guaranteed in all cases that both power transistors are not simultaneously on, a dead time interval is inserted between the turn-on of both control signals $D_H$ and $D_L$ of the switching stage as shown in figure 2. This way there is a limited time that both output transistors are off. To guarantee that the output current through the inductor in the output filter can also flow during this dead time, diodes are

added in parallel to the power transistors. It is well known that this dead time introduces odd order distortion [3]. Of course, this distortion increases with increasing dead time, but it is also function of the carrier frequency, cut-off frequency and Q-factor of the output filter. Typical combinations of commercially available FET-drivers [4] and power transistors [5] require a dead time of a few tens of nanoseconds. Therefore, we decided that the design should be able to deal with dead times of upto 50 ns.

Based on the analysis described in [3] the dead time distortion can be calculated. When the output LC-filter is sized for a cut-off frequency of 30 kHz, for a dead time of 50 ns, a carrier frequency of 400 kHz, the THD amounts to around $10\%$ (20 dB) for small signal levels, going down at higher levels. The design objective is to reach distortion levels close to $0.01\%$ (80 dB) for an as broad as possible power and frequency range. Using negative feedback to reduce non-linearities, we thus aim for an as high as possible loop gain for audio signals.

To discuss the further design of the loopfilter we will now conceptually merge the comparator and the output stage and neglect this effect, although it should be understood that this effect is the reason why a high loop gain is needed. For notational simplicity we will further normalize the power supply $\pm V_{CC}$ to $\pm 1$ without loss of generality.

### *B. Self-oscillation*

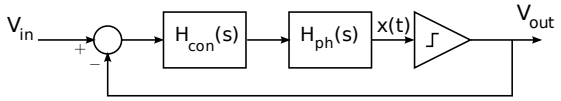


Fig. 3. Basic Topology of our self-oscillating Class-D amplifier.

In a self-oscillating structure the output voltage $V_{out}$ consists of a high-frequency square wave (in our case of the order of 400 kHz) of which the duty cycle is modulated in such a way that the low-frequency component of $V_{out}$ corresponds to the low-frequency audio signal $V_{in}$. The high frequency oscillation occurs at the frequency were the overall loop filter $H_{loop}$ has an $180^\circ$ phase shift. It is important that this oscillation frequency is accurately controlled. However the design of the loop-filter obviously both influences the loop gain as well as the oscillation frequency. This way, it is not obvious how such a loop filter should be designed. In our work this is achieved by splitting the loop filter in a phase shift filter $H_{ph}$ and an actual control filter $H_{con}$. The phase shift filter does not contribute to the loop gain, instead its only task is to accurately set the oscillation frequency. For this phase shift filter, a cascade of 2 passive poles is used, with the following transfer function:

$$H_{ph}(s) = \frac{1}{\left(\frac{s}{\omega_{ph}} + 1\right)^2} \tag{1}$$

To make the point, we will first assume that the actual control filter $H_{con}$ is an integrator $H_{con}(s) = \frac{1}{s\tau}$. Then the integrator gives a $90^\circ$ phase shift and the phase shift filter gives an additional $90^\circ$ phase shift at the frequency corresponding to $\omega_{ph}$. As a result the oscillation frequency $f_C = \frac{\omega_C}{2\pi}$ will equal $f_{ph} = \frac{\omega_{ph}}{2\pi}$, which can be accurately controlled.

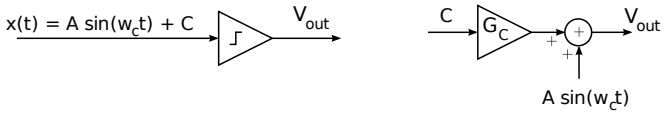


Fig. 4. Linearized model of the comparator valid for the low-frequency signals.

Once we have a controlled self-oscillation, we can build an approximately equivalent linear model of the loop by using describing function theory [6]. The concept is illustrated in figure 4. We start from observing that the signal $x(t)$ in front of the comparator consists of a contribution of the low-frequency audio-input signal and a high frequency oscillation which is caused by the self-oscillation. The audio signal is approximated by a constant $C$, which is justified because it is at a relatively low-frequency. The self-oscillation component is approximated by its first harmonic, which has an amplitude $A$ (which will be calculated later). Then we can calculate the best fitting value for the low-frequency gain $G_C$ leading to the model shown in figure 4. This best fit gain depends on the amplitude $A$ of the carrier and can be approximated as [6]:

$$G_C = \frac{2}{\pi A}$$

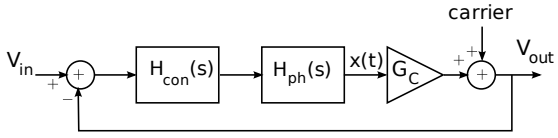


Fig. 5. Overall linear model of the self-oscillating class-D amplifier

This way we obtain the loop gain for the audio signals as the product $H_{con}H_{ph}G_C$. To evaluate this we should evaluate the amplitude $A$ of the first harmonic of the self-oscillation. The self-oscillation component in the output signal $V_{out}$ is essentially a square wave with a frequency $f_c = \frac{\omega_{ph}}{2\pi}$. The amplitude of its fundamental is $4/\pi$. When this signal passes through the cascade of the filter $H_{con}$ and $H_{ph}$ it has the following amplitude:

$$A = \frac{2}{\pi\tau\omega_{ph}}$$

This way we obtain the overall loop gain as:

$$\text{loop gain} = \frac{\omega_{ph}}{s\left(\frac{s}{\omega_{ph}} + 1\right)^2} \tag{2}$$

It is worth mentioning that the integrator time constant $\tau$ is not present in this expression and hence also does not affect the audio-performance. Since $\omega_{ph}$ corresponds to 400 kHz, the loop gain at 20 kHz is approximately 26dB, which is obviously not sufficient. Hence the order of the controller was increased to achieve better performance.

### C. Actual control filter design

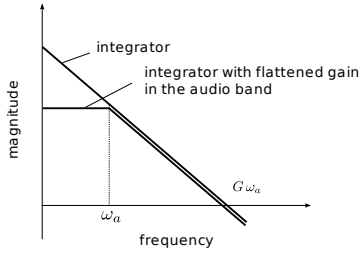


Fig. 6. Flattening the controller loop gain over the audio band

Above an integrator was used for the filter $H_1(s)$. This way the loop gain and hence also the THD increases for lower frequencies. However, audiophile sources suggest that such a behaviour of the THD gives a worse audio experience than a flat THD over the audio band [7]. For this reason the integrator gain was flattened over the audio band and the integrator was replaced by a transfer function with a passive pole:

$$\frac{1}{s\tau} \longrightarrow \frac{G}{1+\frac{s}{\omega_A}} = GT(s)$$

where $\omega_A$ corresponds to the audio band edge frequency of 20kHz and the transfer function $T(s) = \frac{1}{1+\frac{s}{\omega_A}}$. This is also illustrated in figure 6.

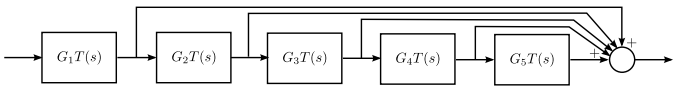


Fig. 7. Overall topology of the filter $H_{con}$

To improve the overall performance a higher order filter was used. Here a classical topology with cascaded sections $G_iT(s)$ and feedforward branches was used as shown in figure 7. Now, the design problem is to choose appropriate values for the gain coefficients $G_i$. This is non-trivial due to several complications. First, each gain section has its effect on the self-oscillation frequency, which was intended to be fixed at 400 kHz. Second, each gain section also has its effect on the audio band comparator gain $G_C$ as explained above. Therefore here an iterative process was set up where the order of the filter $H_{con}$ was increased by adding sections $G_iT(s)$. In the first step a first-order filter is designed with only one filter section $G_1T(s)$. As explained above the actual value of $G_1$ does not affect the overall audio band loop gain. Hence $G_1$ was arbitrarily assigned a value which sets the signal level at the comparator input to an acceptable level. Then a second stage $G_2T(s)$ is added to this first-order filter. After this, $G_2$ was chosen such that the loop gain was maximized, without significantly altering the self-oscillation frequency. Then this process is repeated to obtain the next $G_i$ values.

At each iteration step the gain $G_i$ was numerically optimized to obtain the highest loop gain. In a similar way as explained above, the theory of describing functions is used during the design to predict oscillating limit cycles and low frequency loop gain. This process was iterated upto a 5th order controller and resulted in the following coefficient values:

$$G_5 = 3, G_4 = 0.2, G_3 = 10, G_2 = 1, G_1 = 30.$$

Obviously, it is not guaranteed that this design procedure returns the optimum coefficient values, but it has the advantage that it is quite straightforward. The corresponding bode plots of the overall loop gain, including the best fit comparator gain (calculated with describing function theory) are shown in figure 8. Here we see that the first-order design achieves an audio band loop gain of 26 dB, the 3rd order design a loop gain of 39 dB and the 5th order design a loop gain of 51 dB. In all cases, the loop gain is almost constant over the audio bandwidth.

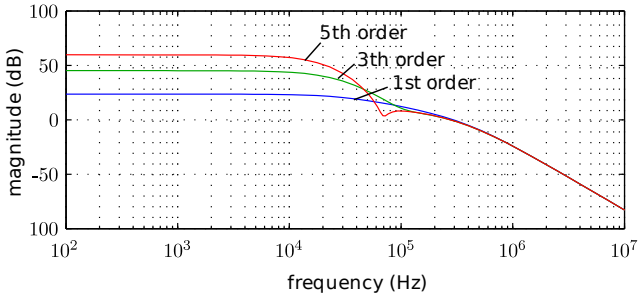


Fig. 8. Loop gain of the analog controller for various orders of the actual control filter $H_{con}$.

## III. Circuit-level design

The analog circuits for the controller were designed in a 0.35$\mu$m CMOS process from AMS. All circuits were implemented for a power supply voltage of 3.3 V. A quite straightforward implementation with active RC circuits was used, as shown in figure 9. The figure shows a single-ended version, but in reality all the circuits are fully differential.

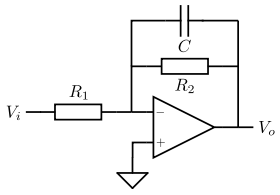


Fig. 9. Basic filter section

A single opamp is designed for all filter sections and the phase shifter filter, see figure 10. Because of the resistive load

a two-stage design is used. It has a folded-cascode first stage and a common source second stage. A modest gain-bandwidth product of 50 MHz is sufficient, as this is a low-speed design. Fig. 3 shows the two-stage folded cascode opamp. The opamp is compensated using the Ahuja-technique. This eliminates the zero in the RHS plane in a conventional Miller compensated design, but introduces a zero in the LHS plane. To place the zero beyond the unity gain frequency, the current in the secondary branch is chosen higher than in the primary branch of the cascode. No attempt was done to power optimize this circuit, which drains approximately 0.7 mA.

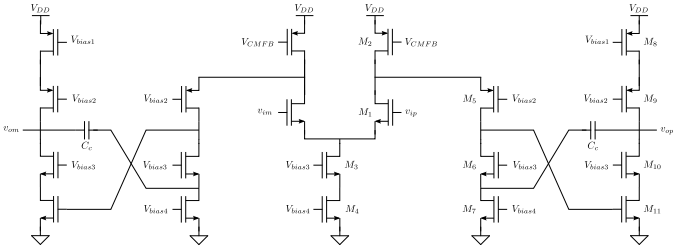


Fig. 10. Schematic of the operational amplifier design.

The comparator was designed in a quite conventional way as well and consists of three stages: a preamp, a decision circuit and an output buffer. The decision circuit utilizes positive feedback to quickly determine an output state, while the buffer converts its input signal to a logic level [8].

To allow for experimentation, a programmable dead time generation circuit is included, in addition to a digital variable-delay line. More delay adds more phase lag to the loop, lowering the frequency of oscillation. Also the phase shift filter is made programmable. This way some experimentation with regard to the oscillation frequency is possible. A digital interface is included and uses a simple three-wire protocol.

At normal operation the overall power consumption of the controller is approximately 20 mW which is negligeable compared to the other power levels in this application.

## IV. Simulation results

To investigate the performance of our circuit, full transistor level simulations were performed. Here an analog model of the off-chip output stage transistors and gate drivers was used. In the simulations a 400 kHz carrier frequency was ursed. The output LC filter was sized with butterworth poles for an 8Ω load and a cut-off frequency of 30kHz. The power supply of the output stage was taken $V_{CC} = 48\ V$. The worst case of an output stage that would require a 50 ns dead time, was considered. Figure 11 shows the resulting THD+N figures. The results are shown for the case of a 1 kHz and 6 kHz audio signal. The main harmonic due to dead-time distortion is the third which is located at 3 kHz and 18 kHz respectively. Due to the flat audio band loop gain, the curves for both frequencies do not differ much. The theoretical performance where the THD due to dead-time distortion is calculated according to [3] and divided by the loop gain is shown as well in the figure. It is clear that there is a reasonable match for signal levels where dead time distortion is the limiting factor. The target performance of 0.01% is obtained for most output power levels (only not for a signal level around 1 Watt). At lower output levels simulation noise due to the finite precision of the simulator limits the simulated THD+N figure.

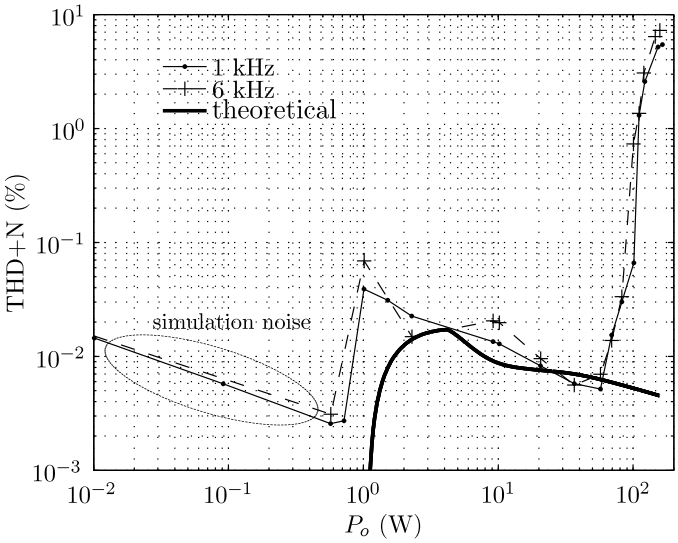


Fig. 11. THD+N simulation results of the analog controller for the case of an output stage that requires a dead time of 50 ns.

Many more simulations were performed, especially with varying dead time and as expected it was found that the performance of the controller dramatically improves by reducing the dead time. Therefore, the performance of any actual realization would require that the dead time is set to the lowest tolerable value allowed by the power stage.

## V. Conclusion

A programmable controller chip for a phase shift based self oscillation class D audio amplifier is designed. The controller uses a negative feedback loop to attenuate non-linear behaviour, mainly introduced by dead time in the switching stage. Here a 5th order control is used for optimal performance. Transistor level simulations indicate that upto 80dB THD performance can be otained, even in the worst case condition of 50 ns dead time.

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