Hybride monolithische integratie van hoogvermogen-DC-DC-convertoren in een hoogspanningstechnologie

Hybrid Monolithic Integration of High-Power DC-DC Converters in a High-Voltage Technology

Jindrich Windels

Promotoren: prof. dr. ir. J. Doutreloigne, dr. ir. A. Monté
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Universiteit Gent
Faculteit Ingenieurswetenschappen en Architectuur
Vakgroep Elektronica en Informatiesystemen
Centre for Microsystems Technology (CMST)
Technologiepark 914A
B-9052 Zwijnaarde, België
Tel.: +32-9-264 53 50
Fax.: +32-9-264 53 74

Promotoren:	Prof. Dr. ir. Jan Doutreloigne Dr. ir. Ann Monté
Examencommissie:	Prof. Dr. ir. Hendrik Van Landeghem - Voorzitter Dr. ir. Herbert De Pauw - Secretaris Prof. Dr. ir. Johan Bauwelinck Prof. Dr. ir. Marnix Botte Prof. Dr. ir. Johan Driesen ir. Edmond Op de Beeck

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List of Acronyms

AC	Alternating Current
ASIC	Application Specific Integrated Circuit
BT	Bipolar Transistor
CR	Conversion Ratio
C-W	Cockcroft-Walton
DC	Direct Current
DCR	Direct Current Resistance
DTI	Deep Trench Isolation
EN/UVLO	Enable/Undervoltage-Lockout
ESR	Equivalent Series Resistance
FIB	Focused Ion Beam
GaN	GalliumNitride
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
I/Os	Inputs/Outputs
IP	Intellectual Property
LCD	Liquid Crystal Display
LDO	Low-dropout

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MIMC	Metal Insulator Metal Capacitor
PCB	Printed Circuit Board
PFC	Power Factor Correction
POL	Point Of Load
PWM	Pulse Width Modulation
RCD	Resistor, Capacitor, and Diode
RESURF	Reduced Surface Field
SiC	SiliconCarbide
SOI	Silicon On Insulator
SR	Synchronous Rectifier

Samenvatting

Elektrische energie is niet meer weg te denken uit het dagelijkse leven, zowel thuis, in ondernemingen als in de industrie. Hoewel bijna alle elektronische applicaties steeds efficiënter worden, blijft de wereldwijde vraag naar energie steeds toenemen, aangezien het aantal gebruikers en applicaties sneller stijgt dan de technologische vooruitgang kan compenseren. Teneinde de totale productie van energie toch haalbaar en betaalbaar te houden, is het essentieel dat de distributie van de geproduceerde elektrische energie zo efficiënt mogelijk gebeurt, of met andere woorden dat de verliezen in de distributie zoveel mogelijk beperkt worden. Door het transport van elektrische energie op de hoogst mogelijke veilige spanning uit te voeren blijven de stromen en de daarmee samenhangende Joule-verliezen beperkt. Om het totale rendement te optimaliseren dient de spanning zo dicht mogelijk bij de eindgebruiker omgezet te worden naar een geschikte lagere spanning, en deze omzetting dient uiteraard ook zo efficiënt, goedkoop en compact mogelijk te gebeuren.

Dankzij een doorgedreven integratie van elektronische systemen, waarbij steeds meer functionaliteit gecombineerd wordt in monolitisch geïntegreerde circuits, kan de kostprijs, het vermogenverbruik en het formaat van deze elektronische systemen sterk beperkt worden. Deze doorgedreven integratie van elektronische systemen is niet beperkt tot de eindgebruikers van de elektrische energie, maar kan ook toegepast worden op de spanningsomzetting. De spanningsomzetting is in de meeste hedendaagse applicaties een efficiënte, schakelende DC-DC-convertor, waarbij energie tijdelijk in een of meerdere reactieve elementen, zoals spoelen en condensatoren, wordt opgeslagen. Hierbij laat een hoge schakelsnelheid toe om de DC-DC-converter compact te houden.

Voor lage vermogens, typisch minder dan 1 Watt, is het mogelijk om deze spanningsomzetting volledig monolitisch te integreren. In sommige gevallen kan dit zelfs samen met het geïntegreerde elektronische circuit dat de eindgebruiker is van de energie, om zo een systeem met minimale afmetingen te realizeren. Voor hogere vermogens voldoen de volledig monolitisch geïntegreerde componenten niet om de gewenste efficiëntie te bereiken en blijken een aantal externe componenten noodzakelijk. Doorgaans zijn de reactieve componenten de meest beperkende factor en worden deze bij stijgende vermogens als eerste buiten het geïntegreerde circuit gebracht. Halfgeleidercomponenten, inclusief de vermogenstransistoren blijven daarentegen deel uitmaken van het geïntegreerde circuit, om zo een hybride geïntegreerde convertor te bekomen. Dankzij deze hybride aanpak is het in de huidige hybride geïntegreerde convertor-toepassingen haalbaar om maximaal ongeveer 60 Watt te verwerken, zij het enkel voor spanningen tot een paar Volt. Voor spanningen

van enkele tientallen Volt is het uitgangsvermogen van deze hybride geïntegreerde convertoren beperkt tot een tiental Watt. Voor nog hogere vermogens worden de geïntegreerde vermogenstransistoren eveneens een beperkende factor en worden deze vervangen door discrete vermogenstransistoren. In deze discrete convertoren is de omzetting van veel hogere vermogens mogelijk, maar de omvang van het systeem neemt snel toe. In dit werk worden de grenzen van de hybride aanpak onderzocht bij het gebruiken van zogenaamde *smart-power* technologieën, een generieke term voor betaalbare sub-micron CMOS technologieën met enkele uitbreidingen voor de integratie van hoogspanningscomponenten. Afhankelijk van de applicatie is het mogelijk om beter te presteren dan de huidige "beste" convertoren op het gebied van efficiëntie, formaat en kostprijs, door het combineren van de gepaste smart-power technologie en de juiste topologie.

Voor het bepalen van de mogelijkheden van smart-power DC-DC-convertoren worden eerst algemeen de belangrijkste parameters besproken voor een efficiënte energiedistributie en bekijken we de rol die spanningsomzetting speelt in de energiedistributie. Aansluitend kiezen we uit de mogelijke toepassingen een tweetal applicaties uit de wereld van de telecommunicatie waarvoor we de hybride monolitische integratie in een smart-power technologie wensen te optimaliseren. Daarna bekijken we de eigenschappen van een ideale convertor en de relevante specifieke kenmerken van de betaalbare smart-power technologieën voor de implementatie van DC-DC-convertoren. Rekening houdend met de beperkingen die aanwezig zijn in deze technologieën bepalen we een kostfunctie die toelaat om systematisch de verschillende topologieën voor convertoren te kunnen vergelijken zonder het volledige ontwerpproces te doorlopen. Vanuit deze kostfunctie valt het op dat de de facto standaard keuze voor de topologie in discrete convertoren, die gebasseerd is op het uitgangsvermogen, niet optimaal is voor convertoren met geïntegreerde vermogenstransistoren. Op basis van deze kostfunctie en de randvoorwaarden die gesteld worden aan onze concrete applicaties bepalen we de optimale topologie voor een smart-power implementatie voor de eerder gekozen applicaties.

Vervolgens gaan we een stap dichter bij de realiteit en bekijken we de gevolgen van parasitaire elementen in een smart-power implementatie van schakelende convertoren. De spanningspieken veroorzaakt door de lekinductantie aan de secundaire van transformatorgeïsoleerde convertoren blijken daarbij een groot struikelblok voor een efficiënte implementatie. Aangezien de gebruikelijke aanpak van deze spanningspieken in discrete convertoren niet voldoet voor smart-power convertoren omwille van technologische beperkingen wordt een alternatieve aanpak aangetoond en geïmplementeerd, waarbij de energie uit de spanningspieken wordt geabsorbeerd en hierbij gerecycleerd naar de uitgang van de convertor. Hierdoor is het mogelijk om de spanningspieken sterk te reduceren en tegelijk het rendement vrijwel constant te houden. Zo bekomen we een efficiënte, compacte en betaalbare implementatie. De correcte werking van deze aanpak werd uitgetest en aangetoond, zowel in een versie gebruik makend van een commercieel verkrijgbaar geïntegreerd circuit, als in een eigen smart-power implementatie.

Uiteindelijk bekijken we ook de optimalisatie van schakelende convertoren over de volledige lastkarakteristiek door de mogelijkheden van een sterk geïntegreerde convertor uit te buiten. Alhoewel het maximale uitgangsvermogen nog steeds een van de karakteristieke

eigenschappen is van een convertor blijkt dat de meeste convertoren een belangrijk deel van hun levensduur significant lagere vermogens omzetten. Hierdoor is het wenselijk om ook bij een lagere uitgangsstroom en uitgangsvermogen het rendement te optimaliseren. Door de vermogenstransistoren op te splitsen in verschillende onafhankelijke segmenten, die in functie van de stroom al dan niet aangestuurd worden, kan het rendement bij lage stromen sterk verhoogd worden. Dit alles zonder de introductie van ongewenste frequentiecomponenten in de uitgangsspanning en zonder dat dit ten koste gaat van het rendement bij hogere stromen. Deze eigenschappen laten toe om deze optimalisatietechniek in vrijwel alle applicaties van hybride monolithische DC-DC-convertoren toe te passen, zonder grote impact op de complexiteit en de kost van het systeem. Deze aanpak werd uitgetest en aangetoond in een versie met discrete vermogenstransistoren, maar kon wegens een probleem met een digitaal controleblok enkel in simulatie aangetoond worden voor de eigen smart-power implementatie.
Tenslotte worden eveneens een aantal algemene conclusies geformuleerd en halen we de mogelijkheden voor toekomstig werk in het verlengde van dit onderzoek aan.

Summary

The supply of electrical energy to home, commercial, and industrial users has become ubiquitous, and it is hard to imagine a world without the facilities provided by electrical energy. Despite the ever increasing efficiency of nearly every electrical application, the worldwide demand for electrical power continues to increase, since the number of users and applications more than compensates for these technological improvements. In order to maintain the affordability and feasibility of the total production, it is essential for the distribution of the produced electrical energy to be as efficient as possible. In other words the loss in the power distribution is to be minimized. By transporting electrical energy at the maximum safe voltage, the current in the conductors, and the associated conduction loss can remain as low as possible. In order to optimize the total efficiency, the high transportation voltage needs to be converted to the appropriate lower voltage as close as possible to the end user. Obviously, this conversion also needs to be as efficient, affordable, and compact as possible.

Because of the ever increasing integration of electronic systems, where more and more functionality is combined in monolithically integrated circuits, the cost, the power consumption, and the size of these electronic systems can be greatly reduced. This thorough integration is not limited to the electronic systems that are the end users of the electrical energy, but can also be applied to the power conversion itself. In most modern applications, the voltage conversion is implemented as a switching DC-DC converter, in which electrical energy is temporarily stored in reactive elements, i.e. inductors or capacitors. High switching speeds are used to allow for a compact and efficient implementation.

For low power levels, typically below 1 Watt, it is possible to monolithically implement the voltage conversion on an integrated circuit. In some cases, this is even done on the same integrated circuit that is the end user of the electrical energy to minimize the system dimensions. For higher power levels, it is no longer feasible to achieve the desired efficiency with monolithically integrated components, and some external components prove indispensable. Usually, the reactive components are the main limiting factor, and are the first components to be moved away from the integrated circuit for increasing power levels. The semiconductor components, including the power transistors, remain part of the integrated circuit. Using this hybrid approach, it is possible in modern converter-applications to process around 60 Watt, albeit limited to voltages of a few Volt. For hybrid integrated converters with an output voltage of tens of Volt, the power is limited to approximately 10 Watt. For even higher power levels, the integrated power transistors also become a limiting factor, and are replaced with discrete power devices. In these

discrete converters, greatly increased power levels become possible, although the system size rapidly increases. In this work, the limits of the hybrid approach are explored when using so-called *smart-power* technologies. Smart-power technologies are standard low-cost submicron CMOS technologies that are complemented with a number of integrated high-voltage devices. By using an appropriate combination of smart-power technologies and circuit topologies, it is possible to improve on the current state-of-the-art converters, by optimizing the size, the cost, and the efficiency.

To determine the limits of smart-power DC-DC converters, we first discuss the major contributing factors for an efficient energy distribution, and take a look at the role of voltage conversion in the energy distribution. Considering the limitations of the technologies and the potential application areas, we define two test-cases in the telecommunications sector for which we want to optimize the hybrid monolithic integration in a smart-power technology. Subsequently, we explore the specifications of an ideal converter, and the relevant properties of the affordable smart-power technologies for the implementation of DC-DC converters. Taking into account the limitations of these technologies, we define a cost function that allows to systematically evaluate the different potential converter topologies, without having to perform a full design cycle for each topology. From this cost function, we notice that the de facto default topology selection in discrete converters, which is typically based on output power, is not optimal for converters with integrated power transistors. Based on the cost function and the boundary conditions of our test-cases, we determine the optimal topology for a smart-power implementation of these applications.

Then, we take another step towards the real world and evaluate the influence of parasitic elements in a smart-power implementation of switching converters. It is noticed that the voltage overshoot caused by the transformer secondary side leakage inductance is a major roadblock for an efficient implementation. Since the usual approach to this voltage overshoot in discrete converters is not applicable in smart-power converters due to technological limitations, an alternative approach is shown and implemented. The energy from the voltage overshoot is absorbed and transferred to the output of the converter. This allows for a significant reduction in the voltage overshoot, while maintaining a high efficiency, leading to an efficient, compact, and low-cost implementation. The effectiveness of this approach was tested and demonstrated in both a version using a commercially available integrated circuit, and our own implementation in a smart-power integrated circuit.

Finally, we also take a look at the optimization of switching converters over the load range by exploiting the capabilities of highly integrated converters. Although the maximum output power remains one of the defining characteristics of converters, it has been shown that most converters spend a majority of their lifetime delivering significantly lower output power. Therefore, it is also desirable to optimize the efficiency of the converter at reduced output current and output power. By splitting the power transistors in multiple independent segments, which are turned on or off in function of the current, the efficiency at low currents can be significantly improved, without introducing undesirable frequency components in the output voltage, and without harming the efficiency at higher currents. These properties allow a near universal application of the optimization technique in hybrid monolithic DC-DC converter applications, without significant impact on the complexity

and the cost of the system. This approach for the optimization of switching converters over the load range was demonstrated using a boost converter with discrete power transistors. The demonstration of our smart-power implementation was limited to simulations due to an issue with a digital control block.
On a finishing note, we formulate the general conclusions and provide an outlook on potential future work based on this research.

1 Introduction

1.1 Introduction

The electrification of the world has been called the greatest engineering achievement of the 20th century, and if we see what can be achieved nowadays by merely flicking a switch this is no exaggeration. Since the end of the 19th century, when the first commercial implementations of electrical power plants began to distribute electrical energy to a region of customers, these customers have realized the advantages of using electrical energy for powering mechanical equipment, lighting, and heat sources, and the availability of electrical power has played a significant part in the development of the world as we know it today, with a notable highlight in the form of today's information technology. The ubiquitous nature of electrical energy in everyday life is mainly obvious when the electrical power distribution is temporarily interrupted, and everything we take for granted suddenly grinds to a halt.

Because of the multitude of applications in which electrical energy can be used, the worldwide hunger for electrical power has seen a steady increase ever since the beginning of the electrification. To make this possible at a reasonable cost, the efficiency of bringing electrical power from where it is generated to where it is used needs to be optimized as much as possible, which includes every aspect from generation over transportation to use of electrical energy.

The transportation of electrical energy is most efficient at high voltages and lower currents, while applications at the end of the line run at lower voltages, with a trend for electronic equipment to operate at ever decreasing voltages. This requires multiple conversions of energy from a high transportation voltage towards a lower utilization voltage.

To optimize the benefits of the high transportation voltage, this conversion also needs to be optimized in the aspects of size, cost, and efficiency, otherwise the gains in the distribution by using an increased voltage are lost again in the conversion.

Electrical energy conversion is an enormously broad field, ranging from gigawatt to nanowatt, so obviously there is no single solution that is optimal for all applications.

In this work we aim to optimize highly – but not fully – integrated converters, where most components, including the power transistors, are integrated on a single chip using affordable smart-power technologies, which are high-voltage extensions of standard semiconductor processes, but still allowing the use of discrete components when integrated components become impractical to integrate from a cost or performance perspective. Because of the integrated character and the associated limitations, these highly integrated converters are limited in power and voltage compared to converters that use discrete power devices. However, the voltage and power is at the high end of the capabilities of integrated technologies and we feel that hybrid monolithic integrated high-voltage high-power converters is an adequate description of the converters that we want to optimize. Even though in absolute numbers the individual gain in efficiency for an optimized relatively low-power converter is small, their large number implies that significant energy saving in the generation and distribution stage can be achieved by optimizing these converters.

First, we will show that voltage conversion is the key to efficient distribution of electrical energy, and that throughout the history of voltage conversion the increasing degree of integration of functionality in a single chip has been an enabling factor for affordable and widespread implementation of efficient converters. Nowadays, thanks to the smart-power technologies it is possible to implement all power devices and controlling logic on a single chip, and by allowing the use of some external components in a hybrid monolithic integrated converter, the power can be increased compared to fully integrated converters, where all components are on the chip.

To optimize these hybrid monolithic integrated high-voltage high-power converters, we first need to be familiar with the properties of the available high-voltage technologies and the impact this has on the potential applications. After this, we can select an optimal combination of application and converter topology, based on an estimation of the efficiency and the required silicon area.

Then, we see that – once we leave the idealized world of textbooks and basic simulations and enter the real world with non-ideal components – voltage overshoot on the secondary side of transformer-isolated converters is a major roadblock for efficient smart-power implementation. To minimize the effects of the secondary side voltage overshoot, we show a new and highly integrated approach that can arbitrarily reduce the overshoot while maintaining a high efficiency, which is not possible using the conventional approach known from discrete converters.

Finally, we take a closer look at how the efficiency of the hybrid integrated power converters over the load range can be optimized by taking advantage of the properties of integrated converters.

1.2 Outline

In the Introduction chapter, which you are reading right now, a short and abstract background to the work is sketched, followed by the outline of the work. Then we briefly highlight the research context, and give an overview of the dissemination that has resulted from the research.

In Chapter 2, a more in depth introduction to efficient energy distribution and the potential applications of hybrid monolithic integrated converters is discussed. Additionally, we select two converter specifications for telecommunications applications as a reference case for hybrid monolithic integrated converters, based on the properties of the available smart-power technologies, the specifications of these converters, and the global relevance of the applications.

In Chapter 3, we begin our search for an a optimal converter topology for integration in affordable smart-power technologies, starting form the definition of an ideal converter, introducing some semiconductor device basics and the relevant properties for smart-power technologies. Then we define a cost function for the monolithic integration of converters in these smart-power technologies and discuss the advantages and disadvantages of several approaches for voltage conversion. To end Chapter 3, we conclude on an optimum converter topology for hybrid monolithic integration of high-power converters in a high-voltage technology.

In Chapter 4, we introduce some parasitic elements in the converters that were not relevant in the discussion of the relative merits of different topologies for integration in a smart-power technology from the previous chapter, but are very much relevant for an efficient implementation of a smart-power converter. We will find out that the voltage overshoot caused by the inductive parasitics in transformer-isolated converters is a major roadblock for an efficient smart-power implementation, and discuss the possibilities to reduce the impact of the voltage overshoot. This discussion leads to an asynchronous active voltage clamp approach, that is significantly different than is common in discrete converters at this power level. We show a discrete prototype confirming the potential benefits of this proposed clamping circuit, and highlight the relevant design aspects for a monolithic version that is integrated with the synchronous rectifier of a smart-power converter. Measurements on the clamping circuit confirm a reduced voltage stress, improved efficiency, and reduced size compared to dissipative clamping circuits, which are the common solution for converters at this power level.

In Chapter 5, we discuss the possibilities for optimizing the efficiency of hybrid monolithic integrated converters over the load range. We take a look at the loss mechanisms that are present in switching converters, and systematically discuss the impact on the efficiency over the load range for a number of modifications to the textbook converters. We see that an approach where the dimensions of the power devices are dynamically adjusted in function of the load based on a non-invasive current estimation is well suited for implementation in hybrid monolithic integrated converters. Therefore, this approach is discussed in more detail, followed by a proof of concept on a discrete implementation with measurements confirming the optimization of efficiency, and a discussion of

the design aspects for a monolithic implementation. Unfortunately, no measurements are available on this monolithic implementation, due to an issue with a digital control block.
In Chapter 6, we arrive at the conclusions, where the main achievements are highlighted and an outlook for future work is presented.

1.3 Research context

In modern times, the days of lone researchers working in a vacuum and emerging after a couple of years to present their work are long gone. Instead, researchers continue to build on the framework built by their predecessors and peers in order to advance the state-of-the-art. This work was situated at the CMST (Centre for Microsystems Technology), formerly known as *TFCG Microsystems Lab* in Zwijnaarde (Gent), a research group in the ELIS (Electronics and Information Systems) Department of the Faculty of Engineering and Architecture of Ghent University, and also an associated lab of imec. Under the lead of em. Prof. André Van Calster, CMST has grown from a small research group working on thin-film displays to a multidisciplinary research group working on smart microsystems integration, focusing on both design and technology in a number of domains: advanced packaging, stretchable interconnects, polymer structuring and microfluidics, optical interconnect and laser technology, display technology, and smart-power. This is a diverse range of domains, with target applications in ambient intelligence, telecom, energy, displays & lighting, and biomedical & health.
The research presented in this work is situated in the smart-power subgroup – specialized in the design of high-voltage integrated circuits – under the lead of Prof. Jan Doutreloigne. Originally, these high-voltage integrated circuits were used for driving thin-film displays, although through the years the applications have diversified to intelligent drivers for bistable, modular, and emissive displays, drivers and splitters for xDSL applications, TCAD simulations of power devices, switching converters for (O)LED applications and telecommunications, smart switches for PV applications, and design of MEMS devices and drivers. The research on telecommunications applications, including the switching converters, is in the framework of a bilateral research agreement with Alcatel-Lucent, a global manufacturer of telecommunications equipment.
This work was initially funded by Ghent University in the form of a *Dehousse* scholarship, followed by an IWT post-graduate *specialisatiebeurs* grant, and finalized as an imec payroll employee. Additional funding was provided by the bilateral research agreement with Alcatel-Lucent.

1.4 Research dissemination

1.4.1 Papers published in an SCI-journal

- **Jindrich Windels** and Jan Doutreloigne, "Active asynchronous secondary side voltage clamping", *Electronics Letters, IEE*, **2011**, 47, 512-514

1.4.2 Papers presented at international conferences listed as P1-publications

- Ann Monté, Jan Doutreloigne, **Jindrich Windels**, Pieter Bauwens, ”Driving electronics for OLED lighting”, SID-ME Spring 2013 Meeting. Ghent, Belgium, April 15-16, 2013
- Jan Doutreloigne, Ann Monté and **Jindrich Windels**, ”Design of an Integrated OLED Driver for a Modular Large-Area Lighting System”, 7th International Conference on Circuits, Systems and Signals (CSS ’13), Cambridge, MA, USA, January 30- Februari 1, 2013
- **Jindrich Windels**, Ann Monté and Jan Doutreloigne, ”Monolithic integration of an active asynchronous voltage clamp with a 12V3A full bridge synchronous rectifier”, Proceedings of the 2012 IEEE International conference on Power Electronics, Drives and Energy Systems (2012), Bengaluru, India, December 16-19, 2012
- Jan Doutreloigne, Ann Monté, Benoit Bakeroot and **Jindrich Windels**, ”Monolithic Integration of an Active Clamping H-Bridge for Isolated Forward DC-DC Converters”, Proceedings of the 11th WSEAS International Conference on Instrumentation, Measurements, Circuits and Systems (IMCAS’12), Rovaniemi, Finland, April 18-20, 2012
- Jan Doutreloigne, Benoit Bakeroot, Ann Monté and **Jindrich Windels**, ”Monolithic Integration of the Synchronous Rectifier in Isolated Forward DC-DC Converters”, Proceedings of the 11th WSEAS International Conference on Instrumentation, Measurements, Circuits and Systems (IMCAS’12), Rovaniemi, Finland, April 18-20, 2012
- **Jindrich Windels**, Christophe Van Praet, Herbert De Pauw and Jan Doutreloigne, ”Comparative study on the effects of PVT variations between a novel all-MOS current reference and alternative CMOS solutions” Midwest Symposium on Circuits and Systems Conference Proceedings (2009) , Cancun, Mexico, August 2-5, 2009

1.4.3 Papers presented at national conferences

- **Jindrich Windels**, Analysis and design of high power monolithically integrated switching DCDC converters, UGent-FirW Doctoraatssymposium, 11e (2010)

2

Enabling efficient energy distribution through voltage conversion

2.1 Introduction

In this chapter we will take a look at the design considerations for an energy efficient distribution network for electrical energy. Typically, energy distribution is considered as everything coming from the electrical power plant, where the electrical energy is converted from other energy sources to electricity, and ending at the industrial, commercial, or home user, which is billed for the energy consumption on-site. However, the same considerations for energy distribution are valid over an even wider range: coming from the power plant, over the billed customer down to individual systems, modules, and subsystems, the same design considerations are in effect for efficient energy distribution, only at a different scale, and therefore leading to different optimal solutions.

After discussing the underlying principles for efficient energy distribution, we will situate where our hybrid monolithic high-power converters are located in the distribution process of electrical energy and identify where our work can improve on the state-of-the-art. We will highlight a number of potential applications for a hybrid monolithic integrated high-voltage high-power DC-DC converter, and select two test-cases where we expect the advantages of hybrid monolithic integrated power converters using affordable high-voltage technologies will be the most relevant.

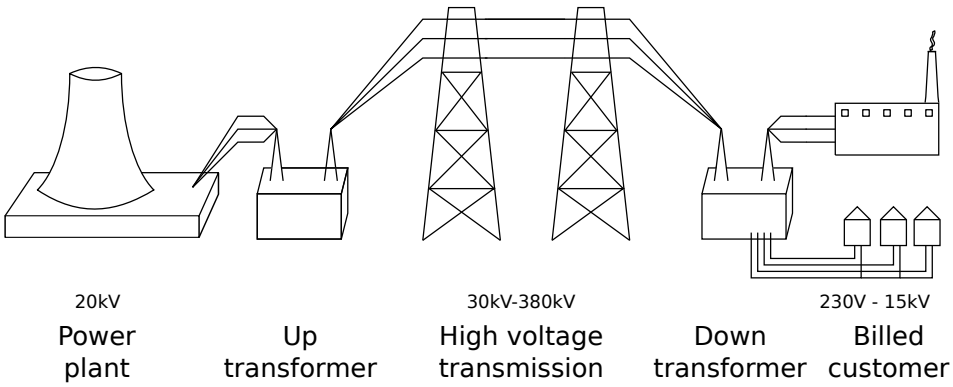

Figure 2.1: Schematic overview of a distribution network for electrical energy

2.2 Efficient energy distribution

In any energy distribution system, it is important to optimize the cost of the energy distribution and the efficiency of the energy distribution. Obviously, every Watt that is generated at the power plant has an associated cost, be it in fossil fuels, nuclear fuel mining and disposal, or simply the resources that are used in the construction of a renewable energy plant with a finite life time. Therefore, it is in the best interest of anyone involved in the generation and distribution of power to ensure the delivery to the end user is as optimal as possible, and reduce the losses to a minimum. A conflicting interest however is the cost of building and maintaining the distribution network, since the resistance of the conductors needs to be as low as possible to achieve low losses in the electrical distribution network. All good electrical conductors, such as copper and aluminum, that can transport large amounts of power without requiring excessive material and space are also finite resources, and can quickly become expensive if large currents need to be transported over large distances. It is estimated that worldwide in 2011 approximately 8 percent of all generated electrical energy was lost in transmission and distribution, i.e. between the power plant and the billed customer [1] [2].

Because electrical power is the product of current and voltage, it is possible to minimize the amount of required conductor material by performing the transport of electrical energy at the highest possible safe and practical voltage, thereby reducing the current through the conductor. Because of the quadratic dependence on current of the Joule loss in a conductor ($P = RI^2$), the loss in identical resistive conductors is reduced by a factor 4 with doubling the voltage, which reduces the current in half.

Regional voltages exist in voltages used for generation, transmission, distribution, and delivery to the end users. In Figure 2.1, a more-or-less typical distribution system is shown with the voltage ranges as used in Belgium [3]. Here, the Alternating Current (AC) voltage as generated by the power plant is converted using a transformer to a higher voltage, typically tens to hundreds of kV to optimize the distribution efficiency. For

safety reasons, these high-voltage lines are either placed overhead on pylons or buried underground. Near the end user, the voltage is transformed down again using another transformer to a voltage that is appropriate for the amount of power that the customer is using, for residential electrical installations and small scale commercial installations, this is typically 230 V, but can be increased for larger commercial and industrial customers up to tens of kV.

Ever since the beginning of the construction of the distribution network, an AC system running at a few tens of Hertz has been the most convenient way to distribute electrical energy. The choice for the mains frequency was a historical compromise between losses over long transmission lines, which increase with frequency, the properties of some rotating machines that do not operate well on high frequencies, and the size of transformers, that become smaller and lighter with increased frequency [4].

The use of AC leads to a less than optimal use of the conductor and isolation material. For the isolation material, this is caused by the peak voltages in AC being $\sqrt{2}$ times the nominal voltage, whereas in DC the nominal and peak voltage are identical. For the conductor material, this is caused by the skin effect in conductors carrying AC which reduces the effective conductor cross-section, and thus the need to use a somewhat larger conductor compared to DC for an identical equivalent resistance. However, the ability to use transformers to increase or decrease the voltage in a simple, relatively low-cost and efficient way has historically compensated for the less than perfect conductor utilization. Typically, only in specialty applications like underseas cables, very long interconnect distances, and to connect asynchronous AC networks, the additional cost of implementing a High Voltage DC (HVDC) distribution link is warranted [5].

However, the power distribution story is not limited to centralized production in a power plant with delivery of the electrical power to the end user, as only a limited number of appliances, such as heaters, electrical motors and incandescent lighting actually use the electrical energy at the voltage at which it is delivered by the distribution grid. Both applications where the electrical energy from the grid is used in other appliances inside the end user facility that operate at other voltages, and applications that are not necessarily connected to the distribution grid, such as battery-powered and battery-backed-up equipment need to be optimized for an efficient energy distribution to reduce the loss to a minimum.

Within the premises of the end user, the same considerations apply as in the distribution network, but at reduced power levels and typically also at reduced voltages to improve the safety when users of the electrical energy can come into proximity of live conductors.

Until relatively recently, almost all power conversion was performed with transformers operating at mains frequency, often followed by rectification and one or more linear regulators to provide a stable DC voltage. This classical approach leads to a bulky power supply, because of the use of physically large and heavy transformers and the need to provide adequate heat-sinking for the linear regulators but is simple and relatively low-cost.

2.3 The rise of the semiconductor

Ever since the first commercial release of an integrated circuit (IC) in 1960, when Texas Instruments announced their TI #502 multivibrator IC [6], the number of components on a single IC has increased exponentially. This trend was first described by Gordon E. Moore in 1965, when he predicted that by 1975 as many as 65000 components on a single chip would not only be possible, but would provide a minimum cost per component [7], based on the then-short history of the integrated circuit and a then-state-of-the art optimum of 50 components per IC. This prediction corresponded with a doubling of the number of transistors in an integrated circuit every 12 months, and when 1975 rolled around, Moore's prediction was confirmed. Based on the additional insights in the production process that were available ten years after his initial observation of the trend, he then revised his prediction to a doubling every 24 months [8],and his prediction of exponential growth has proven to be uncannily accurate until the present day. This is in part because his prediction became a self-fulfilling prophecy, considering it is used by the semiconductor industry to define their long term road-map, and the trend he observed in the 1960's is still referred to as Moore's law.

To achieve this increased density, the dimensions of semiconductor devices also decreased dramatically since the first integrated circuit. Because of the physical limitations in the materials used in the semiconductor manufacturing, such as maximum field strength in semiconductors and dielectrics, this increase in density has corresponded with ever decreasing supply voltages. Although the reduction in size and supply voltage results in a reduction in power consumption per transistor, the exponentially increasing number of transistors leads to an ever increasing current consumption for integrated circuits.

As we have seen in the previous section on efficient energy distribution, the losses in a system are minimized by transferring electrical energy at the maximum possible voltage at low currents, and reducing the voltage and increasing the current as close to the end user as possible. Although the scale in an electronic system composed of integrated circuits is significantly different from the distribution grid, where thousands of Ampere at hundreds of kV can be transported, the same principle still applies, as the conductor cross section is also much smaller.

With the increasing power demands of integrated circuits, the classic voltage conversion approach with transformers operating at the mains frequency followed by a linear regulator became increasingly impractical. Since this approach is limited by thermal considerations in the heat-sinks and transformers, the increasing power demands of the shrinking electronic systems imply increasingly large transformers and heat-sinks.

By 1947, when the first transistor was demonstrated in a laboratory setting [9], switching power supplies were already commercially available using electromechanical switches or *vibrators* operating at a few tens to a few hundred Hertz [10]. Because of the noise and mechanical wear associated with electromechanical switches, these switching power supplies were typically used in battery-powered applications requiring voltages in excess of the battery voltage. Since these electromechanical switching converters operated in the same frequency range as the electrical mains, the potential reduction in size

for the transformer by choosing an increased frequency was relatively limited. Together with the increasing use of semiconductor devices in analog and digital circuits, discrete semiconductor power devices that could be used as switches also became available, and switching power supplies operating at frequencies above the mains frequency gradually became more practical. The first patent for a transistor based power converter was filed in 1959 [11], allowing for an increase in switching speed compared to electromechanical switches. The initial development of these switching converters was mainly driven by aerospace applications, where the reduced weight and size and the improved efficiency made up for the high cost [12]. Gradually, improved power transistors with fast switching speeds and increased voltage ratings became available, and switching converter technology began to trickle down to consumer applications.

A major milestone in the use of switching converters in commercial applications was the availability of controller ICs by 1976, which could replace the until-then discrete control circuits consisting of several dozen discrete components [13]. As with many other analog and digital integrated circuits, the availability of standard building blocks in a single package reduced the design effort and footprint of switching converters, and opened the door for the widespread implementation of switching converters. Around the same time, the first power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices were introduced, which offered superior switching speed and a high input impedance compared to the bipolar power transistors that were used until then [14]. The combination of both of these factors meant that high-performance switching converters became affordable enough for use in consumer applications.

Because all high-performance high-voltage power MOSFET devices are vertical devices to achieve good high-voltage transistor performance in a limited silicon area by using the thickness and doping of the epitaxial layer to provide the required voltage blocking capabilities, these power MOSFET devices typically use the backside of the device as the drain contact [15]. Because of this, in these power MOSFET devices, the entire bulk of the substrate is at the drain voltage potential, which is not compatible with integrating multiple independent devices or low-voltage analog or digital devices on the same chip. Through the use of the RESURF (Reduced Surface Field) technique [16], area-efficient power MOSFET devices with drain and source contacts on the top-side of the device became possible. With these devices, multiple independent high-voltage devices and low-voltage analog and digital circuits can be integrated on a single chip, and so-called smart-power ICs where power devices are combined with low-voltage analog and digital circuits became a possibility. This further degree of integration allows for combining the controller and power devices on a single IC, which reduces the parts count and size of switching converters, and facilitates the implementation of such a converter.

This is not a new idea, as some commercial products, mainly in mains powered AC-DC applications, have been available for almost 2 decades [17]. Because of technological limitations of the high-voltage technologies suitable for mains-powered applications, that require breakdown voltage ratings of several hundred V, typically only straightforward topologies with a limited number of active devices such as buck and flyback, operating at relatively low frequencies are used in these applications.

More recently, we have seen an increase in these highly integrated converters as converters operating from an intermediate bus voltage to generate the appropriate IC supply voltages. Typical voltage ratings, depending on the application, use a bus voltage of 3.3 V to 20 V and output voltage of 0.8 V to 5 V [18] [19]. For these intermediate voltage ratings, highly integrated converters up to a few tens of Watts are available. Also, highly integrated buck converters that can generate the intermediate bus voltage from a higher distribution bus voltage, up to 60 V have become available, although at reduced power levels. Commercial ICs for these input voltage ratings that require an external rectifier achieve output currents up to 5 A [20], while versions with a synchronous rectifier achieve output currents up to 2.5 A [21].
Finally, in recent years the research on fully integrated converters with all passive components on the IC, including all inductors and/or capacitors has increased in popularity. For these converters, the driving factor is the maximum possible reduction of the number of external components for applications with very high density, such as in mobile applications. With the power supply completely integrated with the IC, it is possible to manufacture converters with a minimal footprint, although the limitations of integrated inductors and capacitors impose a practical limit on the achievable efficiency and power handling capability. Even in state-of-the-art fully integrated converters, output power is limited to approximately 5 W [22] [23].

2.4 Selection of the reference applications

In this section, we will discuss a number of potential application areas for hybrid monolithic high-power, high-voltage converters. While mass production of ICs can be relatively cheap per chip due to the economics of scale, the start-up costs for an IC production run are extremely high.Therefore it is not feasible in a research environment – where only a limited number of devices are required to verify the functionality and mass production is at best several years away from the initial prototypes– to have ICs manufactured in a standard foundry fabrication run. To allow research and educational centers to verify their IC design in hardware, a number of Multi Project Wafer (MPW) service providers, such as MOSIS [24], Europractice [25], and CMP [26] are available. These MPW services group multiple IC designs together on a mask set, which reduces the number of available samples per wafer, but also allows for sharing the initial cost, and brings IC manufacturing within the financial realm of possibilities for research facilities. Therefore, we are by necessity limited to applications that are possible to implement using technologies available through one of these MPW service providers, which will influence our application selection.

2.4.1 Home user: 230V AC

A first possible application area is in the conversion of the typical 230 V AC mains distribution voltage to voltages that are appropriate for modern day analog and digital circuits,

since this is a field with a large amount of applications. For any converter design that wants to benefit from the advantage of high switching speed to minimize the dimensions of transformers and filters, the AC voltage needs to be rectified immediately after it enters the converter and can not pass through a mains frequency transformer first to reduce the voltage. Because of this basic property, all of the currently available switching converters in mains powered applications are in fact DC-DC converters, even though the input is $230\ \mathrm{V}$ AC. The peak voltage in an AC system is $\sqrt{2}$ times the nominal voltage, with variations up to $240\ \mathrm{V}$ still being within the acceptable range for the voltage in Europe. Therefore any converter powered by the mains should be able to operate with a DC input voltage of $340\ \mathrm{V}$, which does not yet take into account spurious transients on the line. Although several mains-powered monolithic converters are commercially available [27] [28], no appropriate technologies are available for affordable prototyping [24] [25] [26]. Therefore, our research options in this application area are severely limited, and this is not a preferred field for our research.

2.4.2 Automotive: 12V DC to 42V DC

In the modern automotive industry, the so-called $12\ \mathrm{V}$ system based on a 6-cell lead-acid battery has been the default choice for nearly every manufacturer for several decades. Although the system is nominally referred to as a $12\ \mathrm{V}$ system, considerable tolerance on this value needs to be taken into account, as the voltage over a 6-cell lead-acid battery that is discharging is closer to $12.6\ \mathrm{V}$, and the voltage generated by automotive alternators while the engine is running is typically between $13.5\ \mathrm{V}$ and $14.5\ \mathrm{V}$. Therefore, the same system is more accurately – but admittedly less often – referred to as a $14\ \mathrm{V}$ system.

In the 1990's, under the impulse of Daimler-Benz, a consortium of vehicle manufacturers in the USA went through considerable effort to define a new standard for a more efficient energy distribution network in automotive application, both in terms of conductor cost and power loss. Their conclusion was that the highest DC voltage should be used for the distribution of electrical energy in automotive applications, while never exceeding the maximum voltages imposed by the guidelines for electrical shock hazards, i.e. $60\ \mathrm{V}$. The consortium agreed to the definition of a new standard $42\ \mathrm{V}$ electrical system, which was meant as an addition to the existing platform $14\ \mathrm{V}$ system to supply high-power loads, leading to a dual $14/42\ \mathrm{V}$ system. Low power systems could continue to use the existing implementations, while high-power systems could transition to the increased voltage for reduced conductor cross-sections, coupled with a reduced relative voltage drop. Simultaneously, a number of car manufacturers that are active on the European market, again under the impulse of Daimler-Benz, went through the same process, and agreed on the same dual $14/42\ \mathrm{V}$ standard for their future electrical systems.

However, as of today this switch-over has not occurred, despite relatively short term perspectives put forward by the respective consortia when the standards where drafted. One reason for the –perhaps indefinite– delay in introduction is that because of improvements in the efficiency of applications that were once thought to require the higher voltages, such as electrical power steering, the need for a higher voltage at a reduced current is now

somewhat less acute. Another reason is the relative cost increase to implement reliable mechanical switches, which are still ubiquitous in the automotive industry, at 42 V DC instead of 12 V DC. Because of the increased contact erosion at higher voltages, mechanical switches at increased DC voltages require more complicated spring design and the use of more exotic and expensive materials. Although the energy distribution itself would doubtlessly become more efficient with the proposed increased voltage standard, these side-constraints have caused the total cost-benefit balance to not yet become positive enough to warrant switching to a high-voltage or dual supply voltage system.
Although the input and output voltages of the proposed high-voltage standards for automotive applications are a good fit for the technologies that are available for prototyping through MPW services, the indefinite delay in the implementation of the standard limits the potential applicability of research on converters for this application, so this is not the most attractive option for our research.

2.4.3 Telecom: 48V DC

Because of the large regional differences, there is no such thing as a universal telecommunications voltage standard, however some of the technical considerations are generic enough to allow for a broad description of energy distribution systems. Typical telecommunications power distribution systems are designed to operate at voltages that do not pose shock hazards to a technician on accidental contact. In many cases, the power supply for the telecommunications back-office equipment is complemented by a bank of lead-acid batteries, both to stabilize the supply voltage under transient conditions and to keep the equipment powered on should the mains power fail.
Broadly speaking, most regions have adopted a 48 V DC nominal supply voltage, with a tolerance range of 40.5 V to 57 V DC [29], since voltage in excess of 60 V are considered to be a lethal shock hazard in most modern classifications. However, there is also an older 60 V DC nominal supply voltage, with a tolerance range of 50 V to 72 V DC, and many types of equipment are required to be able to operate from both supply voltage ranges for legacy compatibility reasons. Therefore, a typical ”universal” telecom voltage converter has a nominal input voltage of 48 V DC, but with a wide input voltage tolerance. Many telecom voltage converters are specified over an input voltage range of 36 V to 72 V to be able to operate on infrastructure for both standards and to allow for some headroom for unforeseen voltage drops in the conductors or connectors.
At the point of load, a number of different voltages are used in telecom applications, with typical values being 12 V, 5 V, and 3.3 V. Like the automotive application, the voltages in these telecom applications are a good fit for the technologies available through the MPW services. Because of the required voltage and power ratings, most of these telecom applications are built using discrete power devices, although they should be within the realm of possibilities of the technologies available through the MPW services. Also, because of the large number of telecom converters already deployed in the world, there is a proven demand for this type of converters, and the potential impact of improvements in this application field is substantial.

2.4.4 Specification of the reference applications

As stated in the discussion of the scope, we will limit ourselves to applications where cost-efficient converters can be implemented using high-voltage ASIC technologies that are available for prototyping, while aiming for an increase in output power compared to existing (hybrid) monolithic integrated converters.
If we take into account the limitations of the technologies that are available for prototyping and some of the possible applications that have been highlighted before, it is clear that we will be focusing on the domain of the end-user applications instead of the field of distribution or transmission. In the end-user application domain, a reference application in the telecommunications appears to be the most attractive choice. Although a huge field of applications exists for mains-powered home user applications, it is not possible to prototype hybrid monolithic integrated converters that can operate at the appropriate voltages, so these will not be considered in this work. The voltage ranges that are used in current and future automotive applications appear to be an interesting market for hybrid monolithic integrated converters. However, the lack of available discrete reference applications would render it impossible to compare the performance of hybrid monolithic integrated converters with existing implementations, and the lack of available applications would delay any practical applicability of the converter analysis and optimization with at least several years. Therefore, as the reference applications for this work, two sets of converters specifications for use in telecommunications equipment were selected. From a market demands exploration and an initial feasibility study, a nominal $48\ \mathrm{V}$ input voltage (with a tolerance range for the input voltage between $36\ \mathrm{V}$ and $72\ \mathrm{V}$) and an output voltage of $12\ \mathrm{V}$ at $3\ \mathrm{A}$ to $6\ \mathrm{A}$ was selected as a first reference case, and a telecommunications converter with the same input voltage range with a $5\ \mathrm{V}$ output at approximately $10\ \mathrm{A}$ was selected as a second reference application. We will explore the optimization possibilities for hybrid monolithic integrated converters with these specifications, which extends the maximum usable bus voltage of state-of-the-art hybrid converters, and allows for increased output current compared to state-of-the-art converters.

2.5 Conclusions

In this chapter we have introduced some of the design considerations for an efficient energy distribution network, from the generation over the transmission and distribution grid to the end user. By transporting electrical energy at the maximum possible voltage the power loss in the transport is minimized, and the voltage is reduced to the one required by the load as close to the point of load as possible. For most high-power applications, AC distribution at a couple of tens of Hertz remains the optimum balance between cost, efficiency, and size of the system, where-as thanks to switching power converters closer to the load these same design criteria typically lead to a DC distribution system, with successive down-conversions through DC-DC converters. We have briefly explored the history of switching converters, and identified the factors that enabled them to become increasingly more compact, efficient, and low-cost. Although major improvements in the

available devices and materials can not be ignored, the increased integration of control circuits, drivers, and power devices has enabled a widespread implementation of these switching converters.
In this work, we aim to optimize the performance of high-power, high-voltage hybrid monolithic DC-DC converters, using affordable smart-power technologies for the implementation of the active and passive devices where appropriate, but still allowing the use of external components where integrated devices would impose overly strict limitations on the performance of the converter. To extend on the state-of-the-art highly integrated converters, we aim for an increase in the potential operating voltage range and output current. For this goal, we have highlighted a number of possible end user categories, and selected two test-cases where we expect the results of the research to be most valuable.

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3

Topology optimization for smart-power converters

3.1 Introduction

In this chapter, we will define a method to optimize the converter topology for integration in a smart-power technology. At first we will ignore all physical limitations, and imagine which properties an ideal converter would have. Then, in a closer approximation of the reality, we will introduce some of the practical properties of the smart-power technologies wherein we would like to implement our converter. We will show that the properties of smart-power technologies are sufficiently different from discrete converter implementations that the de-facto standard topologies for the different power levels need to be reconsidered for monolithic integration. Based on the properties of the smart-power technologies, we will define a cost function for the implementation of different converter topologies, which will enable us to compare different topologies at a very early stage in the design. Minimizing this cost function will allow us to select the optimal topology for monolithically integrated converters. At the end of this chapter, we will apply this to the reference cases we have selected in the previous chapter.

3.2 The ideal converter

In the previous chapter, we have established that the requirements on the voltage for efficient transportation of energy and for the efficient use of energy are mutually exclusive,

and any attempt to satisfy both requirements at the same time is bound to be sub-optimal. The alternative to compromising on a middle ground for the voltage is using the highest possible voltage for the distribution of electrical power, to keep the current, and thereby the conduction losses in the distribution conductors as low as possible without an exceedingly high cost for the conductive material, combined with a conversion to a lower voltage that is suitable for an efficient use of the electrical energy as close as possible to the point of load (POL).

This assumes a voltage converter at the point of load, which will also have an impact on the system. To be able to quantify how good a converter is, we will first ignore all physical limitations and describe an ideal converter.

3.2.1 Zero size

In nearly all electronic applications, there are constraints on the physical dimensions, and power converters as a subsystem of an application is no exception to this rule. From the system viewpoint, power conversion is a necessary evil which does not add any functionality to the system and therefore it should be as unobtrusive as possible. Depending on the application, these limitations can be either in 2 or 3 dimensions. In most older electronic applications, the board space was typically a limiting factor, and the ideal converter would occupy $0\ \mathrm{cm}^2$ of Printed Circuit Board (PCB) real-estate.

Nowadays, modern electronic systems have become increasingly dense, and system designers attempt to use the third dimension as efficiently as possible as well. Many systems are designed to fit in a given 3-dimensional space, since they are used in either very compact applications such as hearing aids or mobile phones, or in close proximity to other electronic or mechanical systems, such as in automotive and telecommunications applications. A more modern interpretation of the ideal converter would therefore also include the third dimension and the ideal converter would occupy $0\ \mathrm{cm}^3$.

3.2.2 Zero cost

Every company that sells a product and operates in a competitive market has to be constantly aware of the product cost, and strive to reduce it as much as possible while still satisfying all the implicit and explicit requirements put forward by the customer, e.g. functionality, lifetime, reliability, etc. Design and manufacturing of electronic circuits is an extremely competitive market, so it should not come as a surprise that product cost is an important driver in the design of any electronic system.

To minimize the impact of the converter circuits on the total system cost, the cost for the development, integration, and manufacturing of the converters should be as low as possible. In short: we want our ideal converter to cost nothing at all, or to put it into numbers, the cost for our ideal converter is 0 US$ or 0 €.

3.2.3 Zero dissipation

There are multiple reasons why power dissipation in the converter circuit is undesirable. Primarily, we want the converter circuits to be as efficient as possible to ensure an optimal power distribution in the system. This is of paramount importance in battery-powered systems to squeeze as much operating time out of a given battery, but is becoming increasingly important for mains-powered systems as well. Both the customers and the regulating agencies are demanding that electronic systems that come on the market do not consume excessive electrical power, driven by both ecological and economical concerns.
Additionally, thermodynamics dictate that any difference in input power and output power is evacuated from the converter in the form of heat, otherwise the internal temperature would continue to rise. Since reliability and lifetime of electronic equipment tends to decrease sharply with temperature, the temperature in the converter, and by extension in the system needs to be kept within acceptable limits.
To ensure this, all heat generated in the converter needs to be evacuated to the environment. Small amounts of heat can typically be dissipated by using natural convection in the surroundings, but thermal management solutions, such as large heat-sinks, heat-pipes, and/or forced active cooling may be required to keep the temperature within limits for larger amounts of heat. Needless to say, adding additional thermal management solutions to a system increases system complexity, cost, and potential points of failure, so this is avoided wherever possible.
Ideally, the converters – which are intended to enable a more efficient transfer of energy – should not be the cause for either additional dissipation or introduce additional thermal management issues, however small they may be. Therefore, we can conclude that our ideal converter would have a dissipated power of $0\ \mathrm{W}$.

3.2.4 Additional properties

These three properties are almost universally considered to be the most important characteristics of power converters, regardless of the power level and application. The weight given to each property can be different for individual applications, however every application is fundamentally limited in size, cost, and power dissipation. Besides these three basic properties, the application can impose additional properties. These additional properties are not as universal, but can nevertheless be crucial in the development of converters for a given application.
For converters that are powered by the $50\ \mathrm{Hz}$ or $60\ \mathrm{Hz}$ mains, Power Factor Correction (PFC) [1] and a limited standby-power consumption [2] are in many cases a legal requirement before the product is allowed on the market. Often, the measures that are necessary to comply with these requirements will negatively impact size, cost or power dissipation, but the negative economical consequences of non-compliance force manufacturers to take the required measures.
Other requirements that are imposed on converters may include reliability, availability, lifetime, etc. Typically, these will also influence the size, cost and power dissipation.

Especially when converters are intended for large volume production, they are often designed at the very limit of these additional requirements to limit the impact on the main parameters.

3.2.5 Conclusions

Obviously, the ideal converter we described above is physically impossible to implement in the real world. However, it gives us a clear goal to work towards when we are optimizing our high-power monolithically integrated converters: our ideal real-life converter should be as small as possible, as cheap as possible and be as efficient as possible.

3.3 Semiconductor devices

All devices that can be integrated in smart-power technologies are semiconductor technology based, and it is necessary that the reader is familiar with some basic concepts for the operation of these devices to be able to understand the practicalities of implementing a converter in a smart-power technology. It is by no means the intention of the following sections to provide a thorough discussion of the physics behind the operation of semiconductor devices, and we will limit ourselves to an abstract high level description of the most important devices for the integration of converters to enable the reader to understand some of the design aspects without being intimately familiar with the devices in a converter application. The reader interested in an in depth discussion of the physics behind the device operation is referred to a number of standard works in the (power) semiconductor device physics field [3] [4] [5] [6].

3.3.1 Transistors

The first category of devices that we will discuss are transistor-type devices, which are devices that can amplify or control electrical signals. A transistor-type device has at least 3 terminals, and a voltage or current that is applied to one of the terminals can control the current through the other terminals. A number of different devices have these characteristics, the two most common categories of transistors in modern applications are bipolar transistors and field-effect transistors. In bipolar transistors, the three terminals are referred to as the *base*, *collector* and *emitter*, with the current in the base controlling the current through the collector and emitter. In field-effect transistors, the three terminals are referred to as the *gate*, *drain* and *source*, with the voltage on the gate controlling the current through the drain and source. In the case of field-effect transistors, a fourth terminal called the *bulk* represents the potential of the silicon area below the actual transistor, and is a consequence of the physical build-up of a field-effect transistor. The voltage on the bulk terminal can be seen as a second gate terminal that also influences the current through the drain and source, but not as strongly as the gate terminal.
Although a full derivation of each transistor type leads to a number of distinct operating areas, each governed by equations derived from the physical structure, at our high

level description we can limit ourselves to two possible utilization areas for transistors. Transistors can then be considered to be either linear amplifiers or switches, and we will briefly discuss both categories.

Transistors as linear amplifiers

When transistors are used as linear amplifiers, they are biased in an operating region where a small change in the base current or gate voltage is amplified as a proportional change in current through the output terminals. The bias conditions that are necessary to ensure a transistor is operating in the linear region imply that there simultaneously will be non-negligible current and voltage on the device terminals. Any time current and voltage exist at the same time over two terminals of a device, the corresponding electrical power is dissipated in the device. Transistors are usually driven in their linear region as part of analog circuits, such as amplifiers.
Because of the inherent power dissipation in the device, the use of transistors as linear amplifiers for power conversion is limited to relatively low power applications, such as in linear regulators, which we will discuss later in this chapter.

Transistors as switches

For high-power converters, transistors are typically used as switches to limit the dissipation. To use a transistor as a switch, it is driven outside the linear operating region. If the switch is in the on-state, the transistor is driven by a gate voltage or base current that ensures a large current can flow through the drain-source or collector-emitter terminals. Ideally, if the transistor is driven to be in the on-state, no voltage drop exists over the device, which would imply no dissipation in the device. In the case of bipolar devices, it is impossible for the collector-emitter voltage to drop below the saturation voltage V_{sat} while appreciable current is flowing. In the case of field-effect transistors, the device in the on-state is equivalent with a resistor R_{on} between the drain and the source, causing a resistive drain-source voltage drop $V_{ds} = R_{on} I_{ds}$ while current I_{ds} is flowing through the drain-source terminals. Alternatively, if the switch is in the off-state, the transistor base or gate is driven to ensure as little current as possible flows through the drain-source or collector-emitter terminals. In this state, typically a large voltage exists over the device but the current is limited to a small leakage current. This combination of either large current and low voltage or low current and high voltage allows for the construction of circuits with low dissipation in the transistors. Outside of the power conversion world, the typical application for transistors as switches is in digital circuits, where the same property is used to ensure low dissipation while the circuits are inactive.

3.3.2 Diodes and synchronous rectifiers

As will be seen in the overview of switching power converter circuits later in this chapter, most of the switching converters circuits only need a very limited number of switches that can be actively controlled. The remainder of the current flow can be regulated by diodes

or rectifiers, which are unidirectional circuit elements. Ideal diodes can block any voltage in their reverse bias region and allow any current to flow in their forward bias region. Obviously, real diodes will have some limitations, which we will discuss now.
A standard silicon bipolar diode is formed by creating a P-type doped silicon area immediately adjacent to an N-type doped silicon area. Without an applied voltage or with a negative applied voltage, a depletion layer is formed at the interface, or *PN-junction*, which acts as an insulator and prevents the flow of current. A PN-junction diode needs a forward voltage of approximately 0.7 V before the depletion region at the junction is sufficiently narrow to allow substantial current flow, and the diode is said to be turned on. Therefore, for a bipolar diode to conduct current, there is a voltage drop of at least 0.7 V, but for discrete high-voltage and high-power diodes at full load current, the voltage drop can be several V. The power dissipation in a diode while it conducts current I_{diode} is:

$$P_{diode} = V_{drop} I_{diode}$$

The Schottky diode is formed at a metal-semiconductor junction, which creates a Schottky barrier. The diode characteristics are determined by the type of metal and semiconductor that is used, but in general the Schottky diode can have a lower forward voltage drop than a silicon PN-junction diode, typically starting from 0.15 V to 0.45 V at low currents. This lower voltage drop reduces the dissipation in the diode when in the on-state, but comes at a price: Schottky diodes have limited reverse voltages (often less than 50 V), and can have significant leakage in their off-state. As discrete devices, Schottky diodes are popular rectifiers in low-voltage, high-frequency applications. However, not many smart-power technologies offer optimized or qualified Schottky diode devices, which limits their use in monolithically integrated converters.
Another way to implement a rectifier is as an actively controlled switch, i.e. a bipolar transistor, insulated gate bipolar transistor (IGBT), or a power MOSFET. The control circuit for the switch is then designed to turn the device on when the device is supposed to conduct (the forward bias region), and turn the device off when the device needs to block current (the reverse bias region). Since the control of the rectifier now needs to be synchronized with the turning on and off of the main switch(es) of the converter, this configuration is often referred to as a synchronous rectifier (SR). For bipolar transistors and IGBTs, this reduces the voltage drop in the forward region to the saturation voltage of the transistor, which is typically lower than the voltage drop over a diode. For MOSFET power devices, the voltage drop in the on-state is the product of the current and the equivalent channel resistance of the MOSFET in the on-state R_{on}. Therefore, the power dissipation in a MOSFET synchronous rectifier during the on-time of the transistor is a quadratic function of drain-source current I_{ds}.

$$P_{SR} = R_{on} I_{ds}^2$$

Since the R_{on} is determined by the dimensions of the MOSFET in smart-power applications and by the number and type of parallel MOSFETS in discrete applications, the dissipation in a MOSFET synchronous rectifier can be lower than is possible in bipolar

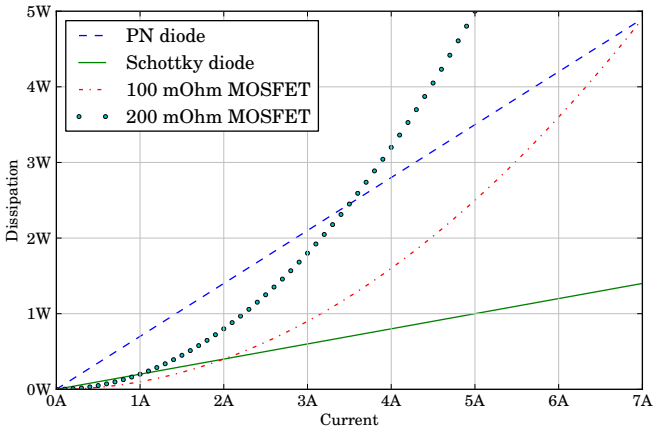


Figure 3.1: Conduction loss with PN diode, Schottky diode, and synchronous rectification versus current

devices. This is illustrated in Figure 3.1, where the power dissipation versus current is plotted for a PN diode, a Schottky diode and 2 power MOSFET channel resistances. Up to approximately $3.5\ \mathrm{A}$ the power dissipation with a $200\ \mathrm{m}\Omega$ MOSFET SR is less than is possible with any PN diode. By placing a second identical MOSFET in parallel, the effective MOSFET R_{on} is halved to $100\ \mathrm{m}\Omega$, and the dissipation in the synchronous rectifier is halved. Therefore, the conduction loss in the $100\ \mathrm{m}\Omega$ SR is less than in a PN diode rectifier up to approximately $7\ \mathrm{A}$. Because of the fixed forward voltage drop in bipolar devices, placing multiple diodes or bipolar synchronous rectifiers in parallel does not reduce the total conduction loss of the rectifier.

It should be noted that the conduction loss is not the only relevant loss component for rectification, but since the conduction loss scales in a linear or quadratic fashion with the current through the device it is definitely an important part of the dissipation at full load. The other loss components either depend on the switching frequency, such as the reverse recovery loss in PN-junction diodes or energy that is used in the gate charge of the synchronous rectifier, or the leakage in the off-state, which is especially relevant for Schottky diodes.

3.4 Smart-power technologies

For low-cost power transistor technologies the specific on-resistance ($\Omega\mathrm{mm}^2$) for DMOS transistors can be approached by $R_{on} = k_{Si} V_{ds,max}^{2.5}$. This expression is known as the silicon limit [7] for regular DMOS transistors, with k_{Si} a factor depending on geometry and doping. This is not a hard limit for silicon DMOS transistors, as so-called superjunc-

tion transistors can exceed this limit [8]. For superjunction transistors, the exponent of the drain-source voltage is reduced. Therefore, superjunction transistors can be much more efficient for implementing high-voltage transistors. However, this requires multi-layer epitaxy (striped or layered implants) in the drain region, which is a relatively complicated and expensive technique (€ per mm^2). Therefore, these types of transistors are generally reserved for discrete power transistors for voltage ranges in excess of approximately $100\ \mathrm{V}$. There is no technical reason these super-junction transistors would not work for smart-power technologies, or for lower voltage ranges, however, as far as we know, no foundry is offering lower voltage devices or smart-power technologies based on superjunction transistors.

This relation implies that for a DMOS with a constant on-resistance, the required silicon area rapidly increases for increasing drain-source breakdown voltage. Because all transistors in a smart-power technology share a common substrate, we need to take into account the isolation between individual transistors, and the isolation of the transistors to the common substrate to determine the required silicon area. A number of different techniques exist for isolating the transistors from each other and from the substrate in smart-power technologies. [9, 10].

A first isolation technique uses inversely polarised PN junctions between each transistor and between all transistors and the substrate. A cross-section of a generic junction isolated technology is shown in Figure 3.2a.

Technologies using these techniques are often referred to as junction isolated smart-power technologies (e.g. On Semiconductor I3T80, STMicroelectronics BCD 5). An advantage of this type of isolation is that it is relatively cheap and easy to implement in a standard CMOS technology, as it only requires sinker and buried layer implant capabilities. A disadvantage of this type of isolation is the considerable silicon area that is required to implement lateral isolation between adjacent devices, since the sinker implant needs to be sufficiently wide to maintain the depletion layer on both sides of the isolation structure under worst case conditions. In these junction isolated technologies, it is paramount that the substrate is thoroughly tied to the lowest possible potential in the circuit, since the isolation depends on the existence of the depletion layer. Besides the significant silicon area required to implement these isolation structures, the reversed biased PN junction can also add significant capacitance from the circuit nodes to the substrate, which can limit the switching speed of the devices.

A second possible isolation technique is realized by creating a trench in the semiconductor material, which is subsequently filled with a dielectric (e.g. On Semiconductor I3T50). A cross-section of a generic trench isolated technology is shown in Figure 3.2b. Trench isolation allows for a compact isolation structure between the different transistors, since there is no need to allow space for a depletion region to form. However, the isolation towards the substrate is still realized using an inversely polarized diode. Since the substrate potential is not used as a circuit terminal or for isolation between the transistors, the substrate automatically follows the lowest potential in the circuit through the parasitic substrate diode in each of the pockets and does not need to be tied to the lowest potential in the circuit. Since no reverse biased diodes are used for the isolation between the de-

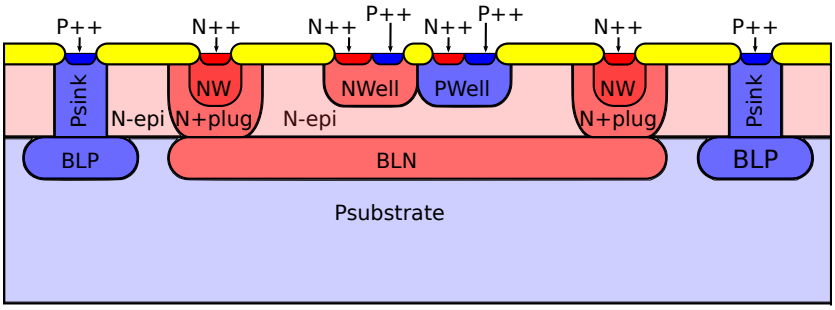
vices in trench isolated technologies, the parasitic capacitance from the circuit nodes to the substrate is reduced compared to junction isolated technologies.

A third possible isolation technique is the use of Silicon On Insulator (SOI), where each transistor or group of transistors is insulated in all directions through a dielectric material. A cross-section of a generic SOI technology is shown in Figure 3.2c. In these technologies, all voltages in the different semiconductor pockets can float to arbitrary voltages, regardless of the potential of the substrate or neighboring pockets, provided the dielectric breakdown voltage isn't exceeded. Therefore, in SOI technologies the node voltage can become more negative than the substrate voltage. An example of smart-power technologies using these isolation techniques is the Philips ABCD technology family. Unfortunately, these technologies are typically more expensive, and none of these SOI technologies is available through the affordable MPW services coordinated by Europractice, MOSIS, or CMP, so this type of isolation will not be included in the design considerations.

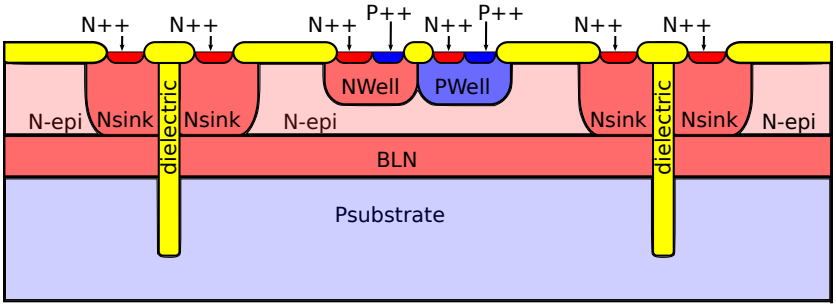
In conclusion, for all the technologies that are available to us for prototyping, no node can go to a more negative potential than the substrate. Therefore, we need to take into account the maximum potential difference between any two points at any point in time in the circuit to determine the voltage stress the technology needs to be able to withstand, and not just the drain-source voltage of individual transistors, as is the case in discrete implementations of switching converters. From now on, we will refer to this maximum potential difference as voltage stress V_{stress}. This voltage stress is a crucial parameter in selecting the appropriate smart-power technology, since choosing a technology with a voltage rating that is much higher than required for the application will lead to a sub-optimal converter. Either the converter will suffer from excessive conduction loss, since the power transistors have a larger on-resistance (for the same silicon area), or the converter will require more silicon area, thereby increasing switching losses and cost of the converter.

Similar to regular, low-voltage CMOS technologies, every foundry that has smart-power technologies in their portfolio makes unique choices in determining the process flow and process options to optimize their product to their target customers and applications. Because of this, large differences exist in the specifications for different smart-power technologies. To compare different technologies with similar V_{stress} rating, we can use the specific on-resistance of the transistors. This value, expressed in $\mathrm{m\Omega mm^2}$, can give an indication of the required silicon area to implement a transistor with given conduction loss.

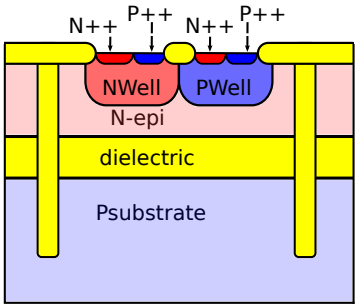
Table 3.1 gives an overview of the specific on-resistance and the maximum voltage stress for an N-type DMOS in the smart-power technologies of Austria MicroSytems [11], On Semiconductor [12], Philips/NXP [13], and STMicroelectronics [14]. Due to the cost of ASIC prototyping, any implementation we realize is limited to technologies available through MPW services such as Europractice, CMP, or MOSIS. Therefore, the subset of technologies that is available through MPW services is indicated in Table 3.1.



(a) Junction isolation



(b) Trench isolation



(c) Silicon on insulator

Figure 3.2: Cross section of isolation structures in smart-power technologies

Foundry	Technology	Vstress(V)	Ron× Area($m\Omega mm^2$)	MPW
AMS	H35	50	110	✓
	H18	20/50	15/110	✓
ON Semi	I2T100	40/60/95	87/153/488	✓
	I2T30	25	139	✓
	I3T80	72	260	✓
	I3T50	14/40	31/52	✓
	I3T25	12	35	✓
Philips	A-BCD1	18/25/60	50/60/150	
	A-BCD2	18/25/60/100	28/43/135/210	
STMicro	BCD4	30/45/70/80/90	50/70/190/280/420	
	BCD5	16/20/48/70	15/27/76/210	
	BCD6	5/12/20	7/12/21	

Table 3.1: Characteristic values for various smart-power technologies

Topology	Power level
Flyback converter	<100 W
Forward converter	$50 - 200$ W
Half bridge	$100 - 500$ W
Full bridge	>500 W

Table 3.2: Typical topology choice in discrete converters depending on output power

3.5 Cost function for ASIC implementation

In the literature a large number of converter topologies have been described, and throughout the years different topologies have crystallized as being optimal for different power levels. In Table 3.2, we have summarized some of the typical application levels for different topologies from a number of sources [15]. Even though some shifting has occurred over the years because of optimizations in control methods, device fabrication and device packaging, this topology optimization is time-tested for discrete converters. However, these results can not be directly transposed to smart-power converters, for both economic and technical reasons. The cost of any electronic circuit is the sum of silicon cost, packaging cost, inventory cost, assembly cost, etc.

For a discrete power transistor, the silicon cost for the power transistor is often only a small part of the total cost of the converter, and in nearly all cases the optimal converter is not the converter with the lowest silicon cost. In a smart-power converter, all power transistors can be integrated on a single die, thereby eliminating much of the overhead costs in a discrete implementation. For these smart-power converters, the power transistors are typically much larger than the associated control circuitry, because the power transistors

need to be able to withstand either a much larger current, or a higher voltage than the control circuits, or both. To enable a comparison between different possible implementations at an early design stage, i.e. without going through the entire design procedure and comparing the end result, it is essential that some abstractions are made.
For the topology optimization, it will be assumed that the silicon cost of the converter is proportional to the silicon area used in the implementation, regardless of foundry and technology. Obviously, this is a gross oversimplification [16], as this does not take into account engineering cost, number of masks, mask cost, wafer size, tool cost, series size, yield, testing cost, licensing fees for IP blocks, etc. For example, the cost for a full set of masks for a last-generation ($22\ \mathrm{nm}$) technology node has been estimated to be on the order of 1 to several million $ [17] in 2009, while a full mask set for a $0.35\ \mu\mathrm{m}$ process was estimated in 2005 to cost around 60 000 $ [18]. Since power devices, unlike logic devices, do not approximately scale inversely proportional with the square of the minimum channel length, but remain more or less constant in area for a given voltage and current rating, economically viable smart-power technologies are typically limited to older technology nodes, between $0.18\ \mu\mathrm{m}$ and $0.7\ \mu\mathrm{m}$, depending on how complex the digital circuits are that are typically integrated with the power devices.

3.5.1 Silicon area vs. expected dissipation

By starting from the relation between the $R_{on} = \frac{kV_{ds,max}^{2.5}}{S}$ for a given silicon area S while a MOSFET transistor is turned on, we can estimate the conduction loss $P_{conduction}$ in each of the transistors when we apply superposition of the different current paths that occur during the operation of switching converters.
In Figure 3.3, this is illustrated for the 4 transistors in the primary circuit of a full bridge converter: a first current path with duty cycle δ passes through transistors T1 and T4, a second current path with duty cycle 0.5-δ passes through transistors T1 and T2, a third current path with duty cycle δ passes through T2 and T3 and a fourth current path with duty cycle 0.5-δ passes through T3 and T4. Therefore, in this circuit the number of power transistors $N_t = 4$, of which $N_s = 2$ transistors are in series for each current path. At the maximum duty cycle $\delta = 0.5$ the time duration of the second and fourth current paths is zero, and these current paths are not responsible for any conduction loss.
In the general case, superposition of the RMS current through the devices gives us:

$$P_{conduction} = \sum_{m,n} \frac{kV_{ds,max}^{2.5}}{S_m} I_{RMS,n}^2$$

Where S_m is the silicon area of transistor m in current path n, and $I_{RMS,n}$ is the RMS current in path n. The total silicon area for this conduction loss is $S_{total} = \sum_m S_m$.
We can note from this relation that it is possible to trade conduction loss for silicon area, so in this approximation the conduction loss can be made arbitrarily small by increasing the silicon area used for each transistor. Obviously, this would be cost-prohibitive, and

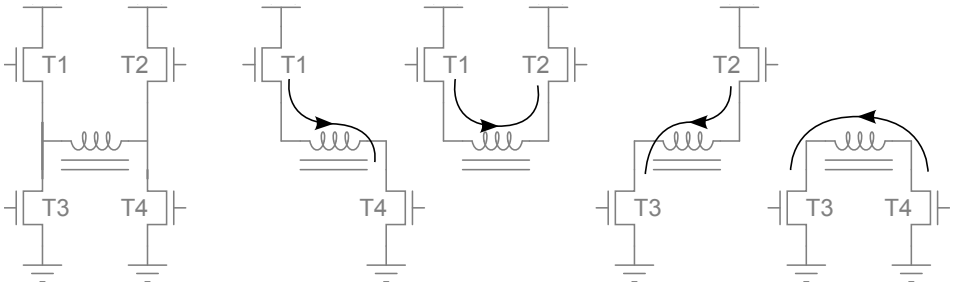


Figure 3.3: Current paths in the primary side of a full bridge

because the switching losses are approximately proportional to the silicon area, the optimal silicon area and the total power dissipation will depend on the switching frequency. By using the product of the dissipation loss and the silicon area as the cost function to minimize, we can optimize the smart-power implementation cost for different converter topologies without requiring information about switching frequency.
If we assume that all transistors involved in the power transfer are identical, the silicon area multiplied by the conduction loss can also be written as:

$$S_{total}P_{conduction} = \sum_{n} kN_t N_{s,n} V_{stress}^{2.5} I_{RMS,n}^2$$

Where N_t is the total amount of transistors involved in the power transfer, $N_{s,n}$ is the number of transistors in series for current path n. Obviously, the assumption of using identical transistors is only fair when all transistors pass the same RMS current and are of the same type. In some topologies, the RMS current is not equal for all devices, which will be mentioned in the discussion of the topology. Another reason why transistors may have different sizes even though the same current is flowing through them is when we want to mix N-type and P-type power devices in a single converter, this will be discussed in more detail next.

3.5.2 N type vs. P type

Since we use the silicon area and the on-state resistance of the power transistor in the cost function, it is important to make the distinction between N-type and P-type power MOSFETs. Theoretically, the P-type power MOSFET is expected to have approximately 2.5 times the on-state resistance for similar dimensions, because of the lower mobility of the charge carriers. In practical implementations, this value can be somewhat different due to differences in implementation, such as a vertical versus a lateral implementation, accounting for differences in tolerances for different masks and differences in the resurfacing structures for different vertical structures. These are typically determined by the device-engineers for a given technology and can not be changed by the circuit designer.

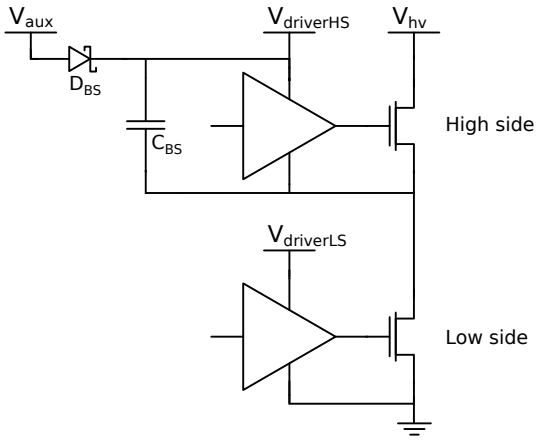


Figure 3.4: Bootstrap power supply for generating a floating supply voltage to drive an N-type high-side switch

In all smart-power technologies that are available for prototyping, only E-mode (enhancement mode) power transistors are used. This means that N-type MOSFETs are turned off when the gate voltage equals the source voltage and need a positive gate-source voltage to turn on. The P-type MOSFETs are also turned off when the gate voltage equals the source voltage, but need a negative gate-source voltage to turn on. For low-side switches, where the switch either conducts to ground or blocks a voltage, the choice for an N-type MOSFET with the source connected to ground comes naturally. The required voltage can easily be derived by a linear regulator from a higher voltage, such as the supply voltage or the output voltage. For a high-side switch, where the switch either blocks or conducts toward a higher voltage, the choice is less straightforward. An N-type MOSFET can achieve a lower on-resistance for the same silicon area than a P-type MOSFET, but requires a gate voltage that can exceed the positive supply voltage to turn on. The high-side driver voltage is typically generated using a so-called bootstrap power supply, as shown in Fig. 3.4. The operation principle of the bootstrap power supply is straightforward. When the switching node is pulled to ground by the low-side switch, the bootstrap diode conducts and the bootstrap capacitor is charged to the auxiliary supply voltage minus the voltage drop over the bootstrap diode. In many converters, the low-side driver voltage is used as the auxiliary voltage, although a different voltage may be used to optimize the converter performance. To optimize the power efficiency of this bootstrap power supply, discrete converters typically implement the bootstrap diode as a Schottky diode. Alternatively, the bootstrap diode is integrated with the controller or gate driver IC, often in the form of a synchronous rectifier to minimize the dissipation in the controller or gate driver IC. Because the bootstrap capacitor is connected to the source of the high-side MOSFET, the capacitor can then provide a sufficient supply voltage to allow the driver to turn the high-side switch on and keep it turned on while the switching node is pulled high.

In converters using discrete power transistors, adding a bootstrap capacitor and diode in exchange for being able to use a cheaper and higher performance N-type MOSFET as the high-side switch is typically the preferred approach. If the bootstrap diode is integrated in the controller or driver, or implemented as a small external SMD-type (Schottky) diode, a physically small SMD type capacitor is sufficient to provide the floating power supply for the high-side N-type power MOSFET. For monolithically integrated converters however, choosing between an N-type and a P-type power MOSFET can be less straightforward.
If we only take into consideration the area used to implement the power MOSFET and ignore the bootstrap circuit, the N-type power MOSFET will allow for a more area-efficient integration, because the mobility of the electrons (which are the majority charge carriers in the N-type MOSFET) is higher than the mobility of the holes (which are the majority charge carriers in P-type MOSFETs). However, if the bootstrap circuit needs to be integrated on the smart-power ASIC, we need to consider the area used by the bootstrap circuit when comparing the N-type and the P-type.
Although many smart-power technologies have dedicated capacitor structures, such as MIMC (Metal Insulator Metal Capacitor), which provide relatively high capacitance per surface area compared to using the capacitance between the gate and MOSFET channel in less advanced CMOS technologies, integrating large capacitor values requires a significant silicon area, and is therefore expensive. In discrete converters, the bootstrap capacitor is typically dimensioned to allow for a certain voltage ripple caused by the charging of the gate capacitance [19, 20], often in the order of 5 to 10 %. In a monolithically integrated bootstrap circuit, such strict demands on the voltage ripple would lead to a bootstrap capacitor that uses a silicon area that is an order of magnitude larger than the N-channel MOSFET that it is providing a supply voltage for.
This might seem paradoxical at first, considering that the dedicated capacitor structures have a higher specific capacitance (capacitance per silicon area, in $\mathrm{fF/mm^2}$) than the MOSFET gate capacitance. However, one should keep in mind that a MOSFET is a 3 terminal device (or 4 terminal device if the bulk/substrate is considered to be a separate connection), and the MOSFET gate capacitance is not a single physical capacitor between gate and source. The parasitic gate capacitance is composed of the gate-source capacitance C_{gs} between the gate and the source of the MOSFET and the gate-drain capacitance C_{gd} between the gate and the drain MOSFET. This is illustrated in Figure 3.5. When starting from the off-state, the gate-source voltage equals 0 V, while the gate-drain voltage is equal to the drain-source voltage. In the transition to the on-state, both of these capacitances need to be charged by the driver circuit, which is powered by the bootstrap capacitor. For the gate-source capacitance, the charging is intuitive: the gate-source capacitor is charged through the driver from a zero voltage to $V_{gs,final}$, the final gate-source voltage. The energy required to charge this capacitor is therefore given by:

$$E_{C_{gs,off->on}} = \frac{1}{2} V_{gs,final}^2 C_{gs}$$

The charging of the gate-drain capacitor is somewhat less intuitive: in order to change the voltage on the gate-drain capacitor, there needs to flow a current from the gate to

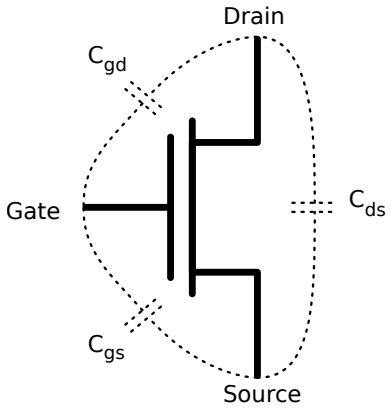


Figure 3.5: Parasitic capacitors indicated on an N-channel MOSFET

the drain. Because the source node of the high-side switch is also the switching node, which is pulled low by the low-side switch before the high-side switch is turned on, and the gate-source voltage is zero at the beginning of the transition sequence, the gate-drain capacitor of the high-side switch is charged to the inverse of the high-voltage supply. To avoid shoot-trough currents, where the power supply is effectively short-circuited when the high-side and the low-side switch simultaneously conduct which causes large currents to flow, appropriate delays will be inserted in the gate drive signals to ensure the low-side switch is completely turned off before the high-side switch starts to turn on. After the turn-on of the high-side switch, the drain-source voltage over the high-side switch is reduced to the drain-source voltage drop, which is equal to the drain-source current multiplied by the transistor on-resistance. Because the gate is charged to $V_{gs,final}$, and the drain-source voltage is close to zero after the MOSFET is turned on, the energy required to charge the gate-drain capacitor can be approximated by:

$$E_{C_{gd,off->on}} = \frac{1}{2}\left((-V_{hv})^2 - (V_{gs,final})^2\right) C_{gd}$$

Because V_{hv} is significantly higher than V_{gs}, and this value is squared in the equation for the required energy, the bootstrap capacitor value needs to be much larger than the simple sum of C_{gs} and C_{gd} to be able to provide a sufficient amount of energy to turn on the high-side MOSFET.

In the above equations, the C_{gs} and C_{gd} capacitance values have been considered as constants. For C_{gs}, this is a reasonable assumption, since this value is mainly attributed to the overlap capacitance of polysilicon gate to the source and channel regions. For C_{gd} however, which is composed of both the overlap capacitance and the capacitance associated with the depletion region this value is a highly non-linear function of the applied voltage [21].

Because of this non-linear capacitance value, the value that is typically specified for discrete MOSFETs for switching applications is the gate charge Q_g, which is the amount of

charge required to reach a certain final gate voltage for one or more initial drain-source voltages [22], starting from a gate voltage of 0 V . This simplifies the calculations for the required bootstrap capacitor size. For the smart-power technologies that are available to us, these values are typically not specified, so they are extracted from simulation.

In Table 3.3, the capacitor charge Q_{cap} per mm^2 for a MIMC capacitor at different voltages is compared with the charge required to reach a final gate-source voltage $V_{gs,final}$ from 0 V for a VFNDM50 high-voltage N-channel MOSFET at different initial drain-source voltages $V_{ds,initial}$ in the ON Semiconductor I3T50 technology.

Even when just comparing the charge storage capabilities for the capacitor structures with the required gate charge to turn on a power MOSFET, it is immediately obvious that we will not be able to ignore the area used by the capacitor structures. Imposing a similar voltage drop requirement on the bootstrap capacitor voltage as in a discrete implementation will lead to a bootstrap capacitor structure that is an order of magnitude larger than the transistor to be driven. With an ideal driver that can transfer the charge from the MIMC to the gate of the MOSFET without any loss, a 10% ripple requirement corresponds with the MIMC being discharged from 3.3 V to 3.0 V, while the gate is charged from 0 V to 3.0 V. Since this difference in voltage corresponds with $0.4\ \mathrm{nC/mm^2}$ of MIMC, and $8.8\ \mathrm{nC/mm^2}$ is required to charge the MOSFET gate to 3.0 V for just 10 V as the initial drain-source voltage, this requirement would lead to at least $22mm^2$ MIMC per mm^2 of N-type DMOS.

Obviously, this is not an attractive option for the high-side switch if the smart-power technology allows for the implementation of P-type MOSFETs that do not require a bootstrap circuit and only use approximately 2.5 times the area of an N-type MOSFET to achieve similar on-resistance. Therefore, we will examine the effect of imposing less strict limits on the voltage drop on the bootstrap capacitor. An absolute lower limit for driving any switch in a switching converter is that the switch can be controlled, i.e. turned on and off.

By definition, the threshold voltage V_{th} is the minimum gate-source voltage at which strong inversion of the silicon surface under the poly is achieved and a significant current can flow in the conductive channel that is formed between the drain and source [5]. For discrete power MOSFET devices, the threshold voltage is often specified as the minimum gate bias for a drain-source current of 250 µA with $V_{gs} = V_{ds}$ [21]. Obviously, using the same technology and the same channel length, a device with a narrow channel will need a much higher gate voltage to be able to conduct a given current than a device with a wider channel. Therefore, if it is possible to adjust the dimensions of the MOSFET channel in function of the desired drain-source current, the threshold voltage is typically extracted from a measurement of the transconductance in function of the gate voltage for a small fixed drain-source voltage [23]. In a typical MOS technology, the threshold voltage is adjusted or tuned at manufacturing time to be approximately the nominal supply voltage divided by a factor of 3 to 4.

Although a conductive channel exists as soon as the gate voltage exceeds the threshold voltage, a voltage in excess of this threshold voltage needs to be applied to the gate to allow the current handling capability associated with a switch in the on-state. This voltage in excess of the threshold voltage is referred to as the gate over-voltage $V_{ov} = V_{gs} -$

Device name	Test conditions	Charge per area ($\mathrm{nC/mm^2}$)
MIMC	V_{MIMC}=1.0 V	1.2
MIMC	V_{MIMC}=1.5 V	1.9
MIMC	V_{MIMC}=2.0 V	2.5
MIMC	V_{MIMC}=2.5 V	3.1
MIMC	V_{MIMC}=3.0 V	3.7
MIMC	V_{MIMC}=3.3 V	4.1
MIMC	V_{MIMC}=3.6 V	4.5
VFNDM50	$V_{gs,final}$=0.7 V, $V_{ds,initial}$=10 V	2.9
VFNDM50	$V_{gs,final}$=1.0 V, $V_{ds,initial}$=10 V	3.6
VFNDM50	$V_{gs,final}$=1.5 V, $V_{ds,initial}$=10 V	4.9
VFNDM50	$V_{gs,final}$=2.0 V, $V_{ds,initial}$=10 V	6.2
VFNDM50	$V_{gs,final}$=2.5 V, $V_{ds,initial}$=10 V	7.5
VFNDM50	$V_{gs,final}$=3.0 V, $V_{ds,initial}$=10 V	8.8
VFNDM50	$V_{gs,final}$=3.3 V, $V_{ds,initial}$=10 V	9.6
VFNDM50	$V_{gs,final}$=3.6 V, $V_{ds,initial}$=10 V	10.4
VFNDM50	$V_{gs,final}$=0.7 V, $V_{ds,initial}$=20 V	3.4
VFNDM50	$V_{gs,final}$=1.0 V, $V_{ds,initial}$=20 V	4.1
VFNDM50	$V_{gs,final}$=1.5 V, $V_{ds,initial}$=20 V	6.6
VFNDM50	$V_{gs,final}$=2.0 V, $V_{ds,initial}$=20 V	8.0
VFNDM50	$V_{gs,final}$=2.5 V, $V_{ds,initial}$=20 V	8.0
VFNDM50	$V_{gs,final}$=3.0 V, $V_{ds,initial}$=20 V	9.3
VFNDM50	$V_{gs,final}$=3.3 V, $V_{ds,initial}$=20 V	10.1
VFNDM50	$V_{gs,final}$=3.6 V, $V_{ds,initial}$=20 V	10.8
VFNDM50	$V_{gs,final}$=0.7 V, $V_{ds,initial}$=40 V	4.3
VFNDM50	$V_{gs,final}$=1.0 V, $V_{ds,initial}$=40 V	5.0
VFNDM50	$V_{gs,final}$=1.5 V, $V_{ds,initial}$=40 V	6.3
VFNDM50	$V_{gs,final}$=2.0 V, $V_{ds,initial}$=40 V	7.6
VFNDM50	$V_{gs,final}$=2.5 V, $V_{ds,initial}$=40 V	8.9
VFNDM50	$V_{gs,final}$=3.0 V, $V_{ds,initial}$=40 V	10.2
VFNDM50	$V_{gs,final}$=3.3 V, $V_{ds,initial}$=40 V	11.0
VFNDM50	$V_{gs,final}$=3.6 V, $V_{ds,initial}$=40 V	11.8

Table 3.3: Nominal charge per mm^2 for the MIMC capacitor at different voltages compared with charge required to reach final gate-source voltage $V_{gs,final}$ per mm^2 for N-type DMOS at different initial drain-source voltages $V_{ds,initial}$

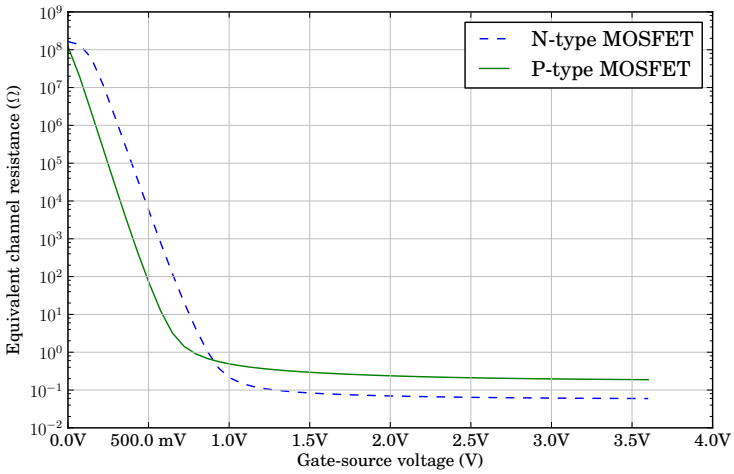


Figure 3.6: Channel resistance in function of gate-source voltage for 1 mm^2 N-type and P-type DMOS devices in the I3T50 Technology

V_{th}. The factor of 3 to 4 between the nominal supply voltage and the threshold voltage allows for a comfortable noise margin when the transistor is turned off to avoid unwanted conduction, while sufficient gate over-voltage can be applied to achieve a satisfactory current handling capability in the on-state [24]. In Figure 3.6, the equivalent channel resistance is plotted in function of the applied gate voltage for a $1\ \mathrm{mm}^2$ N-type and P-type DMOS in the I3T50 technology. For the N-type DMOS, this is a device with the maximum channel width of $10\ \mathrm{mm}$ and a multiplier of 20, for the P-type DMOS, this is a device with the maximum channel width of $10\ \mathrm{mm}$ and a multiplier of 16. It is immediately obvious from this plot that at gate voltages near the threshold voltage the channel resistance is several times larger than at the nominal supply voltage. Allowing the bootstrap voltage to drop significantly below the nominal supply voltage will lead to a reduced overdrive voltage, and therefore will either lead to increased conduction loss when the transistor width is not increased to compensate for this, or increased silicon area when the transistor width is adjusted. Even if we ignore the area required to implement the bootstrap capacitor for the N-type MOSFET, it is only reasonable to implement an N-type MOSFET as long as the equivalent channel resistance is less than a P-type MOSFET with equal area, which can be driven at an arbitrary gate voltage without a bootstrap capacitor, i.e. the nominal $3.3\ \mathrm{V}$ in the I3T50 technology. Therefore, we can derive from the graph that the bootstrap capacitor should be large enough to maintain at least $1\ \mathrm{V}$ on the gate, which is an over-voltage of approximately $200\ \mathrm{mV}$.

As previously mentioned, the gate charge required to reach this gate voltage depends on the drain-source voltage that needs to be switched, since the gate-drain capacitor is

responsible for a significant part of the gate charge. In the I3T50 technology, this gate charge requirement corresponds with a bootstrap capacitor that is between 1.24 and 1.72 times the area of the N-type DMOS, depending on the drain-source voltage, as can be derived from the charge at different voltages in Table 3.3.
Because both bottom metal layers are required to route the drain and source contacts away from the DMOS devices to satisfy the design rules, it is physically impossible to place the MIMC directly on top of the DMOS devices. Therefore, even integrating a minimal bootstrap capacitor that barely allows to turn on the N-type MOSFET multiplies the area requirement with a factor 2.24 to 2.72, while increasing the on-resistance of the MOSFET to a similar value as a P-type MOSFET. This completely negates the advantage of the higher mobility in the N-type MOSFET, while the reduced over-voltage (compared to a P-type MOSFET driven at or near the nominal gate voltage) makes the circuit much more susceptible to tolerances in fabrication and noise in the application, which could cause undesirable turn-on or turn-off of the N-type device. Therefore, when an external bootstrap capacitor is not possible for a certain application, it is typically the better choice to implement the high-side switches as P-type MOSFETs. This can be taken into account in the cost function by introducing a correction factor K_{hs} for the high-side switches, which corresponds with the reduced mobility of the P-type devices or the area required to implement a bootstrap circuit on the ASIC. Obviously, when an external bootstrap circuit is used, an N-type MOSFET is the obvious choice for the high-side switches and the correction factor can be either omitted or considered to be equal to 1.

3.6 Linear voltage regulators

A first category of voltage conversion circuits is the linear voltage regulator. As the name suggests, the operation of the linear voltage regulator is not based on active or passive elements that are either completely switched on or off, but rather on one or more active or passive elements that are used in the linear region. This is in contrast with all other categories that we discuss in this section, and even with the title on the front cover of this work. However, it is important to discuss this category, as it is the classic method to convert a DC voltage into a voltage that is suitable for the intended load, and provides a benchmark for the other categories.
The output voltage of the linear regulator is regulated by adjusting the operation point of an active or passive device that is used as one half of a voltage divider. A voltage divider is a linear circuit that produces an output voltage that is a function of the input voltage, i.e. for the circuit in Figure 3.7 the output voltage V_{out} in function of the input voltage V_{in} is given by:

$$V_{out} = \frac{Z_2}{Z_1 + Z_2} V_{in}$$

In the linear voltage regulators, either Z_1 or Z_2 is dynamically adjusted to maintain an appropriate output voltage. If Z_1 is dynamically adjusted, the adjustable element is in series with the load, and the linear regulator is classified as a *series* linear regulator. This

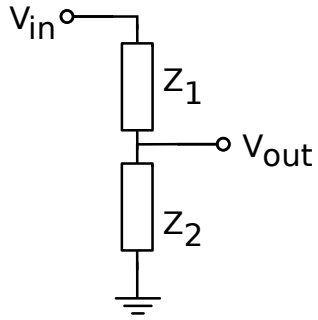


Figure 3.7: Voltage divider

is the most common type of linear regulator, especially if the regulator needs to be able to supply significant current levels. If Z_2 is dynamically adjusted, the adjustable element is in in parallel with the load, and the linear regulator is classified as a *parallel* or *shunt* linear regulator. Because the operating principle of this category of voltage converters is based on using components in the linear region, there is a voltage present over the device while simultaneously current flows through it, and some of the inherent weaknesses of the linear voltage regulators are a direct consequence of this. Primarily, the linear voltage regulators are limited to down-converting the voltage. It is impossible for any voltage divider to have a higher DC voltage at the output than at the input, and this also holds true for the linear voltage regulators. Secondarily, even using ideal components, the linear voltage regulator needs to dissipate power to regulate the output voltage. The theoretical maximum efficiency of a linear voltage regulator is given by:

$$\eta_{linear} = \frac{V_{out}}{V_{in}}$$

This implies that the minimum dissipated power P_{dis} in the linear voltage converter is given by:

$$P_{dis} = (V_{in} - V_{out}) \times I_{load}$$

Even for applications where the power efficiency is not considered to be critical, this limits the usability of the linear voltage converters to relatively low power applications. To ensure reliable operation of the converter, all the dissipated power needs to be transferred away from the converter without reaching excessive temperatures at the junctions in the semiconductor material. Depending on the semiconductor fabrication process and materials, parameter shift, and lifetime requirements, reliability concerns typically limit the maximum permissible junction temperature in silicon semiconductors to between $125\ ^\circ\mathrm{C}$ and $200\ ^\circ\mathrm{C}$ [25] [26]. Up to a dissipation of $1\ \mathrm{W}$ to $2\ \mathrm{W}$, it is possible to limit the junction temperature to these values using inexpensive packages and cooling by natural convection. A well-known example of this is the ubiquitous LM78XX family of linear regulators, where TO-220 packages without additional cooling can typically limit the junction temperature to $65\ ^\circ\mathrm{C}$ above the ambient temperature per $1\ \mathrm{W}$ of dissipation [27].

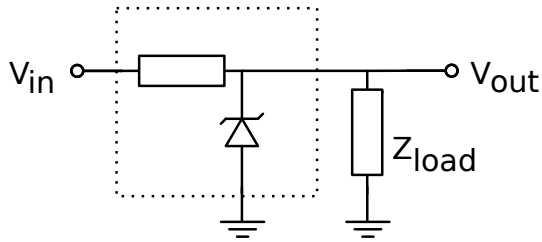


Figure 3.8: Shunt voltage regulator

3.6.1 Shunt linear regulator

In the shunt linear regulator, of which a possible implementation is shown in Figure 3.8, the voltage regulating element is in parallel with the load. In this implementation a Zener diode, which has the ability to maintain a relatively constant voltage over itself while a sufficiently large current is flowing through it in the (reverse) avalanche breakdown mode, is used as the parallel element. However, in some applications the parallel element can also be a number of diodes in series or an LED in forward bias, or an integrated circuit, e.g. with temperature compensation. The resistor is limiting the current through, and thereby the power dissipation in, the parallel element. In applications that are designed for a certain minimum current to be drawn from the voltage regulator it is possible that the chosen resistor value is too low to limit the current through the parallel element when the load is disconnected, leading to destruction of the parallel element when the load is removed. However, this same resistor also limits the maximum available output current, and the output voltage will tend to droop at increased output currents. Therefore, the accuracy of the output voltage, and the achievable output current range is relatively limited for a shunt linear regulator. Shunt linear regulators are typically used when little variation in the output current is expected, in applications such as voltage references, and where low cost and simplicity is more important than a large range of possible output currents. For applications where more output voltage accuracy or larger output currents are desirable, a series linear regulator is typically more appropriate.

3.6.2 Series linear regulator

In the series linear regulator, the impedance in series with the load is dynamically adjusted to maintain a more-or-less constant voltage at the output. A basic example of a series linear regulator is shown in Figure 3.9. In these voltage regulators, the impedance in series with the load is typically referred to as the pass transistor. The pass transistor can be implemented as an NPN Darlington pair, a single PNP or NPN bipolar transistor, or a P-type MOSFET, depending on the desired characteristics of the series linear regulator [28]. The classic implementation of the series linear regulator uses an NPN Darlington pair as the pass transistor, with a PNP driver to provide sufficient current to control the Darlington pair. To allow this type of regulator to maintain regulation of the output voltage, there is

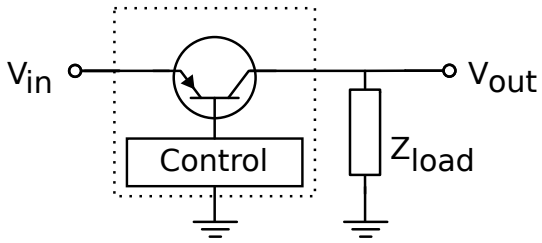


Figure 3.9: Series linear regulator

a relatively high (1.5 V to 2.5 V) minimum voltage difference between the input voltage and output voltage, since 2 base-emitter junctions need to be forward biased to allow the third transistor to reach saturation. This minimum voltage headroom difference is referred to as the dropout voltage, and is therefore given by:

$$V_{drop} = 2V_{be} + V_{sat}$$

In applications where this amount of voltage headroom is not available, such as in many battery-powered applications, the linear voltage regulator is typically implemented as a low-dropout (LDO) bipolar regulator or a quasi LDO bipolar regulator. In these (quasi) LDO bipolar regulators, the pass transistor is a single transistor, which allows the regulator to maintain output regulation with significantly lower voltage headroom.
In the case of the LDO bipolar regulator, a PNP transistor is used as the pass transistor, which limits the minimum dropout voltage to the saturation voltage of this transistor to:

$$V_{drop} = V_{sat}$$

Dropout voltages of $500\ \mathrm{mV}$ at full load are typical, and can be as low as $10\ \mathrm{mV}$ to $20\ \mathrm{mV}$ at light loads.
In the case of the quasi LDO bipolar regulator, an NPN transistor with a PNP driver is used as the pass element. Therefore, only one forward biased base-emitter junction is required to achieve saturation in the NPN transistor:

$$V_{drop} = V_{be} + V_{sat}$$

One may wonder why all three of these bipolar linear regulators are still broadly available, while the LDO seemingly performs the same function with significantly reduced voltage headroom requirements. The relevant parameter, which we have neglected until now in the comparison is the ground pin current (I_{gnd}), which is the part of the input current that is not contributing to the output current. This is electrical power that is provided by the source but not transferred to the output of the voltage regulator, and therefore needs to be dissipated in the regulator, which leads to increased power dissipation. A small part of the ground pin current is caused by biasing and leakage currents in the control circuit. However, the main part of the ground pin current is caused by the current that is required

to drive the pass element. Essentially, this is the output current divided by the gain (β) of the pass transistor. Therefore, a more realistic expression for the maximum efficiency of the linear converters is:

$$\eta_{linear} = \frac{V_{out}}{V_{in}} \frac{I_{out}}{I_{out} + I_{gnd}} = \frac{V_{out}}{V_{in}} \frac{\beta}{1+\beta}$$

Because of the high β of an NPN Darlington pair, very little current is required to drive the pass transistor, and the ground pin current can be as low as a few mA to drive several A load current [27].
The bipolar quasi LDO also has a relatively high β, and therefore reasonably limited ground pin current, e.g. the LM1085 can drive $3\ \mathrm{A}$ of load current with a ground pin current of less than $10\ \mathrm{mA}$ [29].
By contrast, bipolar LDO regulators only have the current gain of a single PNP transistor available, which can be as low as 15-20 at full load. Therefore, the ground pin current can be as high as 7 % of the load current, which is responsible for significant dissipation in the regulator for higher load currents [28].
Alternatively, the pass transistor can be implemented as a MOSFET instead of using one or more bipolar transistors. Since MOSFET devices are characterized by an equivalent on-resistance (R_{on}) of the channel instead of a saturation voltage when they are fully turned on, the voltage headroom for a certain load current can be made arbitrarily small by increasing the transistor size, which is inversely proportional to the on-resistance.

$$V_{drop} = R_{on} I_{load}$$

Obviously, increasing the transistor size proportionally increases the required silicon area, and therefore the cost of the linear regulator, so the voltage drop is dictated by economical and practical limits instead of inherent physical limitations of the bipolar devices. Because a MOSFET is a voltage controlled device instead of a current controlled device, as is the case for bipolar devices, the current gain in DC is essentially infinite and the ground pin current can be even further reduced than was the case for the Darlington pair. Despite combining both of these desirable characteristics, only a few MOSFET based linear regulators have reached the market. This is partially explained by the relatively high cost for discrete MOSFET voltage regulators, since MOS processes typically require more masks and more processing steps than a bipolar implementation. Also, somewhat more care is required to ensure stability of LDO MOSFET based linear regulators with respect to load current and external capacitance than is required for the more common non-LDO bipolar linear regulators [30].

3.6.3 Discussion

Since all linear regulators are based on the operating principle of dissipating the voltage differential between the input and output voltage, only some practical details such as the minimum voltage headroom, ground pin current, and the required output capacitance

differ between the different possible implementations of these converters. Therefore, we can lump all of them together for the evaluation as high-power monolithically integrated converters, using the three criteria we discussed at the beginning of this chapter: cost, space or area utilization, and power dissipation.

While it is true that linear regulators can be extremely cheap for low power applications, e.g. the suggested resale price for a Texas Instruments TLV700XX LDO is just 0.18 US$ in 1k unit quantities and is further reduced to 0.096 US$ in 100k unit quantities [31], this no longer holds true for higher power levels. Because of the inherent link between the efficiency and the ratio of the output voltage to the input voltage, a linear voltage regulator needs to dissipate a significant part of the output power. Using the typical cost-effective plastic IC packages, the dissipation on the silicon die is usually limited to a few W of dissipation when natural convection is used for cooling. Higher dissipation in a single plastic package is possible when using heatsinks and forced cooling, however these thermal solutions are expensive, heavy, require lots of PCB area and space, and because active cooling solutions have moving mechanical parts, are much more prone to failure than a solid state circuit that can be cooled by natural convection.

Therefore, high-power linear regulators score poorly on all three basic criteria for voltage converters: they are expensive, cumbersome and dissipate a lot of power. In fact, they need an input voltage that is higher than the output voltage to be able to work and need more input current than they can provide at the output, in some LDO implementations even significantly more so. Therefore, from the viewpoint of using a converter to optimize the energy distribution network by transporting the energy at high voltages and low currents and converting to a lower voltage and higher current near the point of load, linear regulators do not provide any advantages. However, we can see from the expressions for the efficiency of linear regulators that it is typical for voltage conversion to become less efficient for large differences between the input and output voltage.

3.7 Switching voltage converter topologies

In this section, we will give an overview of the different voltage conversion approaches that use transistors as switching elements. When using the transistors as switching elements rather than as a linear device, the dissipation in the transistors can be significantly reduced. In the theoretical analysis, where we consider the circuit components to be ideal, i.e. switches with a zero on-resistance, an infinite off-resistance, and zero switching time and energy, inductors with zero series resistance, the efficiency in all of these converters would be 100%. The only dissipation in switching converter circuits originate from the non-ideal properties of real-world components.

In order to achieve a voltage conversion without using transistors in the linear region, the semiconductor devices are used as switches to dynamically reconfigure the electrical circuits during each cycle. During a part of the switching cycle, electrical energy from the input is stored in one or more circuit elements, and during another part of the switching cycle this energy is released at the output. For an idealized converter, the amount of

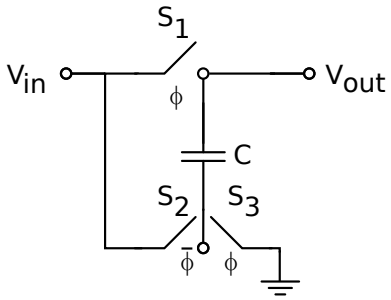


Figure 3.10: Basic voltage doubler

energy that is released is – in steady-state conditions – exactly equal to the amount of stored energy, which is often used in the analysis of the converter operation.

For solid state storage of electrical energy, only two possible storage forms exist: either the energy is stored in the electrostatic field of a capacitor or the energy is stored in the electromagnetic field of an inductor. For our discussion of the switching converters, we will use the energy storage form as the primary differentiating factor. We will first discuss the switched capacitor circuits, where capacitors are used as the energy storage elements, followed by the discussion of the switched inductor circuits, where inductors are used as the temporary energy storage element. Only three basic circuits that have the ability to perform voltage conversion between the input and output are possible using a single inductor, which is why we will discuss these topologies first. Other converters topologies are derived from these, either by replacing the inductor by coupled inductors or by adding a transformer. These transformer-isolated topologies will be discussed last. Since the switched inductor circuits, both non-isolated and transformer-isolated, will be the bulk of our discussion the voltage stress and RMS current for these converters is summarized in Table 3.4.

3.7.1 Switched capacitor

In switched capacitor converters, energy is stored in one or more capacitors, which can be connected in various series or parallel configurations through a number of actively or passively controlled switches. An elementary implementation of a voltage converter using switched capacitors is shown in Figure 3.10, where the input voltage is doubled using a single capacitor and three switches. The operation of this voltage doubler is as follows: during clock phase ϕ, switches S_1 and S_3 are closed and switch S_2 is open, and capacitor C is charged to V_{in}. During clock phase $\bar{\phi}$, switches S_1 and S_3 are open and switch S_2 is closed, which connects the bottom electrode of the capacitor to potential V_{in}. The capacitor retains its charge from the clock phase ϕ, so the charge on the capacitor is $V_{in}C$. Since $(V_{out} - V_{in})C = V_{in}C$ charge conservation requires $V_{out} = 2V_{in}$ during $\bar{\phi}$, as long as no load is connected to the output.

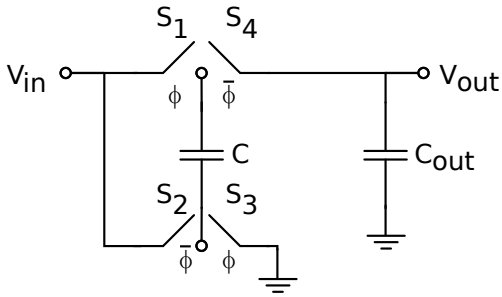


Figure 3.11: The Greinacher voltage doubler

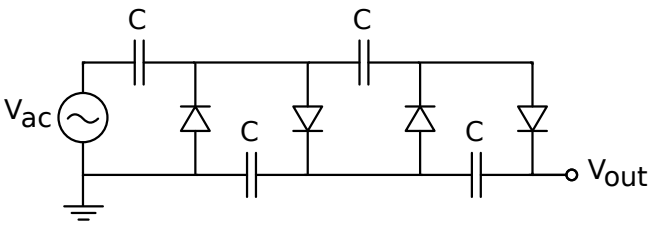


Figure 3.12: A 2-stage Greinacher/C-W voltage multiplier

A more practical voltage doubler, first described by Greinacher in 1914 [32] that can actually drive a load at the output is shown in Figure 3.11. In this circuit, capacitor C is also charged to V_{in} during phase ϕ, when switches S_1 and S_3 are closed and switches S_2 and S_4 are open. During clock phase $\bar{\phi}$, the charge on capacitor C is distributed over C and C_{out}, which gives a no-load output voltage:

$$V_{out} = 2\frac{C}{C + C_{out}}V_{in}$$

Other ratios between the input and output voltage are possible by cascading multiple capacitors in series. This was first shown in 1920 by Greinacher [33], when he generalized his earlier voltage doubler [32], and independently rediscovered in the 1930s by Cockcroft and Walton [34] in experiments with discrete high-voltage generators for particle physics. Cockcroft and Walton used the charge pump circuit throughout several decades of their research, which won them the Nobel Prize in Physics in 1951 [35]. Therefore, this type of charge pump is often referred to as the Cockcroft-Walton (C-W) voltage multiplier. To credit the original inventor, we will use the designation Greinacher/C-W multiplier. This type of charge pump can achieve extremely high voltages in discrete implementations (several 100 kV) because every element in the cascade only needs to withstand the input drive voltage. A 2-stage Greinacher/C-W multiplier is shown in Figure 3.12. The initial implementations of an n-stage Greinacher/C-W multiplier used an AC voltage source at the input, which results in an output voltage $V_{out} = 2n\sqrt{2}V_{in,RMS}$ for ideal components

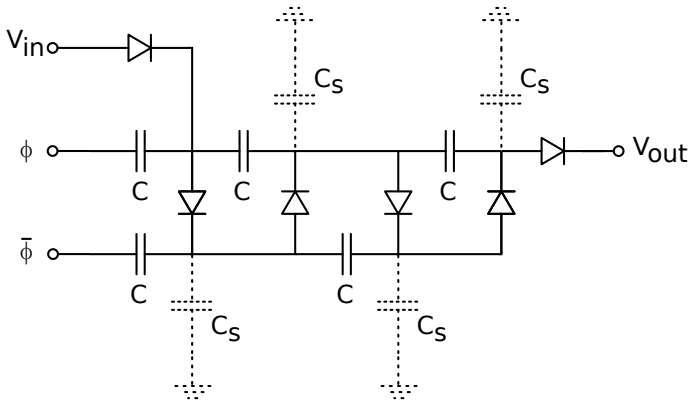


Figure 3.13: A clocked 2-stage Greinacher/C-W voltage multiplier, showing the stray capacitors to ground

and no-load conditions. However, it is also possible to operate the n-stage Greinacher/C-W multiplier from a DC voltage that is switched on and off. Essentially, this does not alter the operation and the output voltage under the same condition becomes: $V_{out} = nV_{in}$, with V_{in} the DC voltage that is switched on and off. For practical implementations however, when the converter needs to supply a load current, the voltage drop on the output rapidly increases with the number of stages, because of the impedance of the capacitors. When all capacitors are assumed to be equal, the output voltage is given by [36]:

$$V_{out} = nV_{in} - \frac{I_{out}}{fC}\left(\frac{2n^3}{3} + \frac{n^2}{2} - \frac{n}{6}\right)$$

An equivalent circuit for this 2-stage Greinacher/C-W multiplier that uses a DC input voltage and two complementary clock circuits is shown in Figure 3.13. On this figure, the stray capacitors to ground are shown. For a discrete implementation, the capacitors C are implemented such that $C_S \ll C$, which allows the voltage multiplier performance to be close to the ideal case. For a monolithic integration where the capacitors are integrated on the IC, it is much more difficult to ensure that the stray capacitors are sufficiently small, which compromises the voltage transformation abilities. Since only the first two coupling capacitors are directly driven by the clock signals ϕ and $\bar{\phi}$, the drive strength for all successive stages is reduced when the stray capacitors become comparable to the coupling capacitor value.

In practice, the output voltage of a monolithic Greinacher/C-W charge pump appears to be limited to approximately twice the input voltage, regardless of the number of stages [37]. An alternative charge pump, first described in 1975 [37] by Dickson overcomes many of the issues of the Greinacher/C-W charge pump. The Dickson charge pump he introduced, shown in Figure 3.14, or a variation thereof is still the de-facto standard for the on-chip generation of the appropriate voltages for non-volatile memories, such as flash and EEP-

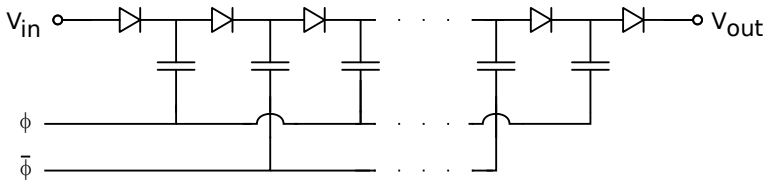


Figure 3.14: Dickson charge pump

ROM. The n-stage Dickson charge pump also generates an output voltage $V_{out} = nV_{in}$ under no-load conditions and for ideal components, but is significantly less susceptible to the number of stages and the influence of stray capacitors, since each stage is directly driven by clocks signals ϕ and $\bar{\phi}$. When taking into account the stray capacitors, output current, and rectifier voltage drop, the output voltage is given by:

$$V_{out} = V_{in} - V_r + n\left(\frac{C}{C + C_S}V_{in} - V_r - \frac{I_{out}}{fC}\right)$$

with V_r being the rectifier voltage drop, f the switching frequency and other symbols as previously defined.
However, since the capacitors in the Dickson charge pump are all in parallel instead of in series as in the Greinacher/C-W multiplier, the voltage over the capacitors increases with V_{in} at each successive stage, with the final capacitor seeing the full output voltage. The Dickson charge pump can be completely integrated on the chip, and is most commonly used to convert the supply voltage of the logic circuit, which can be as low as 0.85 V in modern (2013) EEPROM or Flash memories [38] to the voltage required to write and erase the non-volatile memory blocks or cells, which is in the order of 7 to 9 V for NOR flash and 15 to 17 V for NAND flash [39]. Other uses of these monolithically integrated Dickson charge pumps include the generation of bias voltages for Liquid Crystal Displays (LCD) bi-stable displays [40].

Discussion

Obviously, monolithically integrated charge pumps are already widely used to generate voltages higher than the input voltage. In the expression for the output voltage of both the Greinacher/C-W and the Dickson charge pump, we can see a negative term proportional to the output current. Essentially, this is the output impedance of the switched capacitor converter. For the Greinacher/C-W this term is in a first approximation proportional to the third power of the number of stages, so the available output current is severely limited by the voltage droop caused by the impedance of the converter. In the case of the Dickson charge pump, the output impedance increases linearly with the number of stages, and much more current is available at the output of the converter without excessive voltage droop. However, since the output impedance is in both cases also proportional to $\frac{1}{fC}$, and the switching frequency is limited by the switching related losses in the circuit, the output current is limited by the capacitor size.

For completely monolithically integrated converters, where the capacitors are to be integrated on the same IC as the semiconductor switches, the maximum available output current is limited by the size of the capacitors that can be economically integrated on the IC. Since it is fairly expensive in terms of silicon area to integrate significant capacitors on an IC, this will be the limiting factor in most applications. For the applications that were previously mentioned as popular applications for switched capacitor circuits, the required currents are typically in the order of μA, which is perfectly possible with capacitor sizes that are economical to integrate. For larger output currents, it becomes an economic and technical necessity to use external capacitors to achieve an output impedance of the converter that is sufficiently low.
Commercially available charge pump converters that use external capacitors appear to be limited to a peak output current of 0.3 A at a 5 V output voltage, i.e. an output power of 1.5 W [41] using a switching frequency of several hundreds of kHz and several tens of μF of ceramic capacitors.
For switching frequencies of several hundred kHz, only ceramic capacitors provide sufficiently low Equivalent Series Resistance (ESR) and can retain their capacitance at the switching frequency. Ceramic capacitors values over 100 μF are typically not offered by manufacturers of passive components [42] [43], since these are no longer considered to be cost-effective. Increasing the switching frequency to further reduce the output impedance leads to increased switching losses, and is also limited by the RC time constant of the switches and capacitors, to ensure the voltages on the switched capacitors can reach their steady-state voltages during the switch on-time.

3.7.2 Non-isolated switched inductor

The alternative for the temporary energy storage in the electrostatic field is energy storage in the electromagnetic field, i.e. by using an inductor instead of a capacitor. In capacitive energy storage, the maximum energy density per unit mass and unit volume is fundamentally limited by the dielectric strength, which is the maximum electric field that can be applied over the dielectric. In the case of inductive energy storage, the maximum energy density per unit mass and unit volume is in most cases limited by thermal limits in the conductor and core material. Depending on which abstractions are made in the calculations, the maximum energy storage density in an inductor is typically considered to be one to two orders of magnitude larger than the energy storage density in a capacitor.
Modern power electronics designers publish about switched inductor circuits operating in the order of ten(s) of kW [44, 45], and off-the-shelf commercial DC-DC converter modules for use in medical, military, and telecom equipment are rated at a peak output power of 1 kW to 2 kW [46]. Obviously, these power levels are only achievable using discrete inductors and discrete power transistors. Even though it is possible to integrate inductors with integrated circuit technology, either by defining a coil in one or more of the on-chip metal layers or by placing bondwires on the surface of the integrated circuit, the maximum output power that can be achieved is relatively low, in the order of μW using on-chip inductors and 300 mW using bondwire inductors [47]. The reason for the limited

output power using on-chip or bondwire inductors is the low quality factor Q, which is a measure for how close a real inductor is to an ideal lossless inductor. For an ideal losless inductor, the Q-factor is infinite at all frequencies. For a real inductor, the Q-factor is defined as:

$$Q = \frac{\omega L}{R}$$

with ωL being the inductive reactance at the frequency $f = \frac{\omega}{2\pi}$ and R being the equivalent resistance in the series model, which represents all the losses in the inductor. The inductance can be increased for a given coil structure by placing a ferromagnetic material in the vicinity of the coil. Because of the increased permeability of ferromagnetic materials compared to air, the magnetic field becomes proportionally larger, and the inductance can be increased by a factor of several thousands. However, this increased inductance comes at the cost of core losses and non-linear behaviour. For an air-core inductor, the R as a loss factor is the resistance of the conductor that is used to construct the coil, taking into account the skin effect at high frequencies. If a ferromagnetic material is used to boost the inductance the R also includes the loss components in the core material caused by hysteresis and eddy-currents, which are highly frequency dependent.
Since ferromagnetic materials are not available in standard semiconductor processes, they are not often used in the construction of on-chip inductors. Most on-chip inductors are implemented as a spiral geometry without magnetic materials to increase the inductance, and typically achieve inductance density values in the order of $100\ \mathrm{nH/mm^2}$.
Recently, thin film deposition of magnetic materials and conductors after the standard semiconductor processing have been demonstrated, which allow for higher inductance density values. The maximum value reported in literature is $1700\ \mathrm{nH/mm^2}$, however these deposition processes are not part of standard semiconductor processing and therefore expensive, and not yet available outside of highly specialized research facilities. Also the Q-factor of these high density inductors is typically less than 10 [48], which may be sufficient for use in RF integrated circuits and wireless communications, but is relatively low for efficient power conversion applications, as this will lead to significant dissipation in the inductor's conductor and ferromagnetic material.
Bond wire inductors typically achieve values of $1\ \mathrm{nH/mm}$ length, and are limited by both the chip dimensions and the area on the chip that can be sacrificed to additional bondpads for every drawn loop. Typical values for bondwire inductors are in the order of $10\ \mathrm{nH}$ to $100\ \mathrm{nH}$ with a Q-factor in the 20–50 range [49, 50].
Switched inductor converters that use bondwire inductors for power levels up to $300\ \mathrm{mW}$ have been shown in literature [47]. Because the inductors become the limiting factor in the design of higher power converters, we limit ourselves to converters with external (off-chip) magnetics. In the following sections, we will evaluate each of the switched inductor circuits based on the cost function we defined earlier.

The buck converter

The first switched inductor converter circuit we will discuss is the buck converter, shown in Figure 3.15. This circuit consists of 2 switches: the first switch needs to be actively

switched on and off and is drawn as a MOSFET, while the other switch needs to allow current flow in one direction and block a voltage in the other direction and is drawn as a diode. As mentioned in section 3.3.2, in many practical applications this diode will be implemented as a synchronous rectifier to improve the circuit efficiency.
The basic concept for this converter is as follows: starting from an open switch and no current flowing in the circuit, the switch is closed. The voltage over the inductor is then $V_L = V_{in} - V_{out}$, and because of the inductor reluctance this causes an increase in inductor current i_L, governed by the equation $V_L = L\frac{di_L}{dt}$ as long as the switch is closed. Typically it is assumed that the capacitor at the output is sufficiently large to ensure the change on the voltage V_{out} is negligible over one switching period, so the increase in current is linear.
When the switch is opened, the inductor reluctance forces the current to keep flowing through the inductor. With the switch opened, the only remaining path for the current is through the rectifying device. If the rectifying device is implemented as a diode, the diode can only start conducting when the switching node voltage is one diode forward voltage drop below ground.
Similarly, for a synchronous rectifier, the switching node is pulled to ground by the active device, minus the voltage drop over the device for the current in the inductor. The voltage over the inductor then becomes $V_L = -V_{out} - V_R$, with V_R the voltage drop over the rectifier in the forward conduction operating point. This inductor voltage polarity is reversed, which causes the current in the inductor to decrease. If the output voltage is assumed to be constant during the switching cycle, this decrease in current is also linear. For a converter in steady-state operation, the magnitude of the increase during the on-time and the decrease during the off-time of the inductor should be equal and opposite, and from this the relation between the input voltage, the output voltage and the duty cycle δ, the ratio of the switch on-time T_{on} to the switching period T : $\delta = \frac{T_{on}}{T}$ can be derived. For the full derivation, the reader is referred to any power converter handbook [51, 52]. It can be shown that the relation between the input voltage and the output voltage is given by:

$$\begin{cases} V_{out} = \delta V_{in} \text{ in continuous conduction mode} \\ \\ V_{out} = V_{in} \dfrac{1}{\dfrac{2LI_{out}}{\delta^2 V_{in} T} + 1} \text{ in discontinuous conduction mode} \end{cases}$$

The buck converter operates in continuous conduction mode when there is current flowing through the inductor at each point in time during the switching cycle, and in discontinuous conduction mode when the current through the inductor becomes zero at any point during the switching cycle. The transition between these modes occurs when the current falls to exactly zero when the switch is turned back on for the next cycle. At this point, the converter satisfies both equations, and is said to be in border conduction mode. Typically, buck converters are designed to be in either continuous conduction mode or, more rarely, border conduction mode at full load. In most cases, the size, weight and cost of the inductor are prohibitive to operate a high-power converter in the discontinuous mode over

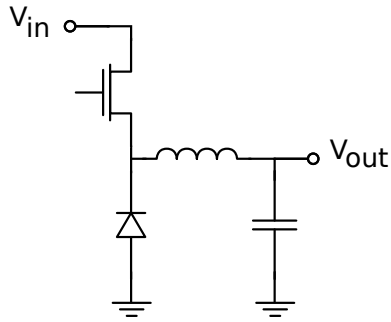


Figure 3.15: Buck converter circuit

the entire load range.
As can be seen from the equations, the output voltage of a buck converter is always lower than the input voltage. However, when we observe the voltage stress on the devices in the circuit, both the switching device and the rectifying device need to be able to block the full input voltage of the converter when they are in the off-state. For continuous conduction mode, which is the relevant condition for full load conditions, the RMS current through the switch and diode is approximated by a DC current that is flowing through the device for the on-time of the device, and no current flowing during the off-time. The approximate RMS current in function of the output current can then be calculated by:

$$I_{RMS,switch} = I_{out}\sqrt{\delta}$$

$$I_{RMS,rectifier} = I_{out}\sqrt{1-\delta}$$

For $\Delta I_{out} \ll I_{out}$, with ΔI_{out} the ripple on the output current which is determined by the inductor value, the duty cycle, the output voltage, and the switching frequency.
If the ripple on the output current is significant compared to the output current, the current waveform is more accurately described by a trapezoid, and the expression for the RMS current becomes:

$$I_{RMS,switch} = \sqrt{\left(I_{out}^2 + \frac{\Delta I_L{}^2}{12}\right)\delta}$$

$$I_{RMS,rectifier} = \sqrt{\left(I_{out}^2 + \frac{\Delta I_L{}^2}{12}\right)(1-\delta)}$$

However, even with a relative ripple $\frac{\Delta I}{I_{out}}$ of nearly 50 %, the simpler expression is in error by just 1 % and the more complex expression does not provide additional information when comparing converters with similar specifications, so we will use the simpler expression for the comparison of different converter topologies.

Because the RMS current for both switching devices in the buck converter is not equal, except in the case where $\delta = 0.5$, i.e. when $V_{out} = \frac{V_{in}}{2}$, the optimum on-resistance and size for both switching devices is not equal. The optimum is reached when the conduction loss per silicon area (in $\mathrm{W/mm^2}$) is equal for both devices and equal to the total conduction loss per the total silicon area. In many applications of high power hybrid converters, it is attractive to use an external bootstrap circuit and implement both the low side and high side switch as N-type MOSFETs to minimize the required silicon area. The following derivation of the optimal area distribution between switch and rectifier assumes this is the case. If the high side MOSFET is implemented as a P-type MOSFET or as an N-type MOSFET with integrated bootstrap, the correction factor K_{hs} we mentioned earlier for the high side switches is required.
Starting from $R_{on} = \frac{kV_{ds,max}^{2.5}}{S}$, we need to satisfy:

$$\frac{P_{total}}{S_{total}} = \frac{P_{switch}}{S_{switch}} = \frac{P_{rectifier}}{S_{rectifier}}$$

Filling in the RMS current and the on-resistance in $P = RI_{RMS}^2$:

$$\frac{P_{total}}{S_{total}} = \frac{kV_{ds,max}^{2.5} I_{out}^2 \delta}{S_{switch}^2} = \frac{kV_{ds,max}^{2.5} I_{out}^2 (1-\delta)}{S_{rectifier}^2}$$

Simplifying this equation leads to :

$$\frac{S_{switch}}{S_{rectifier}} = \sqrt{\frac{\delta}{1-\delta}}$$

With $S_{total} = S_{switch} + S_{rectifier}$, the optimal area distribution for switch and rectifier is:

$$S_{switch} = \frac{S_{total}}{1 + \frac{1}{\sqrt{\frac{\delta}{1-\delta}}}}$$

$$S_{rectifier} = \frac{S_{total}}{1 + \sqrt{\frac{\delta}{1-\delta}}}$$

The boost converter

In the boost converter, shown in Figure 3.16, the same components are used as in the buck converter, but are arranged differently. When the switch is closed in a boost converter, the input voltage is placed over the inductor $V_L = V_{in}$, causing the inductor current to increase linearly according to $V_L = L\frac{di_L}{dt}$. Once the switch is opened, the current in the inductor can not abruptly change because of the reluctance. The only remaining current

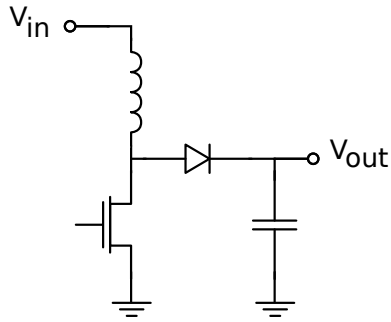


Figure 3.16: Boost converter circuit

path is through the rectifier, which is either a diode that can only conduct when it is forward biased with at least V_R, or is an active device used as a synchronous rectifier that causes a voltage drop V_R , so the inductor forces a voltage $V_{out} + V_R$ on the switching node. While the rectifier is conducting, the voltage over the inductor is $V_L = -V_{out} - V_R + V_{in}$.
To satisfy the inductor Volt-second balance, this second voltage needs to be negative, so the amplitude of the output voltage of a boost converter is invariably larger than the input voltage, which is confirmed by the full expressions for the output voltage:

$$\begin{cases} V_{out} = V_{in}\dfrac{1}{1-\delta} \text{ in continuous mode} \\ \\ V_{out} = V_{in}\left(1 + \dfrac{V_{in}\delta^2 T}{2LI_{out}}\right) \text{ in discontinuous mode} \end{cases}$$

As with the buck converter, the discontinuous operating mode is only relevant at light loads. If we make the same approximation as in the buck converter that the effect of the ripple on the DC value of the current is negligible, the RMS current in both devices in function of the output current is given by:

$$I_{RMS,switch} = I_{out}\sqrt{\delta}\frac{V_{out}}{V_{in}}$$

$$I_{RMS,rectifier} = I_{out}\sqrt{1-\delta}\frac{V_{out}}{V_{in}}$$

For the boost converter, the output voltage is higher than the input voltage, and both the switch and rectifier need to be able to block the full output voltage in their off-state. Since the boost converter can only create an output voltage higher than the input voltage, at a proportionally reduced output current, the boost converter is not really relevant from an efficient energy-distribution viewpoint.

The buck-boost converter

The buck-boost is the third possible permutation for the same circuit elements that are used in the buck converter and the boost converter, and is shown in Figure 3.17.
As with the buck converter and the boost converter, the operation of the buck-boost converter is also best explained by observing the voltage over the inductor during the different stages of operation. While the switch is closed, the input voltage is placed over the inductor $V_L = V_{in}$, causing the inductor current to increase linearly $V_L = L\frac{di_L}{dt}$. When the switch is opened, the inductor reluctance forces the current to keep flowing, and the rectifier needs to start conducting. For the rectifier to conduct, the switching node potential needs to be at $V_{out} - V_R$. Since in this circuit the switching node potential is the voltage over the inductor, and steady-state operation requires that the inductor Volt-second balance is zero, the voltage polarity of $V_{out} - V_R$ needs to be opposite to the voltage polarity of V_{in}. Therefore, the buck-boost converter always generates a negative voltage from a positive input voltage. The expressions for the output voltage are:

$$\begin{cases} V_{out} = V_{in}\dfrac{-\delta}{1-\delta} \text{ in continuous mode} \\ \\ V_{out} = -\dfrac{V_{in}^2\delta^2 T}{2LI_{out}} \text{ in discontinuous mode} \end{cases}$$

As can be seen from these expressions, the buck-boost converter can generate output voltages with an absolute value that can be either smaller or greater than the input voltage, depending on the duty cycle, but with an inverted polarity. The RMS current through the devices in function of the output current is:

$$I_{RMS,switch} = I_{out}\frac{\sqrt{\delta}}{1-\delta}$$

$$I_{RMS,rectifier} = \frac{I_{out}}{\sqrt{1-\delta}}$$

Both the switch and the rectifier must be able to withstand a voltage stress $V_{stress} = V_{in} + |V_{out}|$.

Other non-isolated topologies

Besides the three basic switched inductor topologies that have been mentioned before, other non-isolated topologies exist but are much less commonly used. The best known are the Ćuk converter, the SEPIC converter and the Zeta converter, where two inductors and a capacitor are combined for the energy storage instead of a single inductor. In certain applications, these alternative switched inductor topologies show desirable properties, such as a reduced output current ripple, continuous input and/or output current, being able to perform an up-conversion and a down-conversion without a polarity inversion, etc.

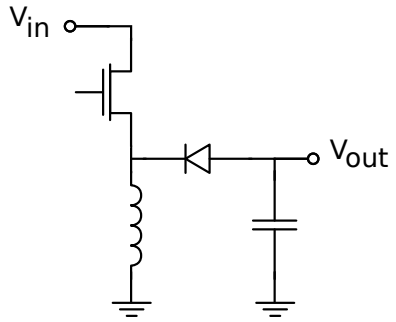


Figure 3.17: Buck-boost converter circuit

In these alternative converters, the RMS current through the devices and the voltage stress is at least equal to the RMS current and voltage stress in the basic topologies that perform the same voltage conversion ratio [53]. Therefore, in terms of our semiconductor cost function which only takes into account the primary characteristics of power dissipation and silicon area, which is equivalent with cost in monolithically integrated converters, these will not perform better than the basic topology from which they are derived. We will therefore not discuss these converters in detail.

3.7.3 Transformer-isolated switched inductor converters

In all of the non-isolated switched inductor converters that we discussed earlier, the input and the output voltages are linked through the duty cycle, which leads to some limitations in the design of the converters. For converters with a relatively large conversion ratio, this hard link between the input and the output voltage leads to either very small or very large duty cycles for the switch and for the rectifier. Because the voltage stress and the RMS current quickly increases to be able to perform the voltage conversion for a given load current when extreme duty cycles are used, the non-isolated converter circuits suffer from large conduction losses when the ratio between input and output voltage is far from unity. The use of these extreme duty cycles is thus inefficient at best and can even be the limiting factor for the maximum switching frequency, since the transition between the on-state and the off-state of the switches and rectifiers can not be made infinitely fast.
Below a certain minimum on-time, which depends on the power switch and the driver circuit, the switches are not sufficiently long in the on-state compared to the transitions and they start to behave more as linear devices than as switches, which includes more losses in the power devices and invalidates the assumptions made for the analysis of the switching converters. In this section, we will discuss the transformer-isolated converters, where an additional degree of freedom is introduced by the transformer turns ratio. The transformer turns ratio removes the hard link between the duty cycle, input voltage, and output voltage, so the duty cycle can be optimized by selecting an appropriate transformer turns ratio. Additionally, in many applications galvanic separation between the input and the

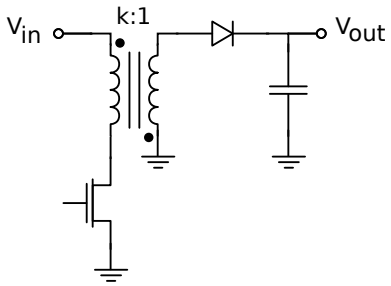


Figure 3.18: Flyback converter circuit

output of the converter is a safety requirement anyway, so no additional cost is introduced by choosing a transformer-isolated topology. In what follows, we will discuss the different possible implementations in significant detail, since this category of converters will prove to have very desirable characteristics for high-power high-voltage monolithically integrated converters.

Flyback converter

The first transformer-isolated converter that we will discuss is the flyback converter, which is derived from the buck-boost converter topology with a split inductor, and is shown in Figure 3.18. Although the schematic of the flyback converter shows two inductors coupled by a core, which typically is used to represent a transformer, the flyback transformer is not used as a transformer in the classical understanding of the operation of a transformer. Typically, a transformer is expected to use two or more windings on the same magnetic core to momentarily transfer energy from one winding to another using the electromagnetic field in the core, and any energy storage in the transformer is considered to be an unwelcome side-effect that is minimized as much as possible. In other words, in the classical transformer a current flows simultaneously in multiple windings, multiplied or divided by the transformer turns ratio as appropriate. However, the flyback transformer is more appropriately described as two inductors that are coupled by sharing a single magnetic core, as the flyback converter circuit prohibits the simultaneous flow of current through both windings.

During the switch on-time, the input voltage is placed over the primary inductor, causing a linear increase in inductor current and magnetic flux in the transformer, and thus storing energy in the transformer core. Because of the placement of the diode in the secondary side and the orientation of the transformer windings (note the dot notation on the transformer in Figure 3.18), no current can flow in the secondary side inductor and rectifier while the primary switch is closed. When the primary switch is opened, the magnetic field in the inductor core can not momentarily collapse and requires an alternative current path. At the primary side, no such path is available, and the current can no longer flow in the winding on the primary. On the secondary side, the current can flow through the diode

into the load if the secondary side voltage is at least $V_{out} + V_R$, which allows the energy that is stored in the magnetic field of the transformer core to be transferred to the output of the converter. Because of the transformer operation, the output voltage multiplied with the transformer ratio is imposed over the primary side inductor, which needs to be added to the input voltage to determine the voltage stress on the primary side switch. Therefore, the voltage stress on the primary side switch is given by:

$$V_{stress,switch} = V_{in} + kV_{out} = V_{in}\left(1 + \frac{\delta}{1-\delta}\right)$$

with k the transformer turns ratio. Similarly, while the primary side switch is conducting, the rectifier on the secondary side needs to block the sum of the output voltage and the transformed input voltage, and the voltage stress on the rectifier is given by:

$$V_{stress,rectifier} = V_{out} + \frac{V_{in}}{k}$$

Because of the low component count, which keeps the cost and size of the converter low, the flyback converter is the default choice for the lower power range (sub 100 W) discrete converter applications. Although the relatively high voltage stress and high peak currents in the devices limit the efficiency, the flyback converter is often considered to be the best compromise between size, cost and efficiency for discrete converter applications.
For a CMOS monolithically integrated converter, where the voltage stress on the integrated power devices is a crucial parameter for an efficient implementation, the flyback converter shows a relatively high voltage stress on both the primary and secondary devices, which makes it unlikely that a flyback converter will be the most appropriate choice, even at low power levels.

Forward converter

The forward converter topology is based on the buck converter topology, with an added transformer to provide galvanic isolation and allow for large ratios between the input and output voltages without using extreme duty cycles. In discrete converters, the forward topology is typically used for medium power converters, between approximately 100 W and 1000 W. The main reason for this is the increased component count, and thus size and cost of the forward converter, which is typically only justified for converters where the increased efficiency when compared to the flyback converter becomes a desirable property. The forward converter derives its name from the transformer utilization: the transformer core is used single-ended, where energy is only transferred in one direction of the core magnetization characteristic. Since the average Volt-second product of the transformer windings needs to be zero, all forward converter circuits need a core-reset mechanism that applies the required negative volt-seconds on the transformer core to avoid core saturation. A number of variations on the reset mechanism of the forward converters have been devised over the years, each with their own advantages and disadvantages of possible duty cycles and voltage stress. The classic 1-Transistor (1T) forward converter circuit

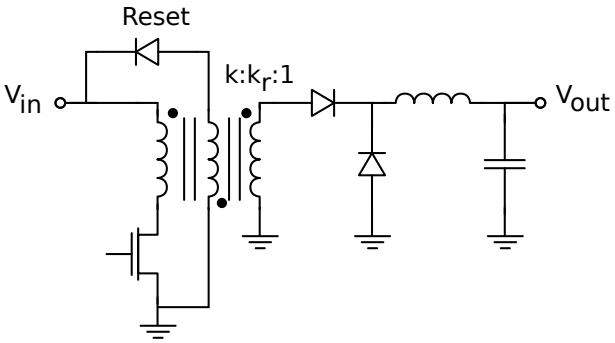


Figure 3.19: 1-Transistor forward converter circuit with a transformer reset winding

with a transformer reset winding is shown in Figure 3.19. In the forward converter with a transformer reset winding, the transformer core is reset by an auxiliary winding on the core, placed in anti-parallel with the primary winding. Since the auxiliary reset winding is only used to apply the transformer reset voltage and does not need to contribute to the load current, this auxiliary winding can be wound on the core using relatively fine wire compared to the current-carrying windings, so it does not significantly add to the dimensions of the transformer. However, the magnetic coupling between the primary winding and the reset winding should be as good as possible, and the reset winding is therefore typically wound together with the primary. This does complicate the fabrication of the transformer and increases cost.

While the switch is turned off, this auxiliary winding allows the magnetic flux in the core to be reset by providing a conducting path through the reset diode, which forces the input voltage on the reset winding. The reset diode will conduct as long as there is a magnetic field present in the core and the switch is not turned on. Depending on the turns ratio between the primary winding and the reset winding, the requirement for the transformer core Volt-second balance to be zero will limit the maximum duty cycle of the converter and will determine the voltage stress on the primary side switch. For a 1:1 turns ratio ($k = k_r$), the duty cycle δ_{max} is limited to 0.5 ($50\ \%$), and the voltage stress on the switch is twice the input voltage. The more general expression is:

$$V_{stress,switch} = V_{in}\left(1 + \frac{k}{k_r}\right) = V_{in}\left(1 + \frac{\delta_{max}}{1 - \delta_{max}}\right)$$

Because of the relation between the transformer primary and reset turns ratio and the maximum duty cycle, the voltage stress on the switch in the 1T forward converter quickly becomes unmanageable for duty cycles of more than approximately 0.7, where the voltage stress on the switch is already well over 3 times the input voltage.

Since a larger allowable duty cycle reduces the RMS current in the switch and simultaneously increases the voltage stress on the switch, there is a significant efficiency trade-off to consider in selecting a duty cycle over $50\ \%$ for the 1T forward converter.

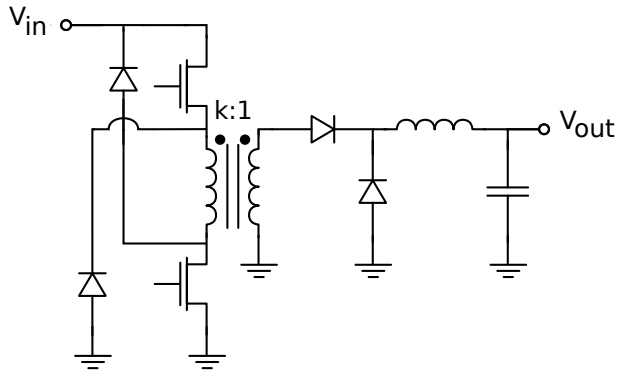


Figure 3.20: 2-Transistor Series forward converter circuit

To overcome this limitation, a 2-Transistor (2T) version of the forward converter circuit, shown in Figure 3.20 was introduced in the 1970's [54]. In literature, this variation of the forward converter is simply referred to as the 2T forward converter, however to avoid confusion with other forward converters that use 2 transistors, we will refer to this type of converter as the 2T *Series* forward converter. The 2T series forward converter circuit uses 2 switches and 2 diodes. During the on-time both switches, which are in series with the primary side of the transformer are turned on simultaneously to provide the forward voltage for the transformer primary. At the end of the on-time, both switches are simultaneously turned off, and the transformer reluctance forces both diodes to conduct, which inverts the voltage over the transformer primary and allows the magnetic field in the core to collapse. Since the 2 diodes are only used in the transformer core reset, the current in these devices is limited. This approach does not require an auxiliary winding, which reduces the winding cost of the transformer. However, in order to achieve a zero Volt-second balance on the transformer, the duty cycle for the 2T series forward converter is limited to 0.5. Although the duty cycle in the 2T series forward converter is more limited than in the 1T forward converter, and the RMS current will be higher, the voltage stress on all devices in the 2T series forward converter is limited to V_{in}. This significant reduction in voltage stress more than compensates for the need to use 2 switching devices that can handle the load current transformed to the primary side.

An alternative 2T forward converter was first presented in 1981 [55], the 2T active clamp forward converter, which is shown in Figure 3.21. In this circuit, the transformer reset is achieved by an auxiliary switch and a capacitor. The auxiliary switch is driven by a complementary signal to the main switch, which provides a conductive path for the core magnetic field to discharge when the main switch is turned off. By using a capacitor for the reset, charge balance in steady-state automatically maintains the appropriate voltage for the transformer core reset on the capacitor. To achieve a zero Volt-second balance, the

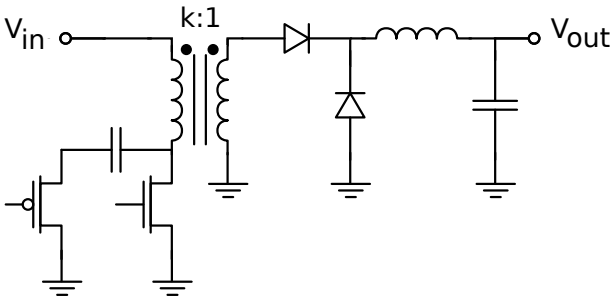


Figure 3.21: 2-Transistor active clamp forward converter circuit

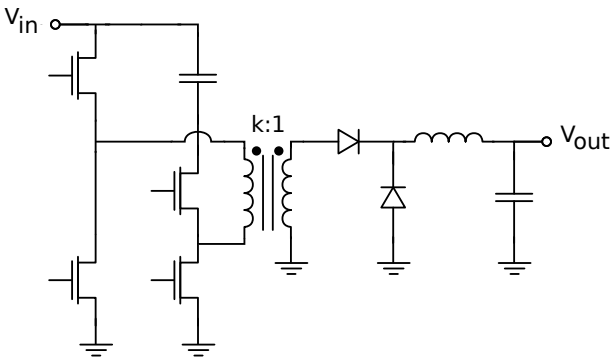


Figure 3.22: Optimized 4-Transistor active clamp forward converter circuit

capacitor voltage V_c in function of the duty cycle is:

$$V_c = \frac{V_{in}}{1-\delta}$$

In the 2T active clamp forward converter, the voltage stress on the switching devices is:

$$V_{stress} = V_{in}\frac{\delta}{1-\delta}$$

In an initial effort to optimize the integration of high-power DC-DC converters, several 4T versions of the 2T active lamp forward converter were proposed [56]. The main improvement in the 4T versions is the reduced required reverse blocking voltage of the switches, and the absence of voltages that are negative compared to the ground voltage.

The optimized 4T active clamp forward converter circuit is shown in Figure 3.22. For this 4T active clamp forward converter, the voltage stress on the switching devices on the

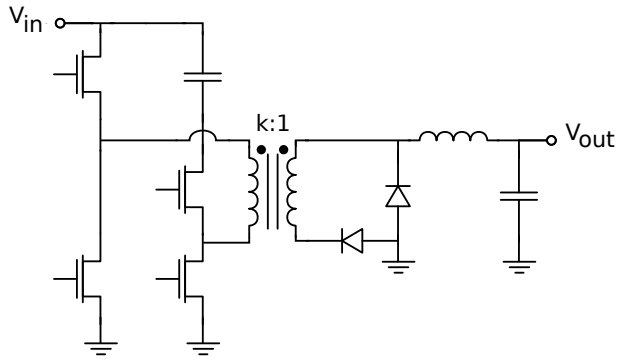


Figure 3.23: Optimized 4-Transistor active clamp forward converter circuit with secondary side rectifiers optimized for integration

primary side is:

$$\begin{cases} V_{stress} = V_{in} \text{ for } \delta \leq 0.5 \\ V_{stress} = V_{in}\dfrac{\delta}{1-\delta} \text{ for } \delta \geq 0.5 \end{cases}$$

Additionally, there are a number of possible implementations for the secondary side of the forward converter topology. In all previous illustrations of the forward converter, we have shown the classical representation of the forward converter secondary, where one rectifier is in series with the high-side of the transformer secondary to conduct during the power transfer phase, and a second rectifier provides a free-wheeling path for the current through the output inductor during the transformer reset phase.
However, for implementation of the forward converter in a smart-power technology, it is more appropriate to implement the power transfer rectifier in series with the low-side of the transformer secondary, which does not change the operation of the secondary side of the converter. However, this change allows both rectifiers, which are preferably implemented as N-type MOSFET synchronous rectifiers to have their source contact connected to ground. The 4-Transistor active clamp forward converter with the optimized placement of the secondary side rectifiers is shown in Figure 3.23. Both devices can then be driven as low-side switches, which simplifies the driving scheme and eliminates the need for bootstrap circuits [57], and no circuit node becomes more than a diode drop negative with regard to ground, which is essential for an efficient integration in a cost-effective smart-power technology. The voltage stress on both synchronous rectifiers is not necessarily equal. The freewheeling rectifier is in the off-state while power is being transferred from the primary side to the load and is blocking the input voltage transformed to the secondary side. The forward rectifier is in the off-state while the freewheeling rectifier is conducting and the primary side of the transformer is being reset by the clamp capacitor. Therefore, the voltage stress for the forward rectifier is the reset voltage transformed to the secondary

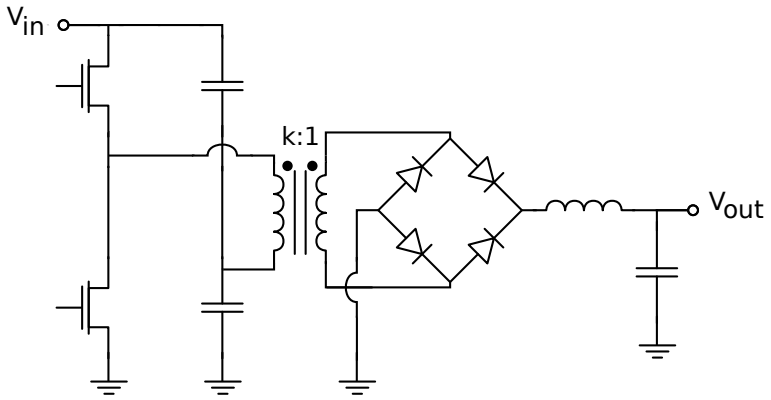


Figure 3.24: Half bridge converter with a full bridge secondary side rectifier

side:

$$V_{stress,forward} = \frac{V_{in}}{k}\frac{\delta}{1-\delta}$$

$$V_{stress,freewheeling} = \frac{V_{in}}{k}$$

The RMS current through the devices in function of the output current is:

$$I_{RMS,forwarddiode} = I_{out}\sqrt{\delta}$$

$$I_{RMS,freewheelingdiode} = I_{out}\sqrt{1-\delta}$$

Half bridge converter

In the half bridge converter topology, the primary side of the transformer is connected between a complementary pair of switches and a capacitive voltage divider, both connected between ground and the input voltage, as shown in Figure 3.24. The complementary switches alternate between connecting their common node to ground and the input voltage, while the common node of the capacitive voltage divider is at half of the input voltage. When the high-side switch is turned on, the voltage over the transformer primary is half the input voltage, and when the low-side switch is turned on, the voltage over the primary is also half the input voltage, but with an inverted polarity. Thus, the voltage over the primary alternates between $\frac{V_{in}}{2}$ and $-\frac{V_{in}}{2}$. Therefore, the voltage stress at all nodes in the primary is limited to the input voltage, independent of the duty cycle δ.

$$V_{stress,primary} = V_{in}$$

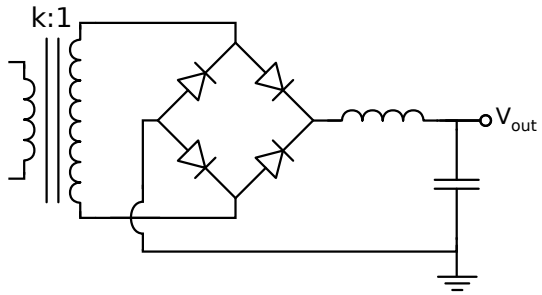


Figure 3.25: Full bridge rectifier for double ended topologies

The RMS current through each of the primary side devices is:

$$I_{RMS,primary} = \frac{I_{out}}{k_{HB}}\sqrt{\delta}$$

The major difference with the forward converter is that in this topology the transformer core magnetization is used in both directions for energy transfer. This removes the duty cycle limitations that were imposed by the transformer reset mechanism in the forward converter, which allows for a more efficient transformer and output filter design. By using both directions for the core magnetization in the energy transfer, there are two energy transfer phases per switching cycle instead of just one in the single ended topologies such as the forward converter. Viewed from the output filter of the converter this is equivalent with a single ended converter operating at twice the switching frequency, which reduces the demands on the output filter to achieve a similar current and voltage ripple. Under optimum conditions, a double ended converter can directly transfer energy from the input of the converter to the output for nearly the entire switching cycle, where the energy transfer in the forward converter is in practice limited to 50 % to 70 % of the time, depending on the transformer reset mechanism that is used.
However, to allow for the energy transfer to be possible in both excitation directions of the transformer magnetization, the secondary side can no longer be made from a single rectifying device as in the flyback converter or a single rectifying device combined with a freewheeling device as in the forward converter. To allow both the energy from the forward and reverse transformer magnetization to be transferred to the output, a full wave secondary is required. Because the forward and reverse magnetization need to be identical to provide a zero Volt-second balance on the transformer primary, the rectifying devices will also need to be symmetrical. Different implementations of a full wave secondary are possible, and these will be discussed next.
A first possible implementation of a full wave secondary is a full bridge secondary, as shown in Figure 3.25. In the full bridge secondary, we can distinguish the power transfer phases and the freewheeling phases. During the power transfer phases, two of the four devices are activated, while two other devices are blocking half the input voltage divided by the transformer turns ratio k_{HB}. During the freewheeling phases, a conductive path

can be formed by either turning on all 4 devices, or keeping the 2 devices that were previously conducting on, and the other 2 devices off. Since the transformer secondary voltage is zero in the freewheeling phase, the devices that are turned off do not need to block a voltage. Therefore, the voltage stress for the full bridge rectifier is given by:

$$V_{stress,secondary} = \frac{V_{in}}{2k_{HB}}$$

The RMS current through each of the secondary side devices during the power transfer phase in the full bridge secondary is:

$$I_{RMS,secondary(powertransfer)} = I_{out}\sqrt{\delta}$$

If all devices are turned on simultaneously during the freewheeling phase in the full bridge secondary, each of the devices is carrying half the output current during each of the freewheeling phases. In that case, the freewheeling RMS current through each of the secondary side device in the full bridge secondary is:

$$I_{RMS,secondary(freewheel)} = \frac{I_{out}}{2}\sqrt{1-2\delta}$$

Because both of these RMS current components are occurring at a different time in the same device, they are orthogonal and the total RMS current for each of the secondary devices in the full bridge secondary with all devices turned on during the freewheeling phase is :

$$I_{RMS,secondary} = I_{out}\sqrt{\delta + \frac{1-2\delta}{4}}$$

Alternatively, if only two devices are turned on during the freewheeling phase, both of these devices are carrying the full load current for half of the clock cycle:

$$I_{RMS,secondary} = I_{out}\sqrt{0.5}$$

Since this value is always larger than or equal (for the maximum duty cycle $\delta = 0.5$), all rectifiers should be kept in the on-state during the freewheeling phase as long as possible to minimize the conduction loss.

A second possible implementation of a full wave secondary is a centre tap secondary, as shown in Figure 3.26. For the centre tap secondary, only two rectifying devices are required instead of the four devices in a full bridge secondary, and a transformer with two secondary side windings in series is used. To obtain the same output voltage as the full bridge secondary, each of the secondary windings needs the same turns ratio as the single secondary winding in the full bridge secondary. Because of this, the voltage stress on the secondary side devices is given by:

$$V_{stress,secondary} = \frac{2V_{in}}{2k_{HB}} = \frac{V_{in}}{k_{HB}}$$

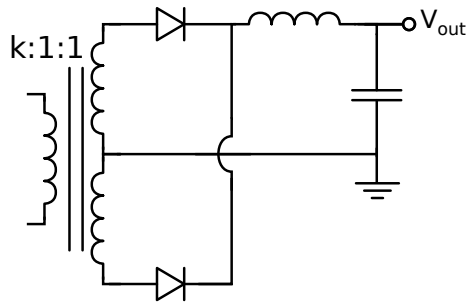


Figure 3.26: Centre tap secondary for double ended topologies

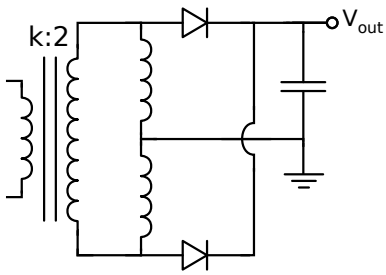


Figure 3.27: Current doubler secondary for double ended topologies

In each of the power transfer phases, one of the rectifying devices is conducting the full load current, while the other rectifying device is blocking the input voltage divided by the transformer turns ratio k_{HB}. During the freewheeling phase, the voltage over the transformer primary is zero, and with an ideal transformer the freewheeling current should be evenly distributed over both transformer secondaries and both rectifiers. In practice however, the magnetic coupling between both secondaries is not perfect because of the leakage inductance in each of the windings, and the current is not shared evenly over both secondaries and both rectifiers [58].
Because of the leakage inductance, most current keeps flowing in the rectifier and secondary that were conducting in the previous power transfer phase, until the transformer magnetization is inverted for the next power transfer phase and the other rectifier begins conducting. Because the leakage inductance is highly dependent on how the transformer is constructed and this is difficult to predict in an early design phase, a good approximation for the conduction loss is made by assigning half of each period to both of the rectifiers, regardless of duty cycle δ:

$$I_{RMS,secondary} = I_{out}\sqrt{0.5}$$

A third possible implementation of a full wave secondary is a current doubler secondary, as shown in Figure 3.27 and Figure 3.28. Because the rectifiers in the circuit in Figure 3.28

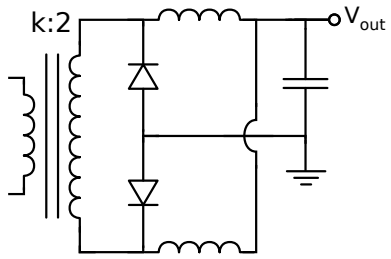


Figure 3.28: Current doubler secondary for double ended topologies with rectifier placement optimized for smart-power

are referenced to ground and can therefore be controlled without floating supply voltages, the circuit in Figure 3.28 is more suitable for implementation in a smart-power technology and is the one for which we will determine the voltage stress when implemented in a smart-power technology. The current doubler rectifier does not require a transformer with a centre tapped secondary, however for the same output voltage the current doubler requires a transformer turns ratio identical to both secondaries of a centre tap rectifier in series, i.e. twice as many secondary turns as the full bridge rectifier. In the current doubler topology, there is an additional inductor compared to the full bridge rectifier and the centre tap rectifier, however each of the inductors only carries half of the output current, so for each of these inductors a version with a lower current and smaller physical size can be used. During each power transfer phase, the full load current is flowing through one of the switches, or:

$$I_{RMS,secondary(powertransfer)} = I_{out}\sqrt{\delta}$$

During the freewheeling phases, the current is shared by both of the rectifying devices in the current doubler rectifier. Since each of the inductors is carrying approximately half of the output current, this portion of the secondary side RMS current is given by:

$$I_{RMS,secondary(freewheel)} = \frac{I_{out}}{2}\sqrt{1-2\delta}$$

Similar to the full bridge secondary, these currents are orthogonal and the total RMS current for each of the secondary devices in the current doubler secondary is thus:

$$I_{RMS,secondary} = I_{out}\sqrt{\delta + \frac{1-2\delta}{4}}$$

Because the current doubler secondary needs twice the number of turns on the secondary side of the transformer as a full bridge rectifier for the same output voltage, the rectifying devices are subject to a voltage stress that is twice as high as a full bridge secondary.

$$V_{stress,secondary} = \frac{2V_{in}}{2k_{HB}} = \frac{V_{in}}{k_{HB}}$$

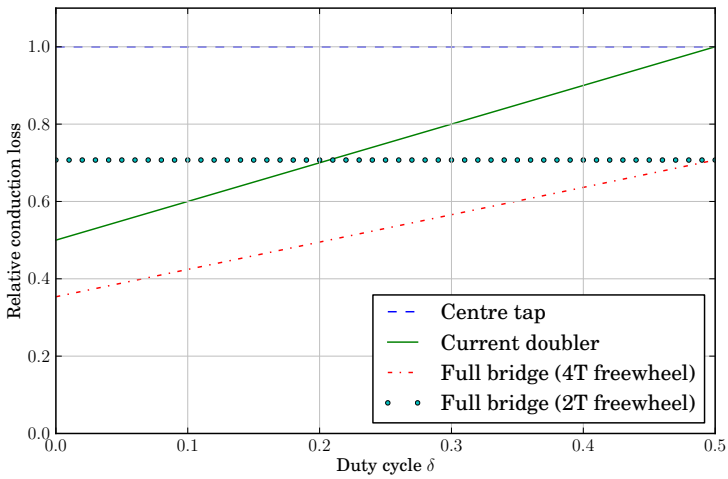


Figure 3.29: Relative conduction loss in double ended secondary side rectifiers in function of the duty cycle

Because of the difference in the voltage stress, the dependence on the duty cycle of the RMS current, and the different number of devices in these possible implementations of a double ended secondary side rectifier, a visual representation of the relative conduction loss in each of these implementations in function of the duty cycle can give the best summary of their relative merit. This is shown for an arbitrary output current and input voltage in Figure 3.29, but is valid for any output current and input voltage. As can be seen, the conduction loss for a given silicon area in a full bridge double ended secondary where all devices are activated during the freewheeling phase is the best case scenario for all duty cycles, despite using four rectifiers instead of just two in the alternative topologies. This can be attributed to the reduced voltage stress in the full bridge secondary compared to the alternative double ended secondary side rectifiers.

Full bridge

The full bridge converter topology is similar to the half bridge topology, with the capacitive voltage divider replaced by an additional pair of complimentary switches, and is shown in Figure 3.30.

In the full bridge converter, the power transfer phases occur when a diagonal pair of switches is turned on simultaneously, i.e. the low-side switch in one pair is turned on simultaneously with the high-side switch in the other pair. The voltage over the transformer primary is thus the input voltage of the circuit with alternating polarity. The voltage stress in the full bridge primary is thus also limited to the input voltage of the converter, regard-

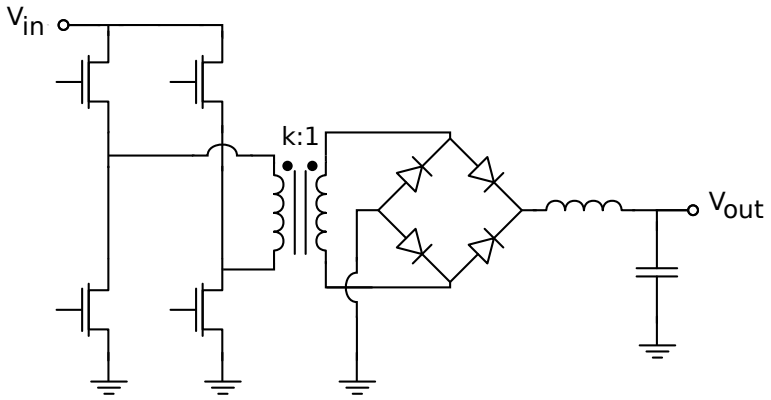


Figure 3.30: Full bridge converter with a full bridge secondary side rectifier

less of the duty cycle.

$$V_{stress,primary} = V_{in}$$

Because the voltage over the primary in the full bridge converter can alternate between V_{in} and $-V_{in}$, instead of $\frac{V_{in}}{2}$ and $-\frac{V_{in}}{2}$ in the half bridge converter, the turns ratio on the full bridge can be half the turns ratio on a half bridge for the same output voltage $k_{HB} = 2k_{FB}$. Therefore, for the same output current and input and output voltages, the current through the primary side switches in a full bridge is reduced by half compared to the half bridge. Because the current is halved and the number of switches is doubled in the full bridge, the expected conduction loss in the primary side of the full bridge and the half bridge is identical. The full bridge converter does not require a voltage divider as one leg of the bridge, and because of the reduced primary current and turns ratio in the transformer the full bridge can be implemented more efficiently.

$$I_{RMS,primary} = \frac{I_{out}}{k_{FB}}\sqrt{\delta}$$

As with the half bridge converter, a full bridge converter needs a full wave secondary to transfer energy for both directions of the transformer core magnetization. Because the transformer primary voltage is doubled and the transformer turns ratio is halved, the absolute value for the voltage stress in the secondary of a half bridge and full bridge converter with the same output voltage is identical. For the full bridge secondary, the expression for the voltage stress is:

$$V_{stress,secondary} = \frac{V_{in}}{k_{FB}}$$

For the current doubler and the centre tap secondary, the expression for the voltage stress is:

$$V_{stress,secondary} = \frac{2V_{in}}{k_{FB}}$$

Because the voltage stress and RMS current in the secondaries for a full bridge converter are identical to the half bridge for the same voltages and currents, the optimal smart-power implementation of a secondary for a full bridge converter is again a full bridge secondary with all devices activated in parallel during the freewheeling phase.

3.8 Optimal topology for the telecom reference applications

In this section, we will apply the information from the topology overview in the previous section to our reference applications. First, we will discuss the telecommunications back-office DC-DC converter with a conversion from a nominal 48 V and an input voltage range between 36 V and 72 V to 12 V, with a peak output current between 3 A and 6 A, followed by a discussion of a second converter with the same input voltage range and a 5 V output at 10 A. As in the general discussion of the division of silicon area over different devices, we will assume that N-type MOSFETs with an external bootstrap circuit are used, as this minimizes the required silicon area.

3.8.1 48 Volt to 12 Volt

Since this is a down-conversion, for the non-isolated converters we only need to consider the buck converter topology, since the increased voltage stress in the buck-boost converter will always lead to increased silicon cost compared to the buck converter. The optimal distribution of the silicon area over the switch and rectifier for a buck converter, taking into account the nominal power supply voltage and duty cycle $\delta = 0.25$, is given by:

$$S_{switch} = 0.366 S_{total}$$

$$S_{rectifier} = 0.634 S_{total}$$

With the total power dissipation being:

$$P_{total} = \frac{k_{Si} V_{ds,max}^{2.5} I_{out}^2 \delta}{S_{switch}} + \frac{k_{Si} V_{ds,max}^{2.5} I_{out}^2 (1-\delta)}{S_{rectifier}}$$

or in this case:

$$P_{total} = \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2 \left(\frac{\delta}{0.366} + \frac{1-\delta}{0.634}\right)}{S_{total}}$$

Once the device dimensions are fixed, we can estimate the conduction losses for an arbitrary total silicon area for the various duty cycles. For the nominal supply voltage, with duty cycle $\delta = 0.25$:

$$P_{total,buck} = 1.866 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}}$$

For the worst case conditions, with the low input voltage and duty cycle $\delta = 0.33$:

$$P_{total,buck} = 1.960 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}}$$

Since we already know from the general treatment on the transformer-isolated converters that the lowest silicon cost is achieved for the half bridge and the full bridge converter, with the full bridge having the advantage of a better transformer isolation and not needing a capacitive voltage divider, we can limit ourselves to considering the full bridge converter.

The transformer turns ratio is determined by the minimum input voltage and the output voltage. The transformer turns ratio is chosen so that at the maximum duty cycle $\delta = 0.5$ for each pair of switches, the output voltage can still be equal to the desired output voltage. In the case of our telecom converter, this translates into a turns ratio of the primary to the secondary of $k_{FB} = 3$, which in theory allows us to output 12 V for a 36 V input, if we ignore all voltage drops over switches and conductors, and if the switching times are infinitely small. In any practical full bridge converter, this is obviously not true, and a smaller turns ratio would be used for these specifications. However, we made the same assumptions for the determination of the duty cycle in the buck converter, so this does not introduce an unfair bias in our comparison.

Since the voltage stress on all devices and the RMS current through all devices in the full bridge primary are identical, we can assume identical power devices in the primary. For the secondary side devices, the voltage stress and RMS current are identical for all devices as well, so we can also assume identical devices at the secondary side.

In the primary side devices, there is only significant current flowing during the power transfer phases. During the freewheeling phase only the transformer magnetizing current, which is typically much smaller than the transformed load current, is flowing through the power devices. Therefore, in this approximation we can ignore the dissipation caused by the magnetizing current, and the primary side conduction loss in function of the relevant parameters is:

$$P_{primary} = 2 \frac{8 k_{Si} V_{in,max}^{2.5} \left(\frac{I_{out}}{k_{FB}} \right)^2 \delta}{S_{primary}}$$

To achieve a 12 V output for the nominal 48 V input with $k_{FB} = 3$, each pair of switches is operating at a duty cycle $\delta = 0.375$. In the full bridge primary, the conduction loss is then given by:

$$P_{primary} = 0.666 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{primary}}$$

In the secondary side devices for a full bridge (4T) rectifier, the maximum voltage stress is $V_{in,max} k_{FB}$. In the 4T full bridge rectifier, 2 devices are conducting during each power

transfer phase, and all devices are conducting during the freewheeling phases:

$$P_{secondary} = 4\frac{4k_{Si}\left(\frac{V_{in,max}}{k_{FB}}\right)^{2.5} I_{out}^2\left(\delta + \frac{1-2\delta}{4}\right)}{S_{secondary}}$$

For the nominal 48 V input, turns ratio $k_{FB} = 3$, and duty cycle $\delta = 0.375$, the numerical values become:

$$P_{secondary} = 0.449\frac{k_{Si}V_{in,max}^{2.5}I_{out}^2}{S_{secondary}}$$

Assuming an optimal distribution of the conduction loss in the primary and secondary over the silicon area leads to:

$$\frac{S_{primary}}{S_{secondary}} = \sqrt{\frac{0.666}{0.449}}$$

or:

$$S_{primary} = \frac{S_{total}}{1 + \frac{1}{\sqrt{\frac{0.666}{0.449}}}} = 0.549S_{total}$$

$$S_{secondary} = \frac{S_{total}}{1 + \sqrt{\frac{0.666}{0.449}}} = 0.451S_{total}$$

Therefore, the conduction loss in function of the total silicon area in the full bridge becomes:

$$P_{primary} = \frac{0.666}{0.549}\frac{k_{Si}V_{in,max}^{2.5}I_{out}^2}{S_{total}} = 1.213\frac{k_{Si}V_{in,max}^{2.5}I_{out}^2}{S_{total}}$$

$$P_{secondary} = \frac{0.449}{0.451}\frac{k_{Si}V_{in,max}^{2.5}I_{out}^2}{S_{total}} = 0.993\frac{k_{Si}V_{in,max}^{2.5}I_{out}^2}{S_{total}}$$

When we compare the buck converter and the full bridge converter for the 48 V (36 V to 72 V) to 12 V specifications, we can see that for the same total silicon area the conduction loss in a buck converter would be smaller, so we can either have a more efficient buck converter with the same silicon area as a full bridge converter, or a smaller buck converter with the same conduction loss. However, since transformer isolation is required for safety reasons in these telecommunications converters, the full bridge converter is the best possible converter implementation for this application.

3.8.2 48 Volt to 5 Volt

If we repeat the same exercise for our second telecom converter reference application, from 48 V (36 V to 72 V) to 5 V at approximately 10 A, the relation for the buck con-

verter based on a nominal duty cycle $\delta = 0.104$ with an optimal distribution of the conduction losses over switch and rectifier becomes:

$$P_{total,buck} = 1.270 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}}$$

For a full bridge converter, with theoretical turns ratio $k_{FB} = 7.2$, the primary side conduction loss is then given by:

$$P_{primary} = 0.116 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{primary}}$$

And at the secondary side:

$$P_{secondary} = 0.0503 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{secondary}}$$

With the optimized distribution of the silicon area over the primary and the secondary:

$$S_{primary} = \frac{S_{total}}{1 + \frac{1}{\sqrt{\frac{0.116}{0.0503}}}} = 0.397 S_{total}$$

$$S_{secondary} = \frac{S_{total}}{1 + \sqrt{\frac{0.116}{0.0503}}} = 0.603 S_{total}$$

The expected conduction loss in function of the total silicon area becomes:

$$P_{primary} = \frac{0.116}{0.397} \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}} = 0.292 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}}$$

$$P_{secondary} = \frac{0.0503}{0.603} \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}} = 0.0834 \frac{k_{Si} V_{in,max}^{2.5} I_{out}^2}{S_{total}}$$

Clearly, for the 48 V (36 V to 72 V) to 5 V application the full bridge converter leads to a significantly more efficient implementation than the buck converter in terms of silicon area versus conduction loss.

3.9 Conclusions

In this chapter, we first introduced the properties an ideal converter would have if we can ignore all physical limitations. Then, we briefly discussed the most important properties of the semiconductor devices that are used in monolithically integrated converters. After that, we discussed a number of possible implementations of the isolation structures in smart-power technologies, and their impact on the implementation of converters in those same technologies.

We introduced a cost function based on the conduction losses and the silicon area requirements of the available smart-power technology options, which allows for a high level evaluation of different converter topologies. The linear regulator topologies with their advantages and disadvantages were discussed next, followed by the switching converters, which are the actual focus of this work. Starting from the switched capacitor circuits, which are in monolithic implementations more appropriate for lower powered applications, we moved on to the switched inductor circuits, which can be divided in non-isolated topologies that can be optimal when the ratio of the input voltage and the output voltage is relatively close to unity, and transformer-isolated topologies that can allow for a significantly more efficient silicon implementation for large voltage conversion ratios.

For the non-isolated converters, the requirements on the input voltage and output voltage range dictate the appropriate topology, e.g. a buck converter can only be used for a voltage down-conversion, a boost converter can only perform a voltage up-conversion and a buck-boost converter can perform both up-conversion and down-conversion, albeit with a reversed polarity for the voltage. In the transformer-isolated topologies, the introduction of the transformer turns ratio allows for an additional degree of freedom, and the topology selection can be performed without constraints on the ratio of the input voltage and the output voltage.

For converters with a conversion ratio that is relatively far from unity, this additional degree of freedom will allow for a more efficient smart-power implementation. In the transformer-isolated topologies, the silicon cost function is minimized and equal for the half bridge converter and the full bridge converter, with the full bridge not requiring an additional capacitive voltage divider and allowing for a more efficient implementation of the transformer.

The most important characteristics of the switched inductor converters in continuous conduction mode are summarized in Table 3.4.

For our first telecom reference application, with a conversion from a nominal 48 V and an input voltage range between 36 V and 72 V to 12 V, the optimal topology selection from the cost-functions minimization would lead to the selection of a buck converter. However, the additional requirement for galvanic separation between the input and output in these telecom converters leads to the selection of a full bridge converter. For our second reference application with the same input voltage range and an output voltage of 5 V, the full bridge converter is optimal in terms of silicon cost, regardless of whether the application demands transformer isolation.

Topology	Non-isolated & single ended switches		Rectifier		Freewheeling	
	V_{stress}	I_{RMS}	V_{stress}	I_{RMS}	V_{stress}	I_{RMS}
Buck	V_{in}	$I_{out}\sqrt{\delta}$	V_{in}	$I_{out}\sqrt{1-\delta}$		
Boost	V_{out}	$\frac{V_{out}}{V_{in}} I_{out}\sqrt{\delta}$	V_{out}	$\frac{V_{out}}{V_{in}} I_{out}\sqrt{1-\delta}$		
Buck-boost	$V_{in} + \lvert V_{out}\rvert$	$I_{out}\frac{\sqrt{\delta}}{1-\delta}$	$V_{in} + \lvert V_{out}\rvert$	$\frac{I_{out}}{\sqrt{1-\delta}}$		
Flyback	$V_{in}\left(1+\frac{\delta}{1-\delta}\right)$	$\gg \frac{I_{out}}{k}$			$V_{out} + \frac{V_{in}}{k}$	$\gg I_{out}$
Forward 2T series	$2V_{in}$ for $\delta \leq 0.5$	$2\frac{V_{out}}{V_{in}} I_{out}\sqrt{\delta}$	$2V_{out}$	$I_{out}\sqrt{\delta}$	$2V_{out}$	$I_{out}\sqrt{1-\delta}$
Forward 2T AC	$2V_{in}$ for $\delta \leq 0.5$	$2\frac{V_{out}}{V_{in}} I_{out}\sqrt{\delta}$	$\frac{V_{in}}{k}\frac{\delta}{1-\delta}$	$I_{out}\sqrt{\delta}$	$\frac{V_{in}}{k}$	$I_{out}\sqrt{1-\delta}$
Forward 4T AC	V_{in} for $\delta \leq 0.5$	$2\frac{V_{out}}{V_{in}} I_{out}\sqrt{\delta}$	$\frac{V_{in}}{k}\frac{\delta}{1-\delta}$	$I_{out}\sqrt{\delta}$	$\frac{V_{in}}{k}$	$I_{out}\sqrt{1-\delta}$
	Double ended primary switches					
Half bridge	V_{in}	$2\frac{V_{out}}{V_{in}} I_{out}\sqrt{\delta}$				
Full bridge	V_{in}	$\frac{V_{out}}{V_{in}} I_{out}\sqrt{\delta}$				
			Double ended secondary rectifier			
Full bridge			V_{out}	$I_{out}\sqrt{\delta + \frac{1-2\delta}{4}}$		
Centre tap			$2V_{out}$	$I_{out}\sqrt{0.5}$		
Current doubler			$2V_{out}$	$I_{out}\sqrt{\delta + \frac{1-2\delta}{4}}$		

Table 3.4: Voltage stress V_{stress} and RMS current I_{RMS} in different topologies. The constant k refers to the transformer ratio.

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4

Enabling efficient smart-power integration

4.1 Introduction

In the typical power electronics textbook approach to the operation of switching DC-DC converters, some initial assumptions are made to simplify the analysis. In the initial chapters, all circuit components are assumed to be ideal: the transistors are represented by ideal switches, and inductors and capacitors behave according to a first order model with no energy leaving the circuit because of resistive loss or electromagnetic radiation. This model of the circuit greatly simplifies the analysis of the converter operation, and results in neat waveform graphs with nice straight lines that are well suited for deriving the basic equations for the operation of the converter. In all of these idealized converter topologies, no loss mechanisms are included, so the efficiency is always 100%.

For a more realistic approach to our topology optimization in the previous chapter, we already introduced the equivalent MOSFET channel resistance as a parasitic element, which includes the MOSFET conduction losses in the analysis and allows us to make an estimation of the required silicon area for a given topology and power budget.

In this chapter, we will first introduce the different types of parasitic elements and their effect on the converter operation. While the physics behind the parasitic elements are identical for the conventional discrete converters and smart-power converters, we will see that due to the specific properties of smart-power technologies the impact of some parasitic elements on integrated converters is not necessarily the same as for converters that use discrete power devices.

Further, we will identify where the traditional approach for handling the effects of these parasitic elements can be used in a smart-power implementation of the converter, and

where the traditional approach is impossible or impractical to implement. The remainder of the chapter will be dedicated to a novel approach for dealing with voltage overshoot at the secondary side of transformer-isolated converters.

4.2 From the ideal circuit to the real world

In this section we will discuss the different types of parasitic elements that appear in switching converter applications, and their influence on the design considerations for these converters.
Although a large number of research groups are tirelessly working towards room temperature superconductivity, the highest temperature at which superconducting materials – which are by definition materials with exactly zero electrical resistance – have been demonstrated is approximately 138 K (-135 °C) [1]. Since these temperatures are difficult and expensive to achieve all switching DC-DC converters that need to be able to work outside of a lab environment will need to take into account resistance as a parasitic element. Due to Joule losses, these parasitic resistances lead to power dissipation whenever current flows through the circuit and are therefore often referred to as conduction losses.

4.2.1 A more realistic inductor and transformer

The ideal inductor has inductance, but no resistance or capacitance, with the inductance resulting from the magnetic field generated by the current flowing through the inductor. Any change in this current results in a corresponding change in the magnetic flux, which by Faraday's Law generates an electromotive force in the conductor that opposes the change in current. Therefore, the inductor current can not change suddenly. The amount of electromotive force per unit of current is referred to as the inductance (in Henry), and is affected by the construction and geometry of the inductor, i.e. the size and number of turns, and the material in the area of the inductor. In the inductors used in switching converter applications, usually a high permeability material is placed in the vicinity of the current carrying conductor to increase the electromotive force, and thereby the inductance of the inductor.
The transformer is a special case of the inductor, where the magnetic flux is coupled between multiple inductors. By using a different number of turns on different inductors that share all or part of their magnetic flux, the amplitude of an AC voltage can be transformed up or down between the different inductors in a transformer. Because no conductive path needs to exist between the different inductors, transformers can be used to transfer electrical energy across galvanic isolation boundaries. Regardless of whether different inductors are coupled or not, the presence of parasitic elements is unavoidable.
A first parasitic element to consider is the resistance of the wire or PCB track that is used to construct the inductor or transformer. This introduces a real component to the purely imaginary impedance of an ideal inductor, and causes dissipation in the inductor. At DC, this real component is at its lowest value, and is referred to as the DCR (Direct

Current Resistance). The equivalent series resistance caused by the limited conductivity is not fixed: depending on the frequency, the physical geometry, and the conductivity of the conductor material, the skin effect limits the area of the conductor where current can flow, which decreases the available conductor cross-section and increases the equivalent parasitic series resistance of the inductor. A second parasitic element to consider is the loss in the ferromagnetic core that is used to increase the inductance compared to an air core inductor. These losses are caused by Eddy currents in the core material and hysteresis losses caused by the alternating magnetization of the core.

4.2.2 A more realistic capacitor

In an ideal capacitor, there is a capacitance but no resistance or inductance. The capacitance results from the electric field caused by a voltage difference between 2 conductors that are in close proximity, separated by a dielectric material. Like with the inductors, the finite conductivity of the conductors used in the construction of the capacitor and the losses in the dielectric between the conductors introduce a real component to the impedance of the capacitor, which causes Joule losses for a non-zero current. For capacitors this real component of the impedance is typically referred to as the ESR (Equivalent Series Resistance).
For switching converters, where the capacitors are charged and discharged often, the ESR and the ripple on the current is a decisive factor in the selection of the appropriate capacitor type. Tantalum electrolytic capacitors can realize high capacitor values in very small volumes, but have a high ESR value, which causes significant dissipation for a large ripple on the current. Aluminum electrolytic capacitors have a somewhat lower capacitor value for the same volume, but have a reduced ESR value compared to tantalum capacitors. Because of their attractive cost per unit of capacitance, aluminum electrolytic capacitors are often used as bulk capacitors to improve the low-frequency behavior of switching converters. However, since the operation of electrolytic capacitors is based on the mechanical motion of ions, which have limited mobility, the capacitance decreases with frequency and at high frequencies electrolytic capacitors no longer exhibit appreciable capacitive behavior. Ceramic capacitors can not match the capacitance density of tantalum or electrolytic, but have very low ESR values, and are therefore often preferred in high frequency applications.

4.2.3 A more realistic switch

In the idealized schematics of switching DC-DC converters, the switches are often represented by the symbol of a classic mechanical switch. In many ways, the mechanical switch is a good representation of what we expect from the switch in this type of converters. If the switch is in the open position, there is no conductive path for the current to flow, or in other words, the open switch represents an infinite resistance. If the switch is in the closed position, there is a direct connection with zero resistance.
In the real world, even in the open position there is a small but non-zero leakage current

flowing through the switch. This leakage current is typically voltage dependent and can be approximated with a large resistor in parallel with the switch. Similarly, in the closed position the switch can not create a perfect conductive path, because of limitations in the device physics and the packaging. The non-perfect nature of the conductive path is typically represented as a small resistor in series with the switch.
As we have discussed in the previous chapter, this is a rather good representation of the actual switch behaviour for MOSFET devices, and can be used to estimate the conduction loss for the switch. For other implementations such as Bipolar Transistors (BT) or Insulated Gate Bipolar Transistor (IGBT), the voltage drop over the switch is not linear with the current through the switch, and a simple series resistor will not allow an accurate estimation of the conduction loss. If such devices are used, the series resistor can be substituted with a more complex representation of the conduction loss component to allow for a more accurate model of the conduction loss.
However, the conduction loss component represented by the equivalent channel resistance is not the only parasitic effect in the MOSFET switches. We have already briefly discussed the energy required to change the voltage on the terminals of the MOSFET when we discussed the requirements for the dimensions of a bootstrap capacitor, but have not yet included the energy dissipation that is associated with the charging of the various capacitors in the calculation of the efficiency of the converters.
Because the MOSFET gate-source and gate-drain capacitor is charged and discharged during every switching cycle to turn the MOSFET on and off again, a more realistic model of the loss in switching converters includes the dynamic loss from the charging and discharging of the gate of the power MOSFET.

4.2.4 Realistic switches need drivers

Although a MOSFET is a current source controlled by the gate-source voltage, and except for some small leakage current, no current is required to keep the device turned on or off, this does not mean that we can control the MOSFET transistors in a switching application without being able to provide significant gate current.
As we have mentioned in the previous chapter, the low dissipation when using transistors as switches as opposed to in the linear region is possible by either having a large voltage over the device with virtually no current flowing, or by having a large current flowing through the device with a low voltage drop. For this to be true, the transition between these two states would need to be infinitely fast, as the linear operating region with the associated dissipation is between the on-state and the off-state.
As mentioned in the discussion of a more realistic model for the MOSFET, the gate of the MOSFET is a capacitive input, with the gate capacitor being the sum of the gate-source and the gate-drain capacitor. Because the charging and discharging of any capacitor is dictated by $I = C\frac{dV}{dt}$, an infinitely short transition time would require an infinite gate current, which is obviously impossible.
Additionally, the digital circuits that generate the timing signals for the MOSFET gate are dimensioned for minimal dimensions to consume as little power as possible, and to

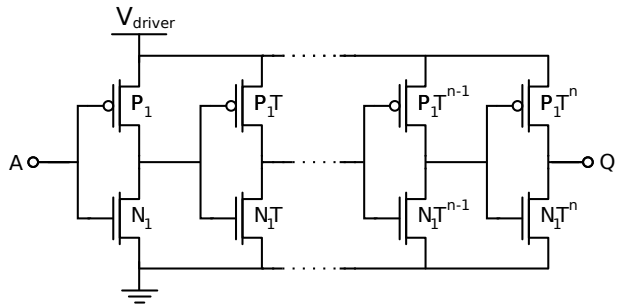


Figure 4.1: Tapered buffer

reduce the required silicon area. Since transistors with minimal dimensions can only provide very limited current, using the digital signals to drive the power devices directly would lead to very large transition times, which would cause significant dissipation in the power MOSFET and severely limit the maximum switching frequency. To allow the gate capacitor to be charged to the appropriate voltage in a time that is sufficiently short to limit the transition times, the MOSFET gate is charged through a driver, which is typically a series of CMOS inverters.

Each inverter is a totem pole configuration of complementary MOSFETs which are used as switches, so by increasing the transistor size in each successive inverter, the current handling capacity of the last stage is many times larger than the current handling capabilities of the logic level circuits. This series of inverters with increasing size is typically referred to as a *tapered buffer*, and is shown in Figure 4.1.

In most tapered buffers, a constant tapering factor is used for consecutive stages. Since the transistors in the tapered buffer are used as switches, and the input for each stage is the sum of the gate capacitors of two MOSFETs, the same considerations are valid for the drivers and the switches, larger devices increase the available current through the device at the cost of requiring more silicon area and having more capacitance to charge and discharge to turn the device on and off. An optimal tapered buffer will balance the switching loss and the conduction loss in both the power device and the driver itself. The design considerations for the implementation of tapered buffers in a monolithically integrated high-voltage converters for given power MOSFET dimension are described in Chapter 5.

4.2.5 Inductive parasitics

All the parasitic elements that have been mentioned until now are either resistive or capacitive, leading to respectively increased conduction loss or switching loss compared to idealized components. Even though this loss of efficiency is not desirable, these are not the most important parasitic effects in the implementation of a practical switching converter. The parasitic inductance in the circuit, combined with large and rapid changes in

current in the switching converters leads to large transient voltages on switching nodes, unless the voltage on these nodes is clamped in one way or another.
As we have seen in the chapter on the topology optimization for converters integrated in smart-power technologies, the voltage rating of the devices is a very important parameter in the design of an efficient switch. If we need to increase the voltage rating of our switches to account for the worst-case operation conditions, this leads to either greatly increased conduction loss when we keep the silicon area constant, or a much more expensive device with increased switching loss when we increase the silicon area to compensate for the reduced efficiency of the switch.
In transformer-isolated switching power converters, the secondary side transformer leakage inductance forms a resonant network with the parasitic capacitor of both the transformer and the rectifier. Since Ohmic losses in the conductors and transformer windings are low in most switching converters, the ringing phenomenon that occurs at the time of switching has large voltage amplitudes and long settling times. To avoid premature failure of the converter, either the breakdown voltage of the rectifying devices must be significantly over-dimensioned, which increases the cost and conduction losses of the converter, or a voltage clamp must be added to absorb the ringing energy.
Since the voltage overshoot at the secondary side of transformer-isolated circuits will have a significant impact on the required voltage rating of the transistors, we will dedicate the remainder of this chapter to ways of dealing with the voltage overshoot.

4.3 Handling the voltage overshoot

4.3.1 Increasing the device voltage rating

In some discrete converter circuits where the parts count, circuit complexity, and assembly cost are a major part of the design considerations for the converter, the optimal solution for handling the voltage overshoot caused by the inductive parasitics can be simply selecting a power transistor with a sufficiently high reverse breakdown voltage. If a power transistor from a similar product family is used, this will typically correspond with an increase in gate charge, an increase in conduction loss, or both. Alternatively, a transistor from a more advanced power technology can be used to maintain a similar gate charge and conduction loss at the increased voltage rating, however this will typically increase the component cost.
As we have seen in the topology optimization for the integrated converters, where most of the circuit components can be integrated on a single die to keep the assembly cost and parts count down, any increase in voltage stress will dramatically increase the required silicon area, so this is not an attractive approach for monolithically integrated converters.

4.3.2 Clamp circuits

When the clamping approach is used, the switching node voltage is limited, or 'clamped' by transferring most of the ringing energy to a clamp capacitor. The basic circuit of a

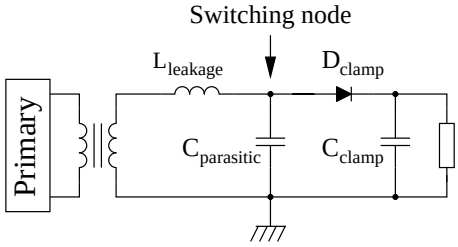


Figure 4.2: A typical dissipative secondary side RCD (Resistor, Capacitor, and Diode) voltage clamp

dissipative secondary side voltage clamp is shown in Figure 4.2. The leakage inductance and the parasitic capacitors are inherent to the transformer, rectifier and interconnects. The switching node, which would normally exhibit large voltage overshoot, is connected to the clamp capacitor by means of a fast clamping diode. Once the switching node voltage exceeds the clamp capacitor voltage, the diode conducts, and effectively parallels the clamp capacitor with the parasitic capacitors. The clamp capacitor is typically much larger than the parasitic capacitors, thereby limiting the rise in voltage. In steady-state conditions, the absorbed energy must be removed from the clamp capacitor by the next switching cycle. Dissipative clamps simply dissipate the energy in a resistor [2], as shown in the figure, whereas non-dissipative clamps recover most of the energy to the input or output of the converter [3] [4] [5] [6]. At least one inductive element, either an inductor or transformer, is required to transfer the energy away from the capacitor in the non-dissipative clamps. In non-dissipative clamp circuits, the capacitor reset operation is typically synchronized with the converter [3] [4] [5] [6], thereby imposing a lower limit on the inductor size.

In these traditional non-dissipative clamp circuits, significant engineering effort is required for every converter design. The optimization of the resonant circuits used in these clamp circuits depends heavily on circuit-specific properties. Therefore, the design of the clamp circuit often requires several iterations, and a successful design can not easily be reused at another output voltage or power level.

Generally, low-power converters can suffice with a simple dissipative RCD clamp. This allows for a simple, cheap and effective voltage clamp circuit, with the limitation being the dissipation in the clamping resistor. When the voltage overshoot on the switching node can no longer be adequately clamped without excessive dissipation in the clamp resistor, the additional complexity of alternative clamp circuits can be warranted. This is typically the case for medium and high-power discrete converters [2], since the parasitics tend to scale with the power level of the converter.

The alternative clamp circuits are often referred to as non-dissipative clamp circuits. Although this name may at first seem to imply that no power is dissipated in the clamp circuit, this merely indicates that contrary to RCD circuits not all energy is dissipated. The limitations of realistic components limit the efficiency of these clamp circuits to less

than unity. The term *energy recovering clamp circuit* is a more accurate description of these alternative clamp circuits, and is the one we will use.

A common property of the energy recovering clamp circuits that have been described in the literature is that their operation is synchronized with the main converter operation. When we take a closer look at the circuits used to implement the energy recovering clamps, we see a number of auxiliary inductors, supplementary transformers or transformer windings. Since the goal of implementing a monolithically integrated converter is limiting the number and size of components in a converter, this is obviously not desirable for a smart-power implementation.

4.3.3 Efficiency of energy recovering voltage clamp circuits

Unfortunately, even though the efficiency of the energy recovering clamp circuits is significantly higher than the dissipative clamp circuits, no clamp circuit can recover all the absorbed energy. Only a fraction η_{clamp} of the energy absorbed in the clamp circuit is recovered as useful energy, the remainder is dissipated in the clamp circuit. Similarly, only a fraction η_{SR} of the energy at the input of the synchronous rectifier is transferred to the output of the converter, and the remainder is dissipated in the synchronous rectifier. Depending on the configuration of the energy recovering clamp circuit, the recovered energy can be transferred to a different part of the circuit. Some clamp circuits recover the energy absorbed in the clamp circuit to the input of the converter, from where it is available again for conversion. Other circuits recover the absorbed energy to the output of the converter, reducing the power handling requirements of the synchronous rectifier.

For a given efficiency of the clamp circuit, recovering the energy to the output is more efficient than recovering the energy to the input as this avoids cycling a single packet of energy multiple times through the converter and clamp circuit, each time with the associated power dissipation. The output power of the converter is then given by $P_{out} = P_{SR}\eta_{SR} + P_{clamp}\eta_{clamp}$, with P_{SR} the input power of the synchronous rectifier and P_{clamp} the input power of the clamp circuit. Both P_{SR} and P_{clamp} originate from the power transferred through the primary of the converter and the transformer. Obviously, the total efficiency of the converter is optimized by transferring the maximum amount of energy through the most efficient path.

In a typical converter, the synchronous rectifier will be more efficient than the clamp circuit, since the design criteria for the synchronous rectifier will favor the energy efficiency as much as possible, while the clamp circuit is primarily intended to be as non-intrusive and small as possible by accepting a somewhat lower conversion efficiency. Therefore, total losses are minimized by limiting the energy transferred through the clamp circuit to what is required to keep the voltage stress within limits. A Sankey diagram of the power flow in a converter with an energy recovering clamp that transfers the absorbed energy to the output of the converter is shown in Figure 4.3.

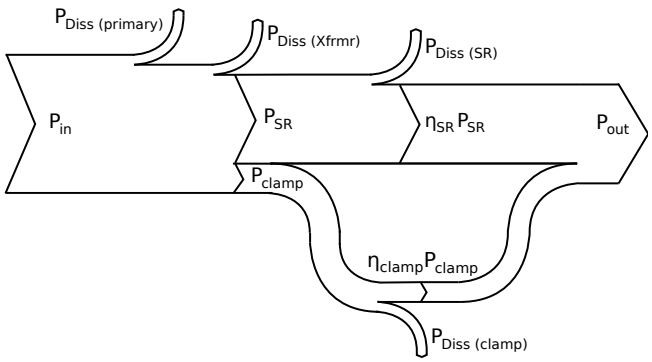


Figure 4.3: Sankey diagram of power in converter and clamp circuit with the clamp circuit recovering the absorbed energy to the output of the converter

4.4 The asynchronous active voltage clamp

4.4.1 Concept

Both the dissipative and energy recovering circuits that have been described in literature [2, 3, 5, 6] are problematic to implement in a smart-power technology if a significant reduction in the voltage stress is desired. To achieve a significant reduction in the voltage stress the clamp circuit needs to absorb a significant portion of the output power of the circuit. For dissipative clamp circuits, this leads to thermal management issues, as all the absorbed energy in the clamp circuit is converted into heat. For the energy recovering clamp circuits that are described in literature, typically one or more auxiliary inductors or transformer windings are required. Because the clamping operation in these circuits is synchronized with the converter frequency, the additional magnetic elements are relatively large, which is undesirable.
In 2011, we have presented a proof-of-concept for an alternative approach [7], where the energy from the clamp circuit is recovered to the output of the converter using a small auxiliary switching DC-DC converter. The principle schematic for this approach is shown in Figure 4.4. The auxiliary converter operates asynchronously from the main converter, so the operating frequency can be selected to be higher than the switching frequency of the main converter. This allows the asynchronous clamp circuit to use a single, physically small inductor to transfer the energy from the clamp circuit to the output of the converter.

The clamping operation of the asynchronous active clamp is identical to the dissipative RCD clamp circuit, but differs in the reset mechanism for the capacitor voltage. For the clamping action, the switching node(s), where the ringing phenomenon occurs and the clamping diode and capacitor can be approximated by the circuit in Figure 4.5. Because the capacitor reset mechanism, both with a dissipative and an asynchronous energy recov-

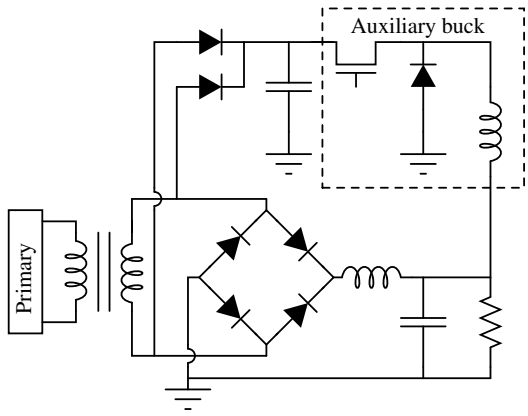


Figure 4.4: Basic schematic of the converter secondary with an asynchronous active clamp circuit

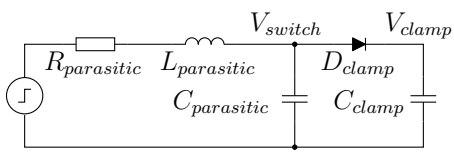


Figure 4.5: Equivalent schematic of the clamped switching node

ering clamp circuit operates on a larger time-scale than the clamping action, the capacitor reset mechanism is omitted from the figure.

The parasitic inductance $L_{parasitic}$ represents the leakage inductance of the transformer in series with the printed circuit board inductance. The parasitic capacitor $C_{parasitic}$ originates from the transformer, the switching devices and the interconnects. The parasitic resistance $R_{parasitic}$ is the transformer winding resistance and interconnect resistance on the printed circuit board. The switching waveform originating from the primary is approximated by a step function with an amplitude equal to the input voltage multiplied with the transformer ratio. The peak voltage stress on the switching node occurs at maximum input voltage. The current in the transformer at the moment of switching determines the initial condition for the current in the parasitic inductance.

Without the clamp circuit, this is a second order RLC circuit, with the damping factor ζ given by:

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$$

Because in a high-power converter circuit the parasitic resistance will be as low as possible to optimize the efficiency, the step response of this system is severely underdamped, and is subject to a ringing phenomenon with large amplitude and long settling times.

With the clamp circuit added to the switching node, the clamping diode can not conduct while the momentary voltage on the switching node V_{switch} remains below the initial voltage on the clamp capacitor $V_{clamp(t=0)}$, and the step response of the voltage on the switching node remains identical for the clamped and the unclamped circuit. Once the momentary voltage on the switching node rises sufficiently to allow the diode to conduct, the clamp capacitor is in parallel with the parasitic capacitor on the switching node, and the dynamic behavior of the circuit changes accordingly. Because of the increase in capacitor value, the damping factor is suddenly increased, and remains increased as long as the diode continues to conduct, which reduces the amplitude of the overshoot. Energetically, this corresponds with the clamp capacitor absorbing a part of the ringing energy, with the amount of energy depending on the initial capacitor voltage and the capacitor values of both the parasitic capacitor and the clamp capacitor.

Under steady-state conditions, the capacitor reset mechanism ensures that the absorbed energy is removed from the clamp capacitor by the next switching cycle. In the traditional dissipative clamps the clamp capacitor voltage is reset by dissipating the energy in a resistor, and the resistor value is selected to keep the peak voltage on the switching node within the desired limits. In the asynchronous active clamp the energy on the clamp capacitor is removed by transferring it to the output of the converter using an auxiliary DC-DC converter. The topology selection for this auxiliary DC-DC converter is discussed next.

The auxiliary converter needs to transfer energy from the clamp capacitor to the output of the converter, which is always a voltage down-conversion. For a smart-power implementation of this auxiliary converter, the optimal topology requires a low silicon area, and the lowest possible number of external components. With these design constraints, the buck converter and the flyback topology are the obvious choices. For similar input and output conditions, the voltage stress on the internal nodes of a flyback converter is relatively high, which requires additional silicon area to implement when compared to a buck converter. Therefore, the buck converter is selected as the topology for the monolithic integration of the auxiliary converter.

The well-known transfer functions of the idealised buck converter in continuous and discontinuous mode remain valid to describe the relation between the duty cycle, input voltage, and output voltage of the converter. However, in this application the output capacitor of the auxiliary converter – which is shared with the main converter – is several orders of magnitude larger than the clamp capacitor. Therefore, adjusting the duty cycle of the auxiliary converter regulates the clamp capacitor voltage instead of the output capacitor voltage. In the following section, we will discuss the efficiency considerations in the design of the asynchronous active voltage clamp, and show that the energy absorbed in the clamp circuit can be controlled by selecting an appropriate combination of the clamp capacitor voltage and the clamp capacitor value.

4.4.2 Discussion

Estimating the cost aspect of implementing an asynchronous energy recovering active clamp circuit is less straightforward than it may appear at first. When comparing the asynchronous active clamp with an RCD clamp, it is obvious that replacing the power resistor with a small DC-DC converter will increase the total complexity of the converter. However, the use of an energy recovering clamp circuit allows for a more aggressive voltage clamp, which reduces the voltage stress on the rectifiers and allows for the use of smaller, cheaper devices and/or improved efficiency. This allows for the use of devices with a lower voltage rating, which are typically cheaper, more efficient, and often also physically smaller. Eliminating the power resistor in the RCD clamp saves weight and space in the converter, and simplifies the thermal management of the converter. When comparing the asynchronous clamp with other non-dissipative clamp circuits, the increased switching frequency of the asynchronous active clamp allows the use of a significantly smaller inductor. The asynchronous active voltage clamp can be implemented using a commercially available buck converter IC with only a few tiny extra components, whereas other non-dissipative clamps typically need to be entirely constructed using discrete components. Using the proposed circuit, the clamp voltage can also be accurately set to optimize the converter efficiency over the entire input voltage range.

4.5 Proof-of-concept

As a proof-of-concept, the asynchronous active voltage clamp was implemented on a prototype phase shifted full bridge converter switching at approximately 220 kHz, using a 1:1 transformer ratio. The basic schematic is identical to the principle schematic shown in Figure 4.4. The secondary side rectifier is implemented as a self-driven synchronous rectifier using MOSFETs, but is shown in the figure as a diode bridge to simplify the drawing. The active clamp is implemented using an LM3103 buck converter IC with an integrated active rectifier, operating at 1 MHz, combined with a small (3 mm x 3 mm x 1.5 mm) SMT inductor.

Commercially available integrated converter ICs are only equipped with a control circuit designed to regulate the output voltage. However, using the EN/UVLO (enable/under-voltage-lockout) feature, which is available on many buck converter ICs, some degree of regulation of the clamp capacitor voltage can be achieved. The regular feedback network for the IC is dimensioned to ensure the duty cycle remains sufficiently large under all operating conditions. With this control strategy, and the clamp capacitor being much smaller than the output capacitor, the buck converter IC attempts to burst-wise discharge the clamp capacitor to the EN/UVLO voltage. Once the EN/UVLO voltage is reached, the IC is shut down to a low-power state for one or more cycles of the main converter, depending on the amount of hysteresis in the EN/UVLO implementation.

The asynchronous active clamp circuit allows for an intelligent control of the energy absorbed by the clamp capacitor. Other voltage clamp circuits operate regardless of the voltage on the clamp capacitor, thereby causing unnecessary losses in the clamp resistor

or in the non-ideal non-dissipative clamp circuit. By setting an appropriate offset on the EN/UVLO feature, the auxiliary converter discharges the clamp capacitor when required, and shuts down to a low-power state for the remainder of the time. This increases the efficiency of the converter by reducing the switching losses in the clamp circuit at lower input voltages.

In the proof-of-concept set-up, the performance of the active clamp — with several offsets, and in always-on mode — is compared to the unclamped converter, and to several resistor values in an RCD clamp. Measurements of the converter efficiency and voltage stress on the rectifiers at different input voltages are included in Table 4.1. The devices on the secondary side of the converter are only rated for a breakdown voltage of approximately $20\ \mathrm{V}$, therefore no measurements could be obtained for the high input voltage in the unclamped and $1\ \mathrm{k}\Omega$ RCD clamped converter.

As an example, we can compare the asynchronous active clamp circuit in always-on mode with a $47\ \Omega$ RCD clamp. For the $10\ \mathrm{V}$ input voltage, the active clamp circuit shows a higher voltage stress than the RCD clamp. However, the voltage is still well within the limits of the voltage rating of the devices, and efficiency is improved by 4.9 %. For the $14\ \mathrm{V}$ and $20\ \mathrm{V}$ input voltages, the voltage stress is comparable, and efficiency with the active clamp is improved by 7.8 % and 13.5 %, respectively. The expected increase in efficiency at lower input voltages by disabling the auxiliary converter at low clamp capacitor voltages is also apparent in the Table. The active clamp with a $15\ \mathrm{V}$ offset compared to the always-on clamp achieves a 0.5 % efficiency improvement at $10\ \mathrm{V}$ input voltage, and a 0.9 % efficiency improvement at $14\ \mathrm{V}$ input voltage, while keeping the voltage stress within limits. For the $20\ \mathrm{V}$ input voltage, the efficiency and voltage stress for the always-on clamp and active clamp circuits with different offsets are identical. In these cases, the rectified voltage is higher than the desired clamp regulation voltage, and the clamping circuit can not transfer enough energy to significantly discharge the clamp capacitor while the primary is providing energy. In Figure 4.6a, the voltages on the secondary side transformer connectors with respect to ground are plotted for the unclamped converter. In Figure 4.6b, the same voltages are plotted for the asynchronous active clamp in always-on mode. To achieve similar voltage stress on the devices, a $47\ \Omega$ RCD clamp is required, for which the voltages are plotted in Figure 4.6c. In the next section we discuss a smart-power ASIC implementation of the active clamp principle with a control circuit dedicated for clamping applications, which is the logical next step after a successful proof-of-concept of the active clamp principle using a commercial buck converter IC to reduce the voltage stress on the secondary side of a discrete converter.

4.6 ASIC Implementation

In discrete converters, it is sometimes desirable to simply increase the voltage rating of the power devices to keep the number of components to a minimum to optimize the cost and size of the converter. In smart-power converters, increasing the voltage rating of the devices to survive the worst-case operating conditions leads to a dramatic increase in circuit

Table 4.1: Peak voltage stress and converter efficiency for several dissipative and energy recovering clamping configurations on the discrete proof-of-concept converter for several input voltages

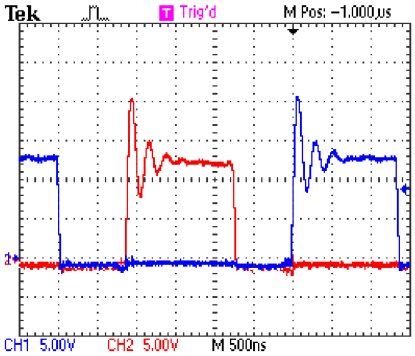
	$V_{in} = 10\ V$		$V_{in} = 14\ V$		$V_{in} = 20\ V$	
	η	V_{stress}	η	V_{stress}	η	V_{stress}
Unclamped	0.781	15.4	0.742	21.4	-	-
RCD 1kΩ	0.777	12.9	0.741	18.8	-	-
RCD 100Ω	0.756	10.3	0.698	14.5	0.621	20.9
RCD 47Ω	0.727	10.5	0.665	14.2	0.555	20.3
AC (always-on)	0.776	12.4	0.743	14.6	0.690	20.5
AC (10V offset)	0.778	12.5	0.743	14.5	0.691	20.5
AC (12V offset)	0.781	14.5	0.752	16.7	0.690	20.4
AC (15V offset)	0.781	15.3	0.752	18.2	0.690	20.4

area for the power devices, as the specific resistance (Ωmm^2) is approximately proportional to $V_{ds,max}^{2.5}$. Since voltage overshoot can easily double the nominal voltage, this would greatly increase cost, or dramatically decrease the performance of the converter. Integrating a dissipative clamp is not feasible, due to limitations on the resistors that can be integrated in IC technologies. Due to the high cost of IC prototyping the numerous design cycles of traditional non-dissipative clamps become prohibitively expensive, and are therefore also not an attractive option.

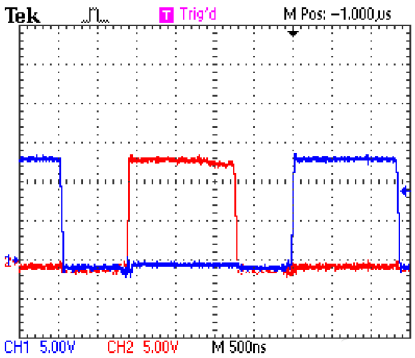
In contrast, the asynchronous active clamp can be integrated on the same die as the synchronous rectifiers, with a small number of passive external components to set the operation point of the clamping operation. A smart-power ASIC integration also allows us to include a control circuit that is specifically designed for use in clamping applications, thus avoiding the workaround with the EN/UVLO feature of a commercial converter IC [8].

The asynchronous active clamp was implemented in the SHARC ASIC, which stands for Self-driven High-power Adaptive Rectifier with Clamp. The SHARC ASIC is a monolithic integration of one leg of a full bridge synchronous rectifier at the secondary side of a 36-72V to 12V phase shifted full bridge converter, designed to work at a switching frequency of $1\ \mathrm{MHz}$. The power stage of this synchronous rectifier is subdivided in multiple segments, which are automatically enabled and disabled depending on the current through the synchronous rectifier. This method to optimize the efficiency of the converter over the load range is discussed in more detail in Chapter 5.

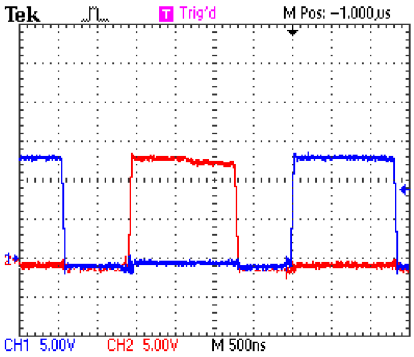
The ASIC was designed for load currents up to $3\ \mathrm{A}$ using the integrated power MOSFETs. The selected smart-power technology for this application is the ON Semiconductor I3T50 (50 Volt, $0.35\ \mu\mathrm{m}$) technology.



(a) Unclamped



(b) Always-on active clamp



(c) 47 Ohm RCD clamp

Figure 4.6: Secondary side voltages for 14 V input voltage with proof-of-concept converter

4.6.1 Preliminary design considerations

Because of the limited flexibility in the control of both the dissipative and traditional energy recovering clamp circuits, the clamp circuit is out of necessity designed to keep the voltage stress within acceptable limits for worst-case conditions, and little consideration can be given to other operating conditions. These clamp circuits cause unnecessary dissipation under most other operating conditions, which negatively influences the efficiency of the converter. The asynchronous active clamp circuit provides greater control over the amount of energy that is transferred through the clamp circuit. For a well designed asynchronous voltage clamp, the worst-case voltage stress can be kept within acceptable limits, while dissipating as little power as possible in the clamp circuit over the entire operating range.

The circuit parasitics, the current in the transformer secondary at the time of switching, the clamp capacitor value, and the voltage that can be tolerated on the switching nodes all determine the energy that is absorbed in the clamp circuit. The power handling requirement for the asynchronous clamp circuit is then the energy absorbed during each switching event, multiplied with the effective switching frequency on the switching node or nodes. Depending on whether a single-ended or double-ended topology used in the switching DC-DC converter, this is either equal to the switching frequency, or twice the switching frequency. In the case of the phase shifted full bridge DC-DC converter, there are 2 switching events during every period.

The energy that is absorbed in the clamp circuit for each switching event can be approximated by assuming the clamping diode only conducts for a short time, during which little energy is transferred away from the clamp capacitor by the auxiliary converter, and by assuming that under steady-state conditions the voltage on the clamp capacitor is reset by the next switching cycle. The equations that describe this system are relatively unwieldy for manual calculations, but can easily be solved with numerical tools. Using these equations, and measurements or estimations of the parasitic elements, the optimal capacitor value in the clamp circuit and the capacitor regulation voltage can be determined.

The lower limit for the clamp capacitor regulation voltage is the maximum idealized secondary side voltage without overshoot, i.e. the maximum input voltage multiplied with the transformer ratio. For lower clamp regulation voltages, the clamping diode would be conducting during the entire on-time of the converter, which would significantly increase power transfer through the clamp circuit, as the clamping circuit then attempts to bypass the (synchronous) rectifier. Typically, neither the clamping diode nor the clamp circuit are designed to transfer the entire output power, and selecting a lower voltage will rapidly decrease the efficiency of the converter. As an initial estimate for the requirements on the clamp circuit, before the ASIC and test-board setup were manufactured, the following values were used to estimate the voltage stress using the circuit shown in Figure 4.5: $L_{parasitic}$ = 50 nH, $C_{parasitic}$ = 5 nF, $R_{parasitic}$ = 100 mΩ, $I_{initial}$ = 2.5 A. Because an integer transformer turns ratio is required, and a 3:1 ratio does not provide adequate headroom for a 12 V output for 36 V input, a 5:2 transformer ratio was selected. Therefore, the response to a 28.8 V step (corresponding with a 72 V input voltage) is calculated

C_{clamp} (nF)	V_{clamp} (V)	P_{clamp}(W)
33	31	9.3
47	35	7.5
100	38	6.5
220	39.3	6.1
470	39.5	6.1
1000	39.7	6.1

Table 4.2: Some combinations of capacitor values, clamp regulation voltages and power handling requirements for the clamp circuit that result in staying within the 25 year safe operating area for the I3T50 technology, assuming an ideal diode and estimations of the parasitic elements

instead of a 24 V step, as might be expected from an idealized transformer winding ratio calculation. Without any clamping, these values result in a peak voltage stress in the circuit of 57.2 V.

To remain within the 25 year lifetime safe operating area over a wide temperature range for the high-voltage transistors in the ON Semiconductor I3T50 technology, the drain-source voltage for these transistors is limited to 40 V [9]. No detailed information is available on the lifetime under other conditions, however the breakdown voltage is specified as minimally equal to 50 V, so the voltage stress should be kept below this value at all times to ensure proper operation. A first design goal is minimizing the power transferred through the clamp circuit to optimize the efficiency of the converter, while using the smallest possible capacitor, to minimize the dimensions of the clamp capacitor. The energy absorbed in the clamp circuit not only depends on the parasitic elements, but also on the clamp capacitor value and the clamp regulation voltage. Some combinations of capacitor values, clamp regulation voltages and power handling requirements for the clamp circuit that result in staying within the 25 year safe operating area for the I3T50 technology are listed in Table 4.2, assuming an ideal clamping diode. With clamp capacitor values below 33 nF, it is not possible to remain within the 25 year safe operating limits, regardless of the clamp regulation voltage, so these results are not included in the Table. To remain within the 25 year safe operating area a 220 nF clamp capacitor with a clamp regulation voltage of 39.3 V results in approximately 6.1 W transferred through the clamp circuit. With these values for the parasitic elements, further increases in the clamp capacitor values offer no significant further reduction in the energy transferred through the clamp circuit, and these parameters were used for the optimization of the power devices in the active clamp circuit on the smart-power ASIC.

To minimize the power under other than worst-case conditions, the clamp regulation voltage should be close to the maximum allowable voltage stress to minimize the power dissipation for non-worst-case situations. Assuming an ideal diode, a 220 nF capacitor would appear to provide a good balance between a low capacitor value, which allows for a physi-

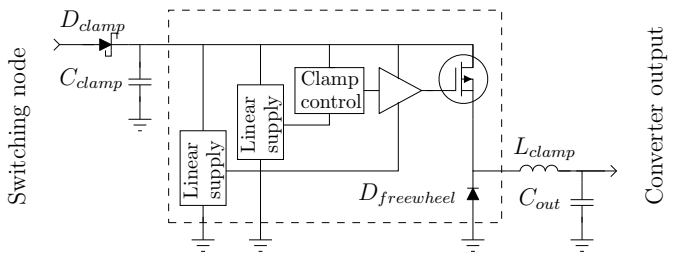


Figure 4.7: The complete asynchronous active clamp circuit. The components that are not integrated on the smart-power IC are shown outside the dashed rectangle.

cally small component, and the power handling requirement of the clamp circuit. Simultaneously, this capacitor value allows for a clamp regulation voltage sufficiently close to the maximum allowable voltage stress to minimize the power under non-worst-case operating conditions. However, like with other components, ideal diodes do not exist and the finite switching speed and the voltage drop of real diodes result in a clamp capacitor voltage that needs be lower than the theoretical value in order to absorb sufficient energy to clamp the voltage to the appropriate value. Since the clamping speed also somewhat depends on the physical location of the clamping diode and capacitor, the exact clamp capacitor voltage for a given voltage stress needs to be verified experimentally, but is expected to be lower than estimated from this approximation.

4.6.2 System partitioning

A schematic of the active clamp circuit, as integrated on the IC is shown in Figure 4.7. The freewheeling diode, the control circuit, the driver and the power MOSFET of the active clamp circuit are integrated on the die. Only an external inductor, a clamp capacitor and a clamping diode are required for the operation of the circuit.

A number of publications have already shown buck converters with inductors integrated on the die, either in metal layers or using bond-wires [10]. However, for the current requirements in the active clamp circuit this is not feasible, and an external inductor is unavoidable. Because the active clamp circuit operates asynchronously from the main converter, a low inductor value can suffice, and this external inductor can be a physically small SMD type inductor.

While it is feasible to integrate high-voltage capacitors in the I3T50 technology, significant silicon area is required to manufacture even small capacitor values, and large values are generally not cost-efficient. Typical values for a 4 metal layer sub-micron technology are in the order of $250\ \mathrm{pF/mm^2}$ [11], so the integration of the appropriate capacitor value for an effective and efficient clamp circuit, as determined in the previous section requires a prohibitively large silicon area. Therefore, the clamp capacitor in a high-power converter is preferably implemented as an external component, since a small and cheap external component will perform the same function at a much lower cost.

Finally, the clamping diode is also implemented as an external device. In the I3T50 technology, no high-voltage integrated Schottky diodes are available, and the high-voltage bipolar devices are not sufficiently fast for clamping applications.
As shown in Chapter 3, the required silicon area for a given conduction loss in a high-side MOSFET is not necessarily lower for a N-channel MOSFET than for a P-channel MOSFET, once the silicon area for the bootstrap circuit is included in the comparison. To simplify the control of the clamp circuit, and to avoid the on-chip generation of floating supply voltages, the switch in the active clamp circuit is implemented as a P-channel MOSFET device.
To minimize the impact of switching noise on the sensitive timing circuit, the power domains for the timer circuit and for the driver circuit have been separated. They have their own integrated linear regulator, and are both decoupled using on-chip capacitors of approximately $25\ \mathrm{pF}$.
The losses in the asynchronous active clamp circuit can be minimized by selecting an appropriate control scheme. The conventional constant-frequency PWM control of a buck converter can be used to control the voltage on the clamp capacitor, however this leads to less than optimal efficiency. Under most input conditions, little power needs to be transferred through the clamp circuit, and a constant-frequency PWM control scheme will generate significant switching losses. Similar to stand-alone converters, the switching losses can be reduced by limiting the switching activity whenever possible. By using a control block with a constant on-time and variable off-time, the clamp capacitor is discharged to the appropriate clamp regulation voltage in as few switching cycles as possible. In applications that are sensitive to the wide spectrum switching noise generated by this control scheme, a fixed frequency approach may be more appropriate. Because of the reduced efficiency of a fixed frequency approach, this was not implemented in the control block for the asynchronous voltage clamp circuit on the ASIC, although a fixed frequency control scheme is expected to be just as effective in clamping the peak voltage to the required value under worst-case conditions.
The freewheeling diode is integrated, however, it can also be externally bridged with a (Schottky) diode for improved performance. In later versions of the clamp circuit, the freewheeling diode could also be implemented as a synchronous rectifier. Because the power is relatively limited, and to simplify the control circuit, this is not implemented in the SHARC ASIC.

4.6.3 Control block

The control block for the active clamp circuit on the SHARC ASIC is a relaxation oscillator, where a Schmitt trigger is connected to a timing capacitor that is alternately charged and discharged. The discharging time determines the buck converter on-time, while the charging time determines the off-time. The timing circuit for the on-chip clamp circuit is shown in Figure 4.8, with R_{ch}, R_{dis} and D_Z implemented as discrete external components for maximum flexibility during characterization of the circuit. In the circuit as shown, the on-time of the P-type power MOSFET in the converter is determined by the

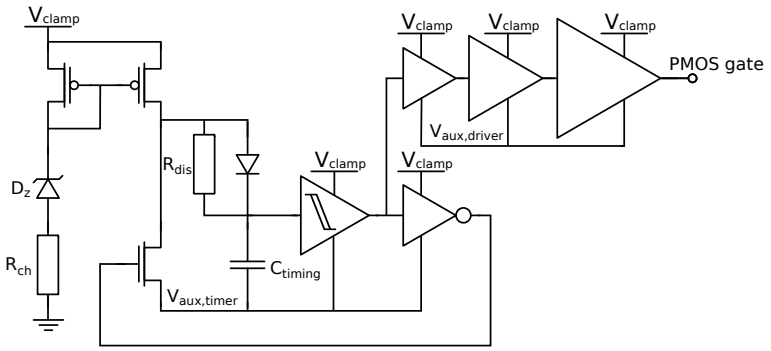


Figure 4.8: Control block for the active clamp circuit on the SHARC ASIC

value of resistor R_{dis} and timing capacitor C_{timing} , and is virtually independent of the value of the clamp capacitor voltage V_{clamp}. The off-time of the power MOSFET is determined by both the timing capacitor value and the current through the current mirror, which depends on the clamp capacitor voltage, the Zener voltage V_z of diode D_z, the current mirror transistor threshold voltage V_{th}, and the value of resistor R_{ch}:

$$I_{ch} = \frac{V_{clamp} - V_z - V_{th}}{R_{ch}}$$

With this configuration, the switching activity while V_{clamp} is smaller than $V_z + V_{th}$ is extremely limited, as only the leakage current through the devices will charge the timing capacitor. Once V_{clamp} exceeds the voltage, the duty cycle and the switching frequency quickly increase, thereby increasing the energy transfer from the clamp capacitor to the output of the converter. Essentially, this simple circuit only provides a proportional control loop, and is therefore expected to give only a relatively crude regulation of the clamp capacitor voltage. However, due to the simplicity of the control circuit the power consumption is very low, while still allowing a large flexibility in the control of the circuit to optimize the efficiency by swapping out a resistor or Zener diode.

4.6.4 Comparison with dissipative clamp circuits

Due to an issue with a digital control block, which is discussed in Chapter 5, the segmented synchronous rectifiers on the SHARC ASIC could not be used to verify the operation of the clamp circuit. As an alternative, the functionality of the clamp circuit on the SHARC IC was verified using a synchronous rectifier in a centre-tap configuration with 2 discrete power MOSFETs that are controlled from the primary side through an ISO7420 [12] digital isolator IC and an LM5110 [13] driver IC.
Unfortunately, this change increases the physical distance between the rectifiers and the clamp circuit, which would in case of the integrated rectifiers have been on the same IC. As a consequence, the parasitic component values are outside of the design margin

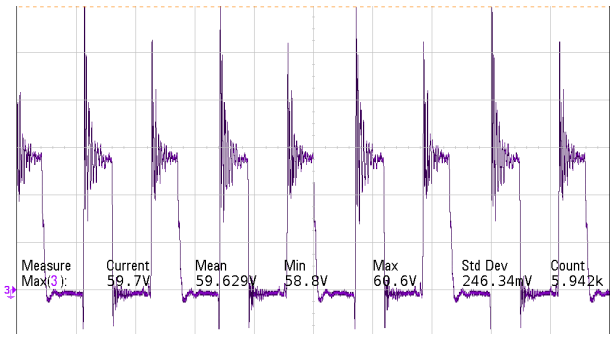


Figure 4.9: Secondary side waveforms for the maximum input voltages for the converter without any clamp circuit (10 V/division) for 30 W output power

for which the clamp circuit on the IC was designed. The most notable difference is in the form of increased inductance, which reduces the damping factor and increases the amount of energy in the parasitic elements. Because of this, the performance of the clamp circuit is expected to be less than optimal at the maximum input voltage, where most of the energy needs to be transferred through the clamp circuit to keep the voltage stress within limits.

As a baseline for the other measurements, the secondary side waveforms for the 72 V maximum input voltage for 30 W output power is shown in Figure 4.9. As can be seen, for this output power the nominal voltage 28.8 V for a 72 V input divided by the 5:2 transformer ratio can reach voltages on the secondary side switching node as high as 59.7 V when no clamping measures are implemented. Although this measurement is performed with a discrete synchronous rectifier instead of an rectifier integrated in the I3T50 technology, which causes the overshoot to be larger than expected with the integrated rectifiers due to the increased parasitics in the interconnects and the rectifier, it is worth noting that these values are not only outside of the 25 year safe operating area for the I3T50 technology, but also well outside of the nominal breakdown voltage rating.

In Figure 4.10, the input voltage is swept over the $36 - 72$ V range for a number of load ranges without any clamp circuit. Each data point represents the average per-cycle peak secondary side voltage, with the error bars indicating the maximum and minimum peak value over a 10 second observation window. Because of the increased parasitics and the expected increase in energy in the leakage inductance, a clamp capacitor value of 2.2 µF is used for the measurements to ensure the measurements are non-destructive to the energy recovering clamp circuit on the smart-power ASIC. To ensure a fair comparison, this increased capacitor value was used for both the dissipative and energy recovering clamp circuits.

As is known from literature, a dissipative RCD clamp circuit is capable of arbitrarily reducing the worst-case voltage stress by increasing the dissipation in the clamp circuit, which obviously is coupled with a reduced efficiency. This is demonstrated for a

500 Ω, 250 Ω, and a 100 Ω resistor in the RCD network, as shown in respectively Figures 4.11, 4.12, and 4.13. It is immediately obvious that to reduce the voltage stress on the devices to a value that is even remotely close to the 40 V 25 year safe-operating area for a hypothetical rectifier integrated in the I3T50 technology that is connected to this switching node, significant power needs to be dissipated in an RCD clamp circuit, leading to reduced efficiency and significant dissipation in the clamp circuit.

As an example, for the 72 V input voltage and the 100 Ω RCD clamp, more than 8 W is dissipated in the resistor of the clamp circuit, regardless of the output power. Obviously, this is detrimental to the efficiency, especially for the lower range of the output power, and necessitates the use of a bulky power resistor. The typical footprint dimensions for a Welwyn WH25 or Tyco THS25 100 Ω resistor that is barely rated for this dissipation without a heatsink at an ambient temperature of 25 °C is approximately 51 mm by 19.8 mm with a height of 15 mm [14] [15]. A power resistor from the Welwyn WH50 or Tyco THS50 series with a slightly more comfortable margin capable of operating at an ambient temperature of 70 °C without a heatsink has footprint dimensions of approximately 72.5 mm by 21.4 mm with a height of 16 mm.

When we compare the performance of the dissipative clamping circuits with the energy recovering clamp circuit as implemented on the IC, we can see that in both the worst-case voltage stress is significantly reduced compared to a circuit without clamping, while maintaining a much higher efficiency in the latter than in the former. As a first comparison, we can compare the energy recovering clamp circuit configured for an on-time of approximately 500 ns and a Zener voltage of 30 V with a 250 Ω dissipative clamp. The measurements on the energy recovering active clamp are shown in Figure 4.14, under the same measurement conditions as the resistive clamp shown in Figure 4.12. We can see that at high input voltage, the voltage stress is in the same range for both clamp circuits, e.g. for the dissipative clamp the worst-case voltage stress is in the range of 40 V to 44 V over the load range, and for the 30 V clamp circuit the worst-case voltage stress is in the 39 V to 44 V range. For lower input voltages, the resistive clamp circuit continues to dissipate energy to reduce the voltage stress on the switching node, although this is not required to protect the switching devices. Therefore, all efficiency curves for the resistive clamp circuit are shifted down over the entire input range, and for all load values. In contrast, the energy recovering clamp circuit maintains more-or-less the same voltage stress on the switching node over the entire input range by only absorbing and transferring energy to the output when this is necessary. This does not cause a significant downward shift of the efficiency compared to the converter without clamping for low input voltages, and can for high input voltages and large load currents even increase the efficiency of the converter compared to the converter without clamping. The increase in efficiency at high input voltages and large output currents can be explained by the reduced conduction loss in the synchronous rectifier devices of the converter, since a non-negligible fraction of the output current is delivered through the parallel path in the clamp circuit.

In this first comparison, neither the dissipative nor the energy recovering clamp circuit was able to reduce the voltage stress to within the limits for the 25 year safe operating area, although both clamp circuits were able to reduce the voltage stress to below the

nominal breakdown voltage. Even though the clamp circuit was designed for use with an integrated synchronous rectifier and is now used with a discrete synchronous rectifier leading to increased power handling requirements on the clamp circuit, the limits of the integrated energy recovering clamp circuit were explored by using a Zener voltage of $27\ \mathrm{V}$ in the control circuit. The maximum per-cycle peak voltage and the efficiency of the converter is plotted in Figure 4.15. As can be seen in the graph, the energy recovering clamp circuit is able to reduce the voltage stress to below $40\ \mathrm{V}$ for all input voltages over the entire load range, which is within the safe operating area for a hypothetical integrated rectifier connected to the switching node. However, it should be noted that for input voltages of $70\ \mathrm{V}$ and above the self-heating in the clamp circuit is significant, which induces parameter shifts in the devices of the timing circuit and can lead to thermal run-away, destroying the ASIC in minutes.

As we have shown, it is possible to achieve a significant reduction in voltage stress while maintaining or increasing the efficiency of the converter over the input voltage and load range with the energy recovering active clamp circuit. This allows for the implementation of the synchronous rectifier in significantly less silicon area than would be possible without clamping, while not requiring bulky power resistors to dissipate the ringing energy. If we want to put the decreased area requirements into numbers, we can take a closer look at the dimensions of the clamp circuit on the ASIC, as shown in Figure 4.17. The silicon area used for the clamp circuit is only $0.63\ \mathrm{mm}^2$, and requires only a handful of external components to operate: because of the desire for a flexible control loop in this prototype, the two resistors, the small signal diode and the Zener diode from the timing circuit are implemented as external components. As discussed earlier, at the required switching frequencies and power level an external power inductor is unavoidable to achieve the necessary current handling capability and inductance value. Despite this, the inductor used in the testing of the clamp circuit only has a footprint of $4.8\ \mathrm{mm}$ by $4.8\ \mathrm{mm}$ with a height of $1.8\ \mathrm{mm}$ [16]. No other components are required to implement the clamp circuit, so the energy recovering clamp circuit not only improves the efficiency of the converter compared to an RCD clamp circuit, but does this in significantly smaller physical dimensions. To illustrate this, Figure 4.16 compares the physical dimensions of the ASIC which includes the clamp circuit and the (non-functional) synchronous rectifiers and the external components that are used for the configuration of the clamp circuit with the two power resistor series that were discussed earlier for use in dissipative clamp circuits. Because of the simple control loop that is implemented on the ASIC, which was mainly selected for its flexibility in testing and low power consumption, the control over the clamp capacitor voltage is relatively crude. A first indication for this is the non-constant clamp capacitor voltage over a sweep of the input voltage and load power, which would be a more-or-less constant value over the range with a control loop tuned for stability and zero steady-state error. A second indication of the shortcomings of the control loop is the relatively large error bars on the measurements of the voltage stress. This is caused by an oscillation in the control of the off-time, leading to a non-constant energy transfer through the clamp circuit. It can be expected that with a more advanced control loop the clamp capacitor voltage and the voltage stress on the switching node can be made more stable.

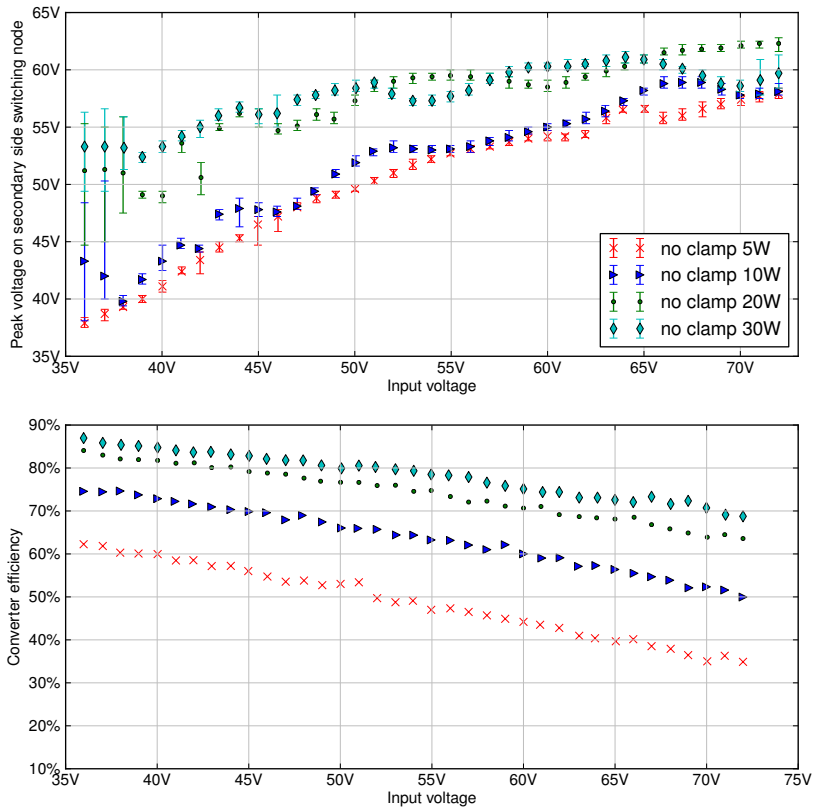


Figure 4.10: Average per-cycle peak secondary side voltages versus converter input voltage for different output loads without any clamp circuit, error bars indicate minimum and maximum value over a 10 s observation window (top), converter efficiency for the same measurements (bottom)

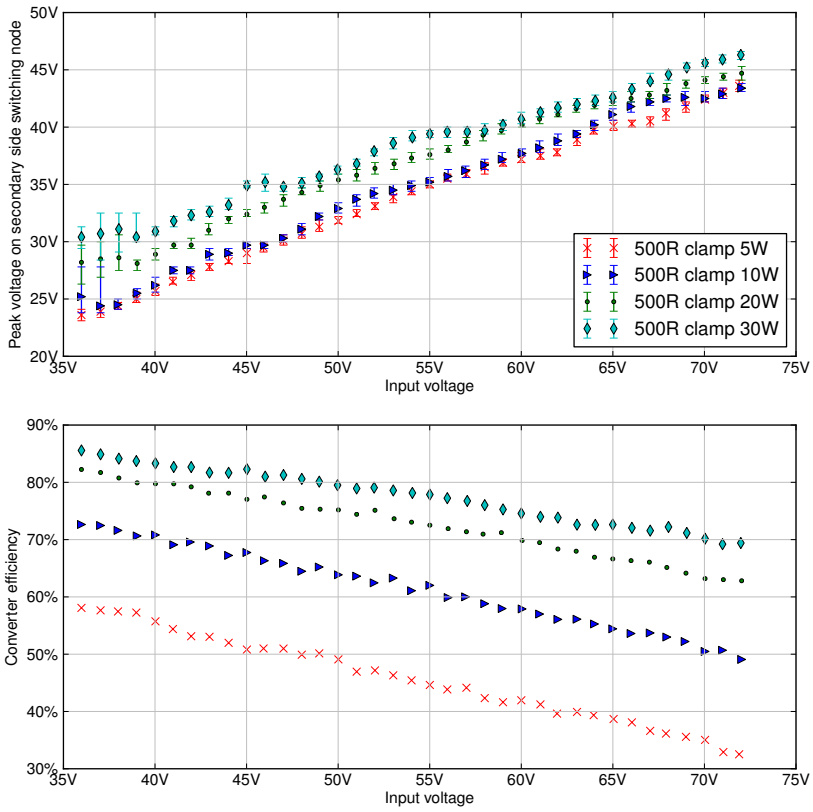


Figure 4.11: Average per-cycle peak secondary side voltages versus converter input voltage for different output loads with a 500 Ohm RCD clamp circuit, error bars indicate minimum and maximum value over a 10 s observation window (top), converter efficiency for the same measurements (bottom)

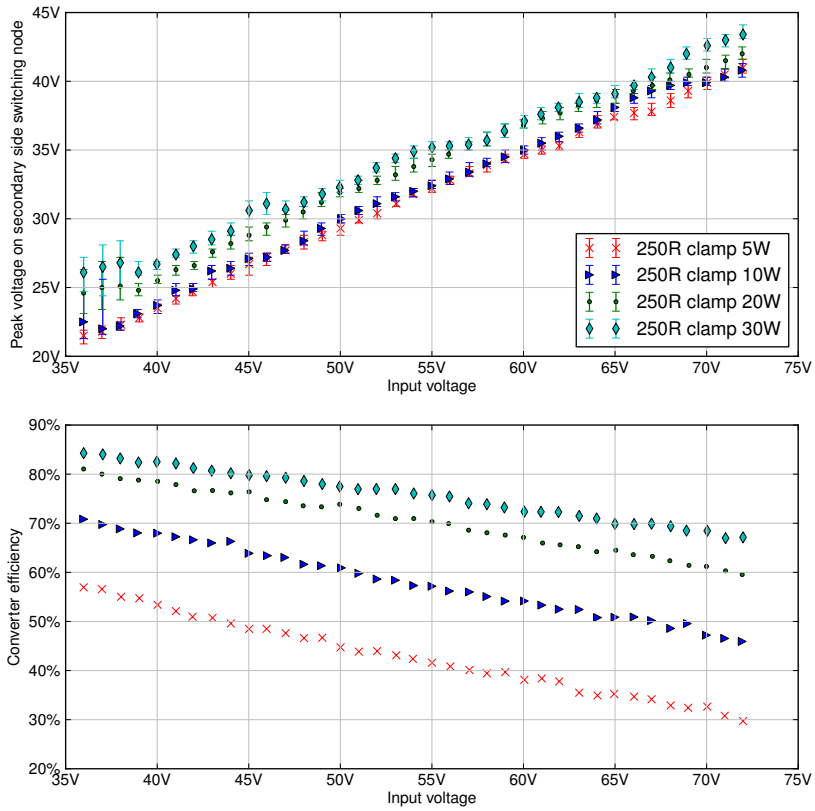


Figure 4.12: Average per-cycle peak secondary side voltages versus converter input voltage for different output loads with a 250 Ohm RCD clamp circuit, error bars indicate minimum and maximum value over a 10 s observation window (top), converter efficiency for the same measurements (bottom)

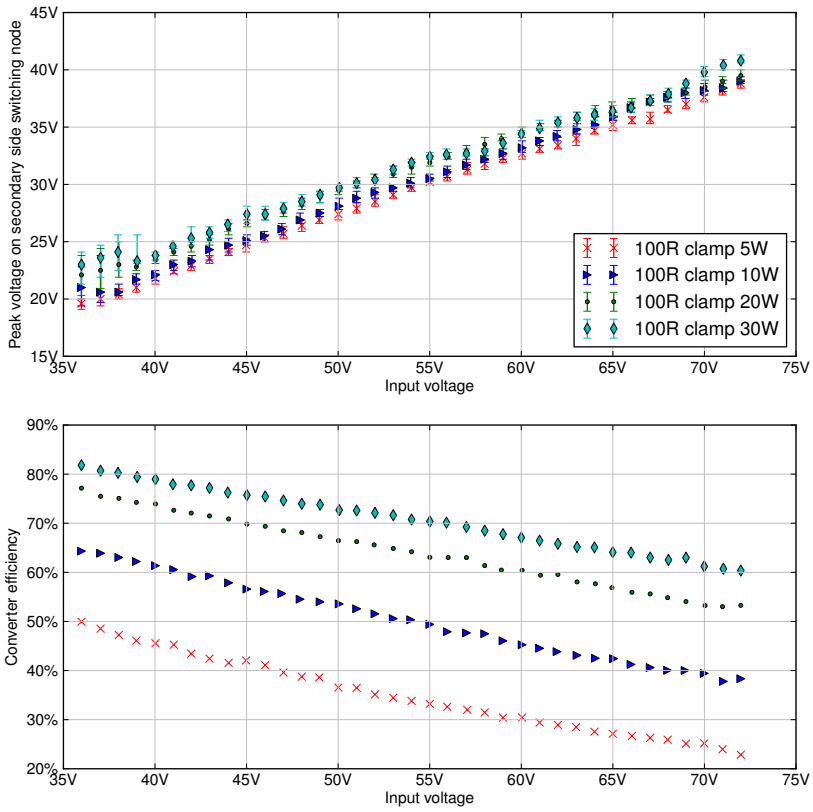


Figure 4.13: Average per-cycle peak secondary side voltages versus converter input voltage for different output loads with a 100 Ohm RCD clamp circuit, error bars indicate minimum and maximum value over a 10 s observation window (top), converter efficiency for the same measurements (bottom)

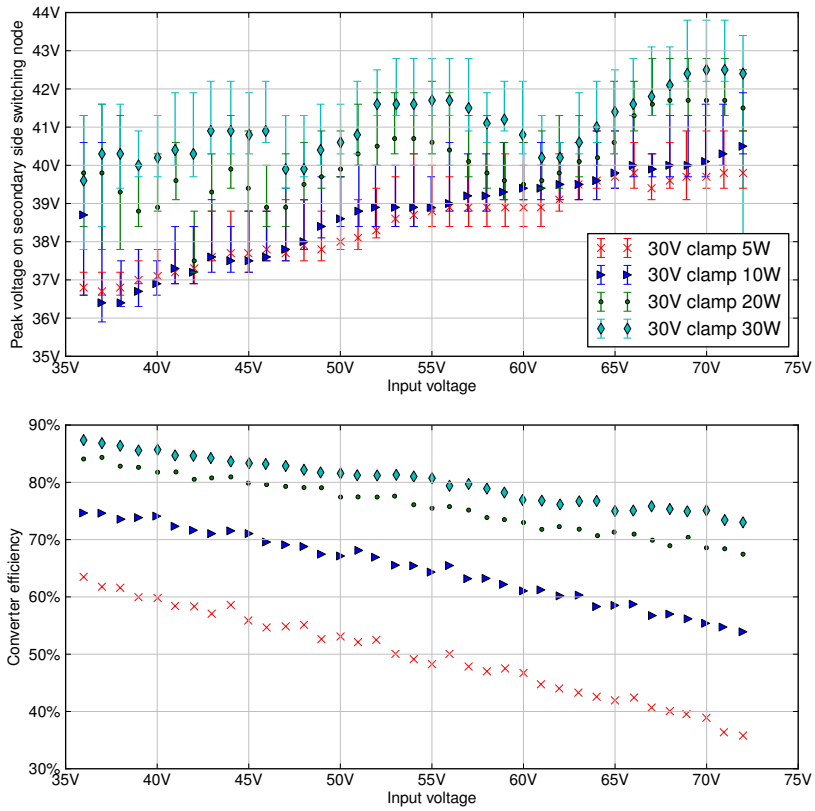


Figure 4.14: Average per-cycle peak secondary side voltages versus converter input voltage for different output loads with a energy recovering active clamp circuit using a 30 V Zener, error bars indicate minimum and maximum value over a 10 s observation window (top), converter efficiency for the same measurements (bottom)

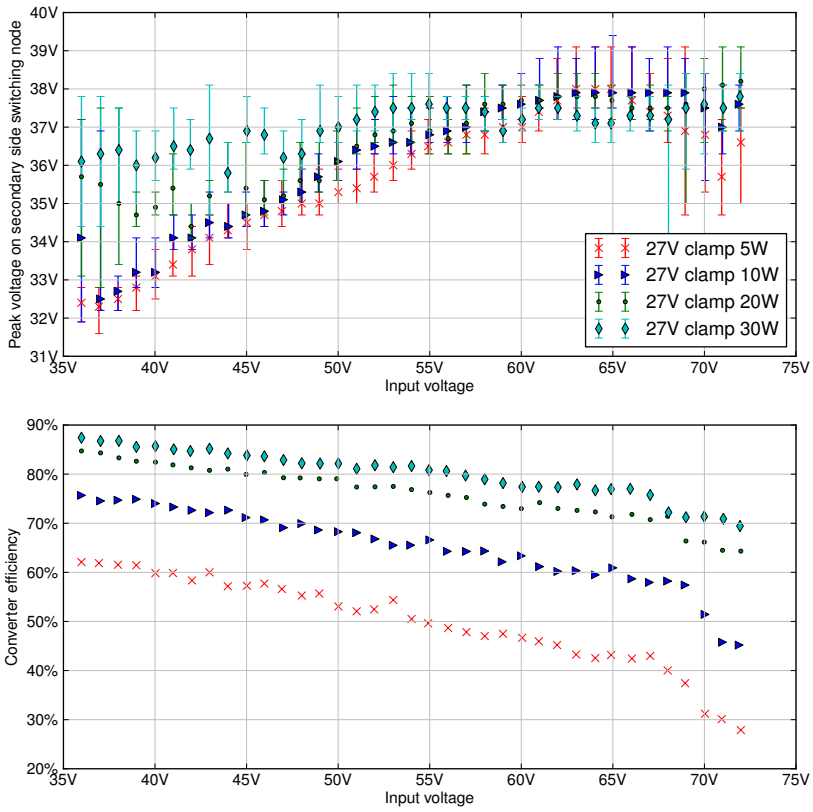


Figure 4.15: Average per-cycle peak secondary side voltages versus converter input voltage for different output loads with a energy recovering active clamp circuit using a 27 V Zener, error bars indicate minimum and maximum value over a 10 s observation window (top), converter efficiency for the same measurements (bottom)

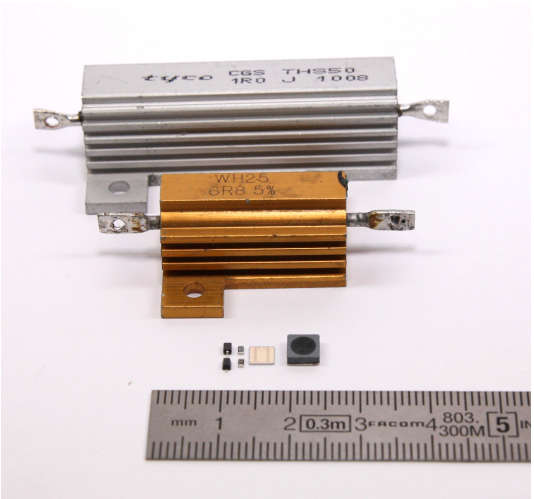


Figure 4.16: Size comparison of the components used in the asynchronous active clamp capacitor reset mechanism (bottom) and a Welwyn WH25 series (middle) and a Tyco THS50 series (top) resistor

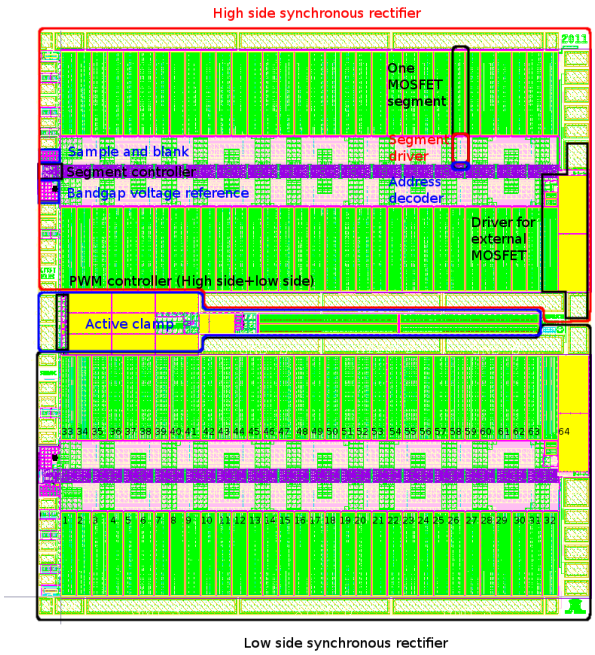


Figure 4.17: Layout plot of the SHARC ASIC

4.7 Conclusions

In this chapter, we have replaced the nearly ideal components of the previous chapter with more realistic approximations, with a number of additional parasitic elements. We have discussed the effects of these parasitic elements on the converter design considerations, waveforms and efficiency, and their impact on monolithic integration of high-power converters. Because we have identified the secondary side ringing – caused by parasitic inductors and capacitors in the transformer secondary, interconnects, as well as rectifiers – as a major roadblock in the efficient integration of these high-power converters, we have investigated the conventional approach of adding an RCD clamp circuit to the switching nodes, and have concluded that this does not offer an attractive solution for integrated converters.

As an alternative, we have shown that it is possible to use an asynchronous auxiliary converter to recover the secondary side ringing energy to the output. The asynchronous operation allows the use of a physically small and inexpensive inductor compared to other non-dissipative clamp circuits. Using the auxiliary converter, the clamping voltage can be accurately controlled, thereby improving the converter efficiency at low input voltages. Measurements using a commercially available buck converter IC as the auxiliary converter on a prototype full bridge converter confirm the voltage clamping abilities of the circuit and show a considerable improvement in efficiency when compared with RCD clamp circuits.

After this successful proof-of-concept, the energy recovering active clamp circuit was also implemented on a smart-power ASIC, together with integrated synchronous rectifiers. Unfortunately, due to an issue with the synchronous rectifiers, the clamp circuit could not be characterized with the recitifiers it was designed for. Instead, a comparison between several dissipative clamps and the energy recovering clamp circuit on a discrete synchronous rectifier, driven from the primary was performed. In this comparison, we included the performance of the clamp circuit, both in terms of voltage stress and converter efficiency, and the physical dimensions of both approaches to clamping. Although the parasitics in the secondary were larger than expected with integrated rectifiers, it was still possible to show a significant decrease in voltage stress on the devices under worst-case conditions, while optimizing the converter efficiency. Over the entire load and input range, the on-chip clamp circuit is able to decrease the voltage stress on the discrete rectifiers to within the 25 year lifetime safe operating area for the I3T50 technology, although this is at the limit of what the energy recovering clamp circuit can handle, and this can only be sustained for short bursts without leading to thermal run-away in the clamp circuit. Using somewhat relaxed voltage stress criteria, we see that the on-chip energy recovering clamp circuit can indefinitely decrease the voltage stress on the devices to a similar level as an RCD clamp using a bulky power resistor, that has several Watt of dissipation.

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5

Load-dependent efficiency optimization

5.1 Introduction

In the twentieth century, the electricity consumption in the standby mode of electrical appliances was nearly universally considered to be a non-issue by the end users, manufacturers, and regulatory agencies of electronic appliances. This point of view changed during the first decade of the twenty-first century, when the constant waste of several Watts or even tens of Watts per device was no longer considered to be acceptable. By 2010, the regulatory agencies in the European Union [1] had restricted the standby power consumption of most categories of electronic appliances to one Watt, with a further reduction to half a Watt starting from 2013. In the USA, a 2001 Presidential Executive Order [2] states:

> Each agency, when it purchases commercially available, off-the-shelf products that use external standby power devices, or that contain an internal standby power function, shall purchase products that use no more than one watt in their standby power consuming mode.

Actual regulation of the requirement to implement the low-power standby modes remained at the state level, with California leading the way by limiting the standby power of external power supplies to half a Watt starting from July 2007 [3]. With these limited power budgets, the manufacturers still strive to implement as much functionality as possible, so the efficiency of the power converters under low-load conditions becomes an important design criterion.

In the previous chapters on topology optimization and the analysis of the influence of parasitic elements on the converter, we have made the classic textbook assumption that the converter would be operating at or at least near the rated (maximum) power. This approach is not wrong, as in any practical converter, we need to consider the rated power as the main design parameter for the sizing of the primary switches, transformer, synchronous rectifier switches, filter components, and thermal management solutions. This is necessary because in absolute numbers the power loss, and therefore the thermally induced stress, reaches a maximum at this point. However, to be able to implement the desired functionality in standby mode, the converter design also needs to take into account the efficiency at the low-load condition of the power supply. In this chapter we will introduce the different loss mechanisms and show their relative impact on the total loss over the load range, followed by a discussion of different approaches that can be used to optimize the efficiency over a wide load range. From these approaches, we will select the most appropriate one for hybrid monolithically integrated converters, and highlight the design aspects of the implementation in the secondary side full bridge rectifier for a full bridge converter.

5.2 Loss terms in switching converters

Regardless of the converter topology and power range, a number of loss terms can be identified. Different classifications of the loss terms can be used, such as component based loss analysis and descriptive loss analysis. A component based loss analysis – where the total loss is determined for each individual component i.e. transistor, transformer, inductor, sense resistor, controller, capacitor, etc. loss – is important for the thermal management, thermal de-rating and life-time of each individual component. A descriptive loss analysis, where the loss is determined based on a functional description i.e. conduction loss, switching loss, and fixed loss can either be a further subdivision of the component based loss analysis, or can be used by itself to quantify the dissipation for the entire converter. Both these approaches are useful, but the functional description of the loss type can give the most insight in the possible modifications to the default converter for a load-dependent loss analysis and optimization.
In the functional loss description of switching converter applications, the power dissipation can be divided in fixed loss, conduction loss, and switching loss.

$$P_{total} = P_{fixed} + P_{conduction} + P_{switching}$$

The fixed loss P_{fixed} is the power consumed by the auxiliary or housekeeping circuits in the converter, such as an opto-coupler, clock generator, PWM generator, feedback network, etc. and the power lost in the leakage current through the power switches when they are switched off. As the name implies, the fixed loss is virtually independent of the switching frequency and the load power. The conduction loss is the loss caused by current flowing through the switches and the filter components, and is inversely proportional with the channel width of the MOSFET. Typically, the main contributing factors to the con-

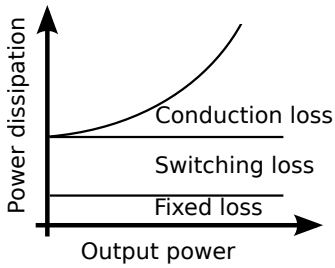

Figure 5.1: Power loss distribution in function of load power

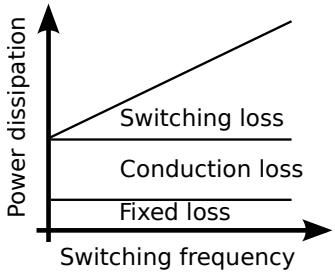

Figure 5.2: Power loss distribution in function of switching frequency

duction loss is the Ohmic loss in the MOSFET channel while the devices are turned on and the Ohmic loss in the inductor. The conduction loss is quadratic to the load current, and therefore the load power for a given output voltage, and independent of the switching frequency. The conduction loss in the MOSFET in function of the RMS current I_{RMS}, dimensions W and L, threshold voltage V_{th}, gate voltage V_{gs}, and technology constant K_1 is given by:

$$P_{conduction} = \frac{K_1 \times L}{W \times (V_{gs} - V_{th})} I_{RMS}^2$$

The switching loss $P_{switching}$ is the dynamic loss incurred at every switching cycle, which is caused by charging and discharging the parasitic capacitors in the switches, and is proportional with the channel width of the MOSFET and the switching frequency, and is independent of the load power. The switching loss in function of gate voltage V_{gs}, dimensions W and L, and switching frequency f_{sw}, and technology constant K_2 is given by:

$$P_{switching} = K_2 \times W \times L \times V_{gs}^2 \times f_{sw}$$

For the load-dependent optimization, there is very little we can change about the fixed loss, since in a good converter design this typically will be as low as possible while still achieving a sufficiently robust control loop. The conduction loss and the switching loss are mutually dependent, since the parasitic capacitor value and Ohmic loss in the switches

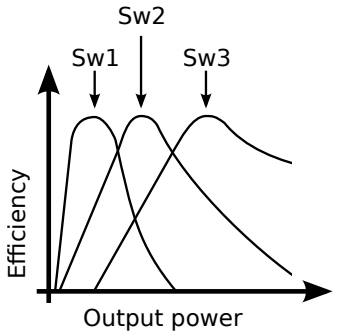

Figure 5.3: Efficiency of several switching power converters over the load range

are inversely proportional in a given technology for the same voltage rating. Therefore, a trade-off exists between these 2 types of loss, both in discrete and integrated converters. In discrete converters, these losses are balanced by selecting an appropriate number and type of the MOSFETs, while in integrated converters, the balancing of conduction losses and switching losses is done by selecting an appropriate channel width for the power devices. This trade-off results in an efficiency curve over the load range as shown in Figure 5.3 for converters that are optimized for different nominal load currents. Below the optimal load, for which the switching devices are sized, the switching loss dominates and efficiency is sub-optimal, since the switching loss for a given converter is virtually independent of load conditions, and the devices are larger than optimal for this load. Above the optimal load, the efficiency quickly begins to decrease, since the conduction loss for a resistive switch is quadratic in function of the output power and output current.

Despite the limitation that the switching devices must be sized for good efficiency at the rated load, a number of modifications can be made to the converter to improve the efficiency at low-load. All of these modifications will have an impact on the converter: either on the complexity, and therefore the cost, or on the performance of the converter in some load ranges. Whether this impact is acceptable will depend on the application in which the converter is to be used. In the following sections, we will discuss two broad categories of modifications that can be made to the standard converter topologies to improve the low-load efficiency, and their impact on the properties of the converter.

First, we will discuss the bypassing of the converter by auxiliary circuits to improve the efficiency for the low-load range. Second, we will systematically discuss modifications that can be made to the converter that have either been proposed in the literature or are used in commercially available devices. Finally, we will discuss a proof-of-concept and a smart-power implementation of the modification that is most appropriate for integration of a converter, where we have full control over the MOSFET and driver configuration. This proposed modification also can be used for the development of hybrid converters, where a low-power integrated approach is combined with the power handling capabilities of discrete power MOSFETs.

5.3 Bypassing the switching converter

If it is not desirable to make modifications to the switching converter to improve the low-load efficiency, it is possible to bypass and disable the converter under low-load conditions. This bypass can either be implemented as a linear regulator or as a separate auxiliary switching converter. The converter bypass, whether implemented as a linear regulator or a switching converter is not only useful for optimizing the efficiency of the converter at low-load, it can also be used in parallel with the main converter to allow for an increase in the permissible load range without exceeding the ratings of the individual components, especially under transient conditions or for input voltages that are relatively close to the output voltage.

5.3.1 Linear regulator bypass

In the topology optimization for smart-power converters in Chapter 3, we briefly touched upon the linear regulator for voltage transformation. Earlier, when we only considered the efficiency at the full load of the converter, the linear regulator was quickly discarded because of the limited overall efficiency. As was noted in the previous discussion, the theoretical efficiency limit is given by $\eta = \frac{V_{out}}{V_{in}}$, which is independent of the load current. However, for practical implementations an additional loss term caused by the quiescent current of the regulator must be taken into account. The quiescent current is the difference between the input current and the output current, and is caused by the power consumption of the housekeeping circuits, such as a power device driver, a band-gap voltage reference, error amplifier, over-current and over-temperature protection circuits, etc. In a first approximation, this additional loss term is proportional to the input voltage, resulting in a linear regulator efficiency of:

$$\eta = \frac{V_{out} I_{out}}{V_{in}(I_{out} + I_q)}$$

Because of this additional loss term, the already low efficiency of the linear regulator decreases even further for low-load conditions. However, since the control circuit in a linear regulator is relatively simple, the quiescent current to power the housekeeping circuit can be very low, i.e. less than $1.6\ \mu\mathrm{A}$ typical or $4\ \mu\mathrm{A}$ maximum for a high-performance MCP1700 [4] linear regulator. Even for standard low-cost regulators such as the LM317 [5] or LT1086 [6] the quiescent current is specified to be less than $10\ \mathrm{mA}$. For a high-power switching converter the fixed loss and the switching loss, which are not load-dependent, are typically larger than this loss.

Consequently, for low-load conditions, the linear regulator that was previously discarded for its low efficiency actually becomes more efficient than a switching converter that is optimized for high output power. By placing a linear regulator in parallel with a high-power switching converter, and implementing an appropriate enable or shutdown signal for each of the blocks in function of the load current, it is possible to optimize the efficiency of the converter system over a much wider load range than would be possible with any high-power switching converter. This principle is illustrated in Figure 5.4. Linear reg-

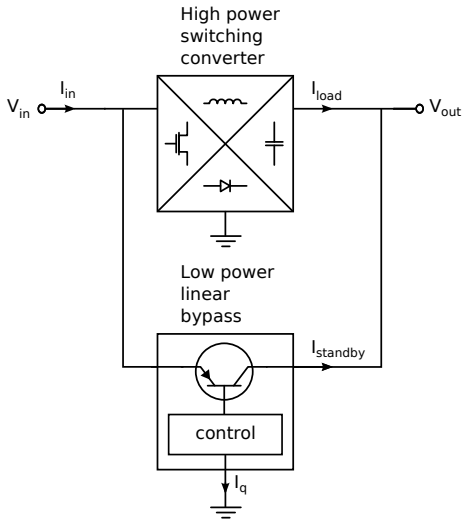

Figure 5.4: Linear regulator bypass of a high-power switching converter to optimize the low-load efficiency

ulators are simple, low-cost devices that require few external components to implement in a converter that uses discrete components, and for low output power the silicon area requirements for a smart-power implementation are relatively modest. Linear regulators tend to deliver an output voltage with an extremely low output ripple and good stability compared to switching converters, and therefore the implementation of this technique to improve the efficiency for low-load conditions is typically not limited by the type of load. Switching converters that use this technique to improve the efficiency for low-load or low input voltages are already commercially available, e.g. the Maxim MAX8989 [7]. Typical applications for this technique include battery-powered hand-held devices, such as mobile phones, where the input voltage is relatively close to the output voltage. For these applications, the inherent efficiency limits for linear regulators still allow for a reasonable efficiency of a linear regulator, so the loss at low output currents is relatively limited.

5.3.2 Switching converter bypass

The linear regulator bypass can significantly improve the efficiency at the lower limits of the load range, e.g. to allow a standby mode for a remote wake-up, although the useful range is limited. To increase the range where a bypass is useful, especially if the ratio of the input voltage to the output voltage is far from unity, a low-power switching converter can also be used in parallel with the high-power switching converter, as illustrated in Figure 5.5. Although this additional converter will still be a compromise between the switching and conduction loss, the reduced demands on this converter for the load current allow for reduced switching loss by selecting a smaller power transistor. Therefore, the

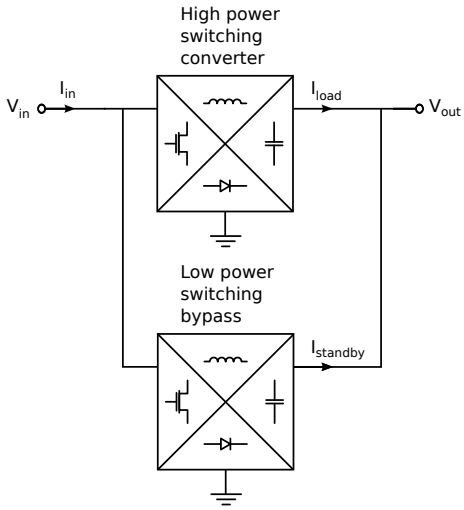

Figure 5.5: Low-power switching converter bypass of a high-power switching converter to optimize the low-load efficiency

efficiency curves for different converters as shown in Figure 5.3 may be combined to optimize the efficiency over a wider range.

5.4 Modifying the switching converter

Instead of disabling a high-power converter under low-load conditions and bypassing it with a low-power linear or switching converter as discussed in the previous section, it is also possible to dynamically modify a high-power converter in function of the load. To examine the possible mechanisms for these dynamic modifications, we will first examine the switching loss term in the switching converter in more detail. The switching loss term is caused by charging and discharging the various parasitic capacitors in the converter. Since the largest parasitic capacitors in a switching converter are typically the gate capacitors of the switching power devices, this can be illustrated by observing the charging and discharging process of the gate capacitor in every switching cycle, as shown in Figure 5.6. Any time the capacitor C, in this example C_{gate}, is charged from 0 V to V_{swing}, in this example V_{driver}, the final energy on the capacitor is given by:

$$E_{capacitor} = \frac{CV_{swing}^2}{2}$$

When a capacitor is charged by turning on the P-type transistor in the final stage of the driver, which allows current to flow from voltage source V_{driver}, the equivalent resistance of the P-type transistor only determines the charging speed, not the dissipated energy in

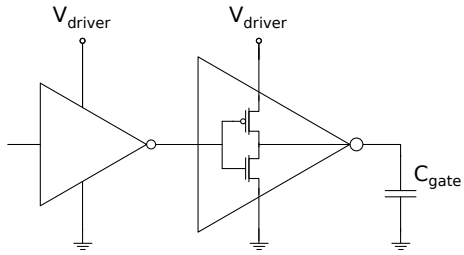

Figure 5.6: A 2-stage complementary MOSFET driver charging the gate capacitor of a switching power device

the driver. It can be shown that the energy loss in the driver circuit for charging a capacitor from a voltage source is equal to the final energy on the capacitor:

$$E_{loss,charging} = \frac{CV_{swing}^2}{2}$$

The discharging of the capacitor through the driver to ground is done by activating the N-type transistor in the driver, which is equivalent to connecting the capacitor to a 0 V voltage source, leading to the dissipation of all the energy in the capacitor in the equivalent resistor of the N-type transistor in the driver circuit. Similarly to the charging of the capacitor, the value of the equivalent resistor only influences the discharging speed, not the energy dissipation in the driver.

$$E_{loss,discharging} = \frac{CV_{swing}^2}{2}$$

Therefore, the dynamic power loss in charging and discharging a total of n parasitic capacitors at switching frequency f_{sw} is given by the equation:

$$P_{loss,charging+discharging} = f_{sw} \sum^{n} C_n V_{swing(n)}^2$$

Note that for MOSFET switches several of these capacitances are non-linear and voltage-dependent, so this linear equation should not be used for a direct calculation of the power loss. However, at an abstract level this equation shows that to reduce the dynamic power loss, either the (effective) switching frequency, the voltage swing over the capacitors, or the capacitor value needs to be reduced. In this section, we will show discrete and monolithic converter applications where one or more of these approaches are used, and discuss their potential impact on the efficiency of high-power high-voltage monolithic converters over the load range.

5.4.1 Effective switching frequency reduction

Concept

Because the switching losses are caused by the charging and discharging of the capacitors at each switching cycle, a first method for reducing the switching loss at light load is reducing the effective switching frequency. Although the amount of energy needed to charge and discharge each capacitor remains constant, a reduction of the effective switching frequency at light load corresponds with a reduction of the switching loss. However, as was mentioned in the introduction on switching converters, the selection of a high switching frequency allowed for using physically small filter components while still maintaining an acceptable filter performance, so reducing the effective switching frequency for low-load conditions will have an impact on the output ripple at low-load.
Broadly speaking, there are two approaches to reduce the effective switching frequency at low-load conditions. A first method is pulse skipping, where below a lower threshold load current a fraction of the clock pulses are blocked, e.g. one in every two or one in every three clock pulses are skipped, and the remaining pulses become correspondingly wider to maintain the same effective duty cycle. This corresponds with a decrease in the switching frequency proportional to the number of skipped pules, and therefore also with a proportional decrease in switching loss. A second method is using a so-called burst mode, where the switching frequency is maintained for a number of cycles until the output exceeds an upper threshold, followed by a complete suppression of switching pulses until the output drops below a lower threshold. The clock pulses and the resulting ripple of both of these approaches is illustrated in Figure 5.7.

Discussion

In many commercially available controller ICs, either one [8] [9] or both [10] of these methods for reducing the effective switching frequency is available to optimize the efficiency under low-load conditions. Obviously, this wide scale of implementation implies that these methods are effective for improving the low-load efficiency. However, both of these methods do have their drawbacks in the form of increased ripple on the output, and increased peak current in the switches and inductors if no additional measures are taken, and the application in which the converter is used needs to be able to tolerate this increased ripple for low-load conditions.
In pulse skipping mode, it is possible to accurately predict the frequency components of the ripple that can appear on the output, since it is known which ratios of skipped pulses are possible. Having known frequencies for the supply ripple makes it easier to filter these components in the load circuit, but limits the potential reduction in switching losses at low-load to the ratio of skipped pulses to the clock frequency. In burst mode, the effective switching frequency is dynamically adjusted in function of the load, and it is possible to optimize the efficiency over a very wide load range. However, this wide optimization range for the efficiency comes at the cost of a much less predictable switching frequency for low-load conditions, which is much more difficult to filter.

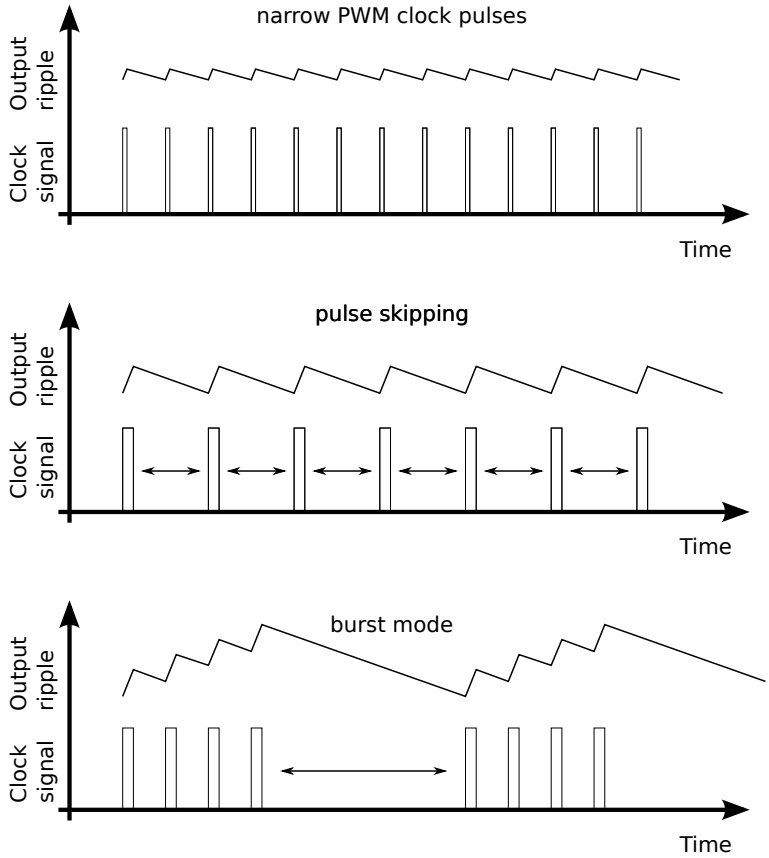

Figure 5.7: Illustration of the clock signal and output ripple when using pulse skipping and burst mode to optimize the low-load efficiency

For both approaches, the usability depends on the characteristics for the load. In some applications, such as converters for lighting applications [11] [12], the human observer sees a light stimulus as completely steady as long as the flicker fusion threshold is not reached, which is much lower than the switching frequency in modern high-frequency switching converters. This allows for the implementation of pulse skipping or burst-mode to significantly improve the low-load efficiency while still using small inductors and capacitors in high-frequency switching converters. In other applications however, such as in converters for telecommunications equipment, it is not feasible to reduce the effective switching frequency, since any switching noise in the signal range makes it virtually impossible to achieve the performance dictated by international communications standards. Therefore, we can conclude that although it is definitely possible to optimize the low-load efficiency through a reduction of the effective switching frequency, the applicability of this method is limited by the type of load.

5.4.2 Dynamic gate drive voltage optimization

Concept

As was noted in Chapter 3 in the discussion of using N-type power devices as high-side switches at a less than nominal gate voltage, a MOSFET power transistor can already be considered to be in the on-state at gate voltages that are significantly less than the nominal gate voltage. This does however correspond with an increase in the equivalent on-resistance of the transistor, and an increase in noise susceptibility of the power device. It was already shown in 2003 [13] [14] that for high switching frequencies the dissipation in a switching DC-DC converter can be reduced by driving the power devices with a gate voltage that is less than the nominal gate voltage for said technology. However, this optimization only takes into account the power dissipation in the driver stage, power stage and inductor, and assumes that any arbitrary voltage is available to provide power to the converter. While this is a reasonable assumption for an experimental converter in a lab setting, and does provide the most impressive improvement compared to a converter using the nominal gate voltage, for a stand-alone converter, the generation method of these auxiliary voltages also needs to be taken into account. In many applications, the DC current requirements for the gate driver are relatively limited, and the appropriate voltage is generated through a linear regulator from the output of the converter or an auxiliary winding on the transformer.
Because of the inherent limitation of the efficiency of linear regulators to $\eta = \frac{V_{out}}{V_{in}} = \frac{V_{driver}}{V_{aux}}$, the energy required to charge and discharge a gate capacitor C_{gate} for a given transition of drain-source voltage through a driver fed by a linear regulator from voltage V_{aux} is given by :

$$E_{capacitor,gate} = C_{gate} V_{driver} V_{aux}$$

Therefore, changing the gate drive voltage in an application with a linear regulator for providing the auxiliary voltage only gives a linear change in the switching loss with the gate voltage rather than a quadratic reduction in switching loss, as would be expected when

only taking into account the gate charge. By generating the gate drive voltage through an auxiliary switching converter, i.e. a buck converter driven from the output of the converter or an auxiliary winding, it is indeed possible to approach the switching losses described in [13] [14], where the auxiliary voltages appear out of thin air. However, this does come at the cost of increased complexity, since each auxiliary switching converter will also require control circuits, an inductor, filter capacitors, etc.

A possible method for the optimization of the converter efficiency over the load range would be the dynamic adjustment of the voltage that is used for driving the gate, depending on the load current [15]. Because of the quadratic relation between the conduction loss and the RMS current through the device, and the switching loss being virtually independent of the load current, the increase in on-resistance at low-load would be compensated by a reduction of the switching loss.

Discussion

Unlike the reduction in the effective switching frequency by implementing pulse skipping or burst mode, this approach to reduce the dynamic loss at low-load is not limited by the type of load and its tolerance to increased ripple and switching noise at frequencies below the nominal switching frequency at low output power. From the viewpoint of the load, a reduced gate voltage for the power devices at less than nominal output power does not change the output characteristics in terms of ripple or noise. However, the limitations of a dynamic gate voltage adjustment in function of the load are in the noise sensitivity of a MOSFET driven at a gate voltage that is less than the nominal voltage. Regardless of the load power, it remains undesirable to have the power MOSFET turn on or off at inappropriate times, so a sufficient noise margin is required over the entire load range.

In discrete power MOSFETs, most devices use a relatively thick gate oxide, with a threshold voltage between 2 V and 4 V and a nominal gate voltage of around 10 V. For specialty applications, so-called *logic level* MOSFET devices are available that use a thinner gate oxide, with a threshold voltage between 1 V and 2 V, and a nominal gate voltage of around 5 V, making these devices compatible with being directly driven by 5 V CMOS digital circuits [16]. This ratio of the threshold voltage to the nominal gate voltage in the range of 2.5 to 5 is typically seen as a good compromise between the on-resistance, the noise-margin in the on-state, and the leakage in the off-state. Similar ratios are observed in power devices for smart-power technologies, although typically with a nominal gate voltage equal to the supply voltage of the logic circuits, to ensure the power devices can be directly controlled by the on-chip devices. Broadly speaking, this corresponds with nominal gate voltage of 5 V for 0.7 µm technologies, over 3.3 V for 0.35 µm technologies to 1.8 V for 0.18 µm technologies [17]. Reducing the gate voltage below approximately twice the threshold voltage is generally considered to be counter-productive in gate voltage optimization, since the conduction loss rapidly increases below this value [15]. Depending on the technology, this allows for a potential reduction in gate voltage of 20 % to 60 % over the load range, if the optimal gate voltage at full load is the nominal gate voltage and the gate voltage can be reduced to twice the threshold voltage without com-

promising on the noise sensitivity and conduction loss at low-load.
Although generally speaking the MOSFET gate capacitor is highly non-linear, once the gate voltage has surpassed the Miller-plateau voltage, the equivalent gate capacitor is almost linear, which allows for a quick estimation of the order of magnitude of the potential gain in efficiency by dynamically adjusting the gate voltage over the load range. If a linear regulator is used for the generation of the auxiliary supply voltages, a 20 % to 60 % reduction in gate voltage over the load range approximately corresponds with an equally large reduction in switching loss at low-load. If a hypothetical lossless auxiliary switching converter is used for the generation of the auxiliary supply voltages, and under the same assumptions as with a linear regulator, this corresponds with a potential reduction in switching loss of 36 % to 84 %. When a realistic auxiliary switching converter is used to generate the reduced supply voltages, these values need to be multiplied with the efficiency of the auxiliary converter. Low-power, monolithically integrated converters typically have an efficiency in the order of 30 % to 90 % [18] [19], resulting in a reduction of the switching loss between 10 % and 75 % at low-load in the most optimistic case. Although a potential 75 % reduction in switching loss at low-load compared to full load is definitely not negligible, this depends on the condition that at full load the nominal gate voltage is the optimal voltage, and comes at the cost of a reduced noise margin, an increase in complexity, and the requirement to either provide an external inductor, or use significant silicon area to implement an inductor or switched capacitor based fully integrated converter.

5.4.3 MOSFET segmentation

Concept

The third parameter in the dynamic loss equation is the capacitor, which is charged during every switching cycle to a voltage, and is discharged to its initial value by the next switching cycle. Because the capacitance is directly linked to the dimensions of the power devices, this is typically a parameter that is fixed at design time by choosing the device dimensions that provide an optimal balance between conduction loss and switching loss. However, if a single power device in a converter is replaced by multiple devices in parallel, which can be independently controlled in function of the load current, it is possible to select which gate capacitors are charged and which gate capacitors remain at a fixed voltage during a switching cycle. Effectively, this corresponds with dynamically adjusting the gate width of the power devices in function of the load current.

Discussion

In the design of discrete converters, it is typically desirable to limit the number of power devices to a minimum, since the overhead introduced by the packaging, testing, and assembly of multiple power devices will typically lead to a larger and more expensive converter. However, for very high-power discrete converters, it is not unheard of to use multiple devices in parallel to satisfy or simplify the thermal management requirements.

Typically, the parallel power transistors are driven by identical gate signals to minimize the loss at full load, and the potential for a dynamic adjustment of the drive in function of the load is not used, since this requires multiple independent drivers, with additional overhead for each additional device.
In the design of monolithically integrated converters, where we have almost infinite degrees of freedom in selecting the dimensions of the power transistors, it is possible to optimize the converter for arbitrary output currents. The first derivative of the expression for the total loss in a power transistor for a variable width W is:

$$\frac{dP_{total}}{dW} = -\frac{K_1 L}{W^2(V_{gs} - V_{th})} I_{RMS}^2 + K_2 L V_{gs}^2 f_{sw}$$

Therefore, the power loss is minimized for:

$$W = I_{RMS}\sqrt{\frac{K_1}{K_2 V_{gs}^2 f_{sw}(V_{gs} - V_{th})}}$$

The optimal MOSFET width to minimize the power dissipation is thus a linear function of the RMS current through the device, for all other parameters remaining equal. Typically, the dimensions of the power transistors will be dictated by the maximum output current specifications, since this is the operating point with the maximum dissipation, and it is desirable to keep the efficiency at this point as high as possible. If the MOSFET width can be dynamically adjusted in function of the load current, the potential gain in efficiency over the load range only depends on the relative size and number of segments.
Contrary to discrete converters, the overhead introduced by using multiple independently controlled power devices in parallel instead of a single large power device is limited to adding isolation structures between the different power device segments and the drivers, and providing the appropriate control signals for each segment. Similar to adjusting the gate voltage in function of the load current, dynamically adjusting the transistor dimensions in function of the load current only influences the equivalent series resistance of the power transistor and the gate charge, and therefore this optimization approach is completely transparent towards the load.
Unlike a dynamic adjustment of the MOSFET gate voltage in function of the load current, where the change in gate charge and equivalent series resistance over the load range is fundamentally limited by the noise margin limitations combined with the non-linear relation between conduction loss and switching loss in function of the gate voltage, a segmentation approach allows for a wide range of optimization.

Controller based MOSFET segmentation

The potential for improving converter efficiency over the load range by using a segmented power stage was shown by Musunuri [20]. However, this work depends on an unspecified external controller to set the number of activated segments. An automated approach is described by Trescases in several publications [21–23]. Although automated, this work

depends on the availability of digital information about the load, or an estimation thereof, to determine the appropriate number of segments to turn on. For specific digitally controlled loads, such as switching audio amplifiers where a digital stream of data completely corresponds with the expected power consumption of the load this approach can work very well.
However, for more generic DC-DC converters, where power demands can not be predicted or estimated by a stream of digital data, a method for measuring or estimating the output power is required if the number of active MOSFET segments is to be optimized. In the next section, we will discuss the possible smart-power implementation forms for an automatic integrated controller to optimize the number of active segments, which does not require a stream of digital information about the load, and instead relies on an estimation or measurement of the current through the power MOSFET.

5.5 Automatic adaptive MOSFET segmentation

In a more typical DC-DC converter, where little to no a priori information about the load current is available, an alternative approach is required to optimize the number of active segments. The segment controller needs to select a (close to) optimal number of segments, without a stream of digital information from the load. Since the optimal number of segments is a function of the current through the MOSFET devices, any optimization scheme will require a measurement or an estimation of the current in the power path. First we will discuss a number of methods for estimating the current in smart-power converters, followed by a discrete proof-of-concept for an implementation of an automatic adaptive controller for MOSFET segments. Finally, we will conclude with the design considerations for a smart-power IC implementation of a synchronous rectifier with an automatic adaptive controller for the number of activated MOSFET segments.

5.5.1 Current estimation

In many converters, information about the load current is crucial for the implementation of the control loop or short-circuit protection to satisfy performance, reliability, or safety requirements. Therefore, a number of current estimation or measurement techniques have been developed over the years. We will discuss some of these techniques, and evaluate their potential implementation in a smart-power technology.
The most straightforward way to measure a current is measuring the voltage over a sense resistor in the current-carrying path, i.e. in series with the device through which we want to know the current. The voltage on the sense resistor is linearly proportional to the current, and provides an accurate representation of the current. However, by breaking the power path and inserting a dissipative element, the efficiency of the converter is somewhat reduced, since the voltage drop over the series sensing resistor must be significant compared to the noise for an accurate measurement of the current. However, the implementation of an appropriate current sense resistor on an smart-power IC is not im-

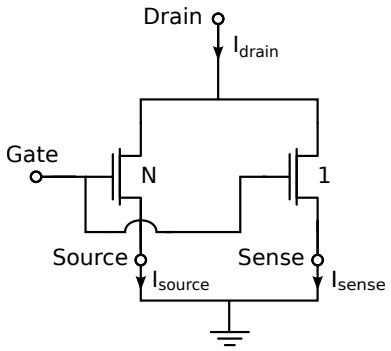

Figure 5.8: SenseFET equivalent circuit

mediately straightforward, since it is desirable for the current sense resistor to have a low, typically sub-Ohm value that is reproducible with a low temperature dependency, and is capable of sinking large currents. The combination of these properties is typically not available in integrated resistors, and any implementation with an integrated sense resistor is a compromise on one or more of these properties. Alternatively, a number of schemes have been proposed to circumvent the power loss in a series current sense resistor, which are typically described as *lossless*, since they do not rely on a resistor in series with the current path.

One possibility is the use of a so-called SenseFET [24], which is essentially a power transistor with an integrated current mirror. Each power MOSFET transistor is made of hundreds to thousands of identical transistor cells in parallel on a single die, to achieve a desirable equivalent on-resistance $R_{ds,on}$ for the total die. Since each transistor cell is identical, driven by the same gate voltage, and power MOSFET devices have an inherent temperature feedback that ensures current sharing in parallel devices, each of these cells has an identical drain-source current. By isolating the source connection of a fraction of these cells, and providing a separate sense connection to these cells, the sense connection functions as a current mirror, as shown in Figure 5.8, where the source current ratio to the sense current ratio is identical to the ratio of the number of cells N. For the SenseFET to function as an accurate current mirror, the potential at the sense terminal needs to be identical to the potential at the source terminal. In discrete SenseFET implementations this is typically achieved using an amplifier circuit, as shown in Figure 5.9, either implemented as a discrete circuit, or using a dedicated IC [25]. In a smart-power implementation, where power MOSFETs are also typically constructed from a number of cells in parallel, and the IC designer is responsible for defining the interconnects, an implementation of the SenseFET is technically possible, although a commercial exploitation may be subject to permission from, and payment of a licensing fee to, a number of patent-holders. Because the output of this amplifier circuit needs to be at a potential below the source potential to keep the sense terminal potential equal to the source terminal potential, and the source potential is at ground for a low-side switch, a negative supply voltage is required

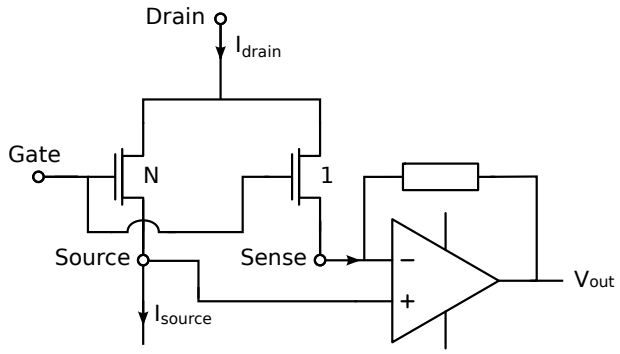

Figure 5.9: SenseFET current sensing circuit with amplifier

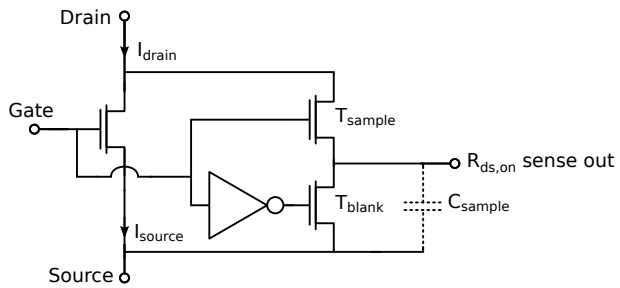

Figure 5.10: Sensing current by observing the MOSFET drain-source voltage drop over the channel resistance $R_{ds,on}$

for the amplifier circuit. As discussed in the introduction of the cost-efficient smart-power technologies that are available, any negative voltage in the circuit is undesirable in these technologies, as the substrate potential follows the lowest voltage in the circuit and increases the voltage stress on the entire die. Additionally, even though the SenseFET is typically described as a lossless current measurement, the actual dissipation depends on the specifics of the implementation and the desired accuracy, and can be comparable to a state-of-the-art implementation with a series resistor [26].

An alternative lossless method for estimating the current is measuring the voltage drop over the equivalent MOSFET channel resistance $R_{ds,on}$ while the transistor is turned on. The $R_{ds,on}$ sensing principle is illustrated in Figure 5.10. Contrary to series sensing resistors and SenseFET implementations, the $R_{ds,on}$ current sensing circuit is connected to a circuit node that is subject to large voltage swings. Since this sensing principle is based on the voltage over the power device, the input of the current sensing circuit needs the same voltage rating as the power device in the off-state. Since we are only interested in the voltage over the MOSFET while the device is turned on, it is not necessary to implement an amplifier or comparator circuit capable of processing the entire input voltage

range. Instead, the $R_{ds,on}$ current sensing circuit input can be implemented with a single high-voltage sampling transistor that is activated during the power MOSFET on-time, to pass the useful part of the signal, and is turned off during the power MOSFET off-time to protect the amplifier or comparator circuit from excessive voltages. Since the voltages that are to be measured in an $R_{ds,on}$ current sensing circuit are relatively small, practical implementations benefit from the addition of a blanking transistor that is turned on during the power MOSFET off-time to provide a low-impedance path to ground and to limit the susceptibility to noise. If further filtering of high frequency noise on the sampled drain voltage node is desirable, a small capacitor can be added to this node. To limit the dissipation by simultaneous conduction of the sample and blank transistors, appropriate delays are inserted in their respective control signals.

Of all these techniques, the $R_{ds,on}$ current sense comes closest to being lossless. Unlike the series current sense resistor, which causes some additional voltage drop in series with the device to be measured, and the SenseFET which redirects a fraction of the current, the $R_{ds,on}$ current sense is only observing a voltage drop over an already existing resistive element. This comes at the cost of a relatively limited accuracy in the measurement of the current, since the manufacturing tolerances for the MOSFET channel resistance are much larger than is feasible with a discrete sense resistor, although the accuracy of integrated sense resistors is also limited. Additionally, the $R_{ds,on}$ has a relatively high sensitivity to temperature, since increasing the temperature from room temperature to $120\ ^{\circ}\mathrm{C}$ approximately doubles the equivalent channel resistance.

If the limited accuracy is not an issue, the $R_{ds,on}$ current estimation technique is the most attractive to integrate in a smart-power converter, since it does not involve resistor values that are difficult to integrate, and no negative voltages are required for the processing circuit.

5.6 Proof-of-concept

To enable verification of the concept, and allow some initial real-life measurements, an experimental prototype of a boost converter was constructed using discrete components. The implementation uses 5 parallel MOSFETs (IRL510) at a switching frequency of 500 kHz. A simplified schematic for this circuit is shown in Figure 5.11. Measurements of the inductor current, the drain-source voltage, and the sampled-and-blanked drain-source voltage on a simple boost converter are plotted in Figure 5.12. As shown on the schematic in Figure 5.11, the sample transistor is connected to the switching node, allowing the drain voltage to be transferred to the sampling node during the power transistor on-time, and blocking the high voltage during the transistor off-time. The complementary control signal for the blanking transistor provides a low-impedance path to ground for the sampled signal, ensuring the voltage on the node does not experience undesirable spikes during switching transitions.

Since a segmented power stage does not have a fixed $R_{ds,on}$, the sampled voltage is not a linear representation of the drain current, and depends on the number of activated

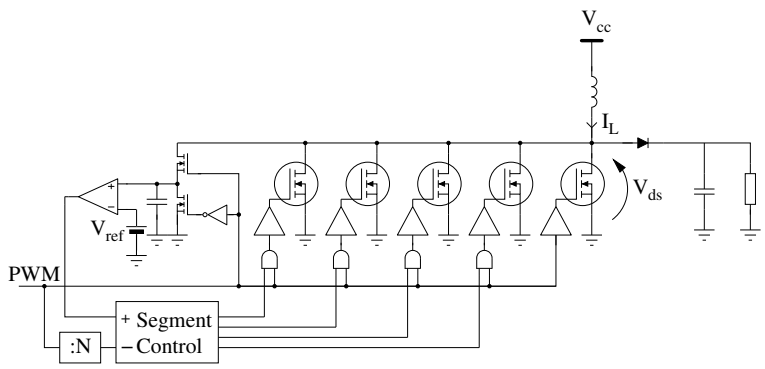

Figure 5.11: Schematic of a boost converter with segmented power stage

segments. However, the same property can be used to implement a simple control mechanism for an $R_{ds,on}$ current sense based segment controller, as shown in Figure 5.11. Since the optimal transistor width is linearly proportional to the drain-source current, and the equivalent channel resistance is inversely proportional to the transistor width, the transistor width where the conduction loss and the switching loss is balanced corresponds with a fixed voltage drop over the device.

By using a comparator to compare the blanked drain-source voltage with a well-chosen reference voltage V_{ref}, the comparator will generate a pulse every time the blanked drain-source voltage exceeds the reference level. For a well chosen reference voltage, this level corresponds with a situation where the conduction loss is greater than the switching loss, and the segment controller can use this pulse as a signal that one or more additional segments need to be activated to minimize the total loss. The activation of additional segments then increases the effective width of the transistor and decreases conduction loss, at the cost of a somewhat increased switching loss.

If a sufficient number of segments are activated to keep the blanked drain-source voltage below the reference voltage, the segment controller no longer receives these pulses, and no additional segments are activated. Since with this control circuit overcurrent pulses are only generated when too few segments are activated for the actual current through the device, the segment controller periodically (every N clockpulses) deactivates a segment to check whether the sampled drain-source voltage exceeds the reference voltage. If this checking mechanism is performed on a relatively large time-scale, i.e. N is large, this checking mechanism only has a low impact on the converter efficiency, since the generation of an overcurrent pulse immediately activates an additional segment and the situation is restored to the previous state.

In the prototype discrete boost converter, the segment controller is implemented as a microcontroller that generates appropriate clock pulses for a bi-directional shift register, with digital zeroes shifting in from one side and digital ones from the other side. This allows for both manual and automated control of the number of activated segments. The

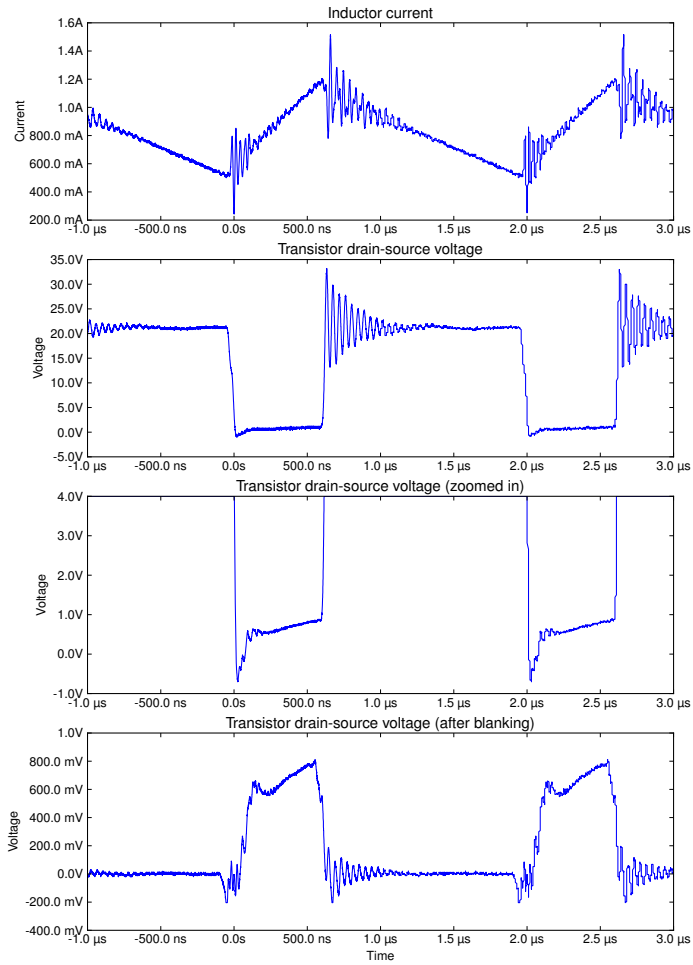

Figure 5.12: Some key waveforms in the $R_{ds,on}$ current sense technique for a simple boost converter

sequence of events for a sudden increase in load current with the automated control is shown in Figure 5.13. At the beginning of the sequence, only one segment is activated. Since this segment is always on, no control bit is required for this segment, whereas each additional MOSFET segment is represented and controlled by one bit in the shift register. As soon as the sampled drain-source voltage exceeds the reference voltage, the comparator is tripped, and the direction of the shift register is reversed. At the next clock pulse, which is in this case generated by the microcontroller, a one is shifted in the bit register, and an additional segment is activated. Because the load current step in this case is large enough to require more than one additional segment to be activated to restore the drain-source voltage, additional overcurrent pulses continue to be generated until all 5 segments are activated. Once this is achieved, the blanked drain-source voltage is approximately at the same level as before the sequence of events. This corresponds with the measured inductor current, which was at an average of $400\ \mathrm{mA}$ with one activated segment, and is at approximately $2\ \mathrm{A}$ with all 5 segments activated. Even with a relatively slow microcontroller and a sequential process for controlling the shift register that selects the activated segments, this segment controller can respond to a large load step in a timeframe of hundreds of microseconds.

Measurements on the prototype converter confirm the optimization of the efficiency over the entire load range. At a switching frequency of 500 kHz, the segment controller automatically selects the optimal number of segments to optimize the power loss in the converter when the reference voltage is set to 200 mV. Measurements of the efficiency over the output load range with a fixed number of segments and with the automatic segment selector are shown in Figure 5.14.

As can be seen on the graph, the segment controller is capable of activating the appropriate number of segments to optimize the efficiency, however the gain in efficiency is relatively limited because of the use of only 5 identical segments. For a discrete implementation, the relatively limited gain in efficiency is unlikely to warrant the additional complexity of adding the required circuit components, such as the sample-and-blank circuit, a comparator, a reference voltage generator and the segment controller logic. Therefore it is not likely that controller ICs that allow the independent use of multiple parallel power devices in function of the load will become commercially available, even though it is technically possible to implement this approach.

5.7 ASIC implementation

In the world of smart-power converters, with integrated power devices on the smart-power IC, many of the drawbacks of a discrete implementation are much less relevant, as the silicon area required to implement the auxiliary circuits is very limited when compared to the power stage, i.e. the area consumed by the drivers and MOSFETs. Since the power MOSFET and driver devices in a smart-power converter no longer have the overhead from packaging, testing, and handling of each individual device, the main source of overhead introduced by segmenting the power stage in a smart-power converter is in the isolation

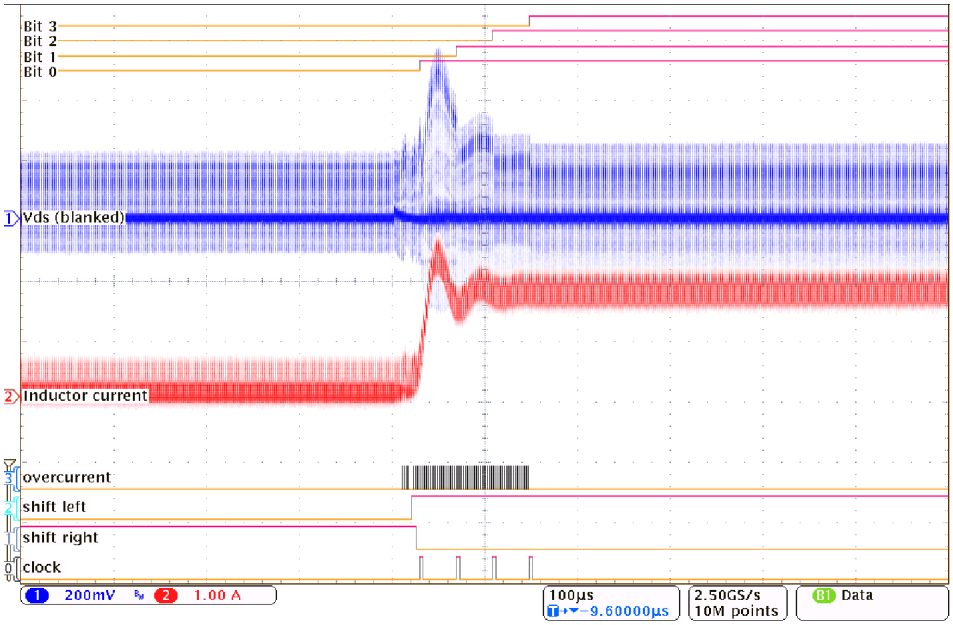

Figure 5.13: Transient response during a sudden increase in load current for the proof-of-concept boost converter with segmented power stage. Each Bit x represents one activated MOSFET segment

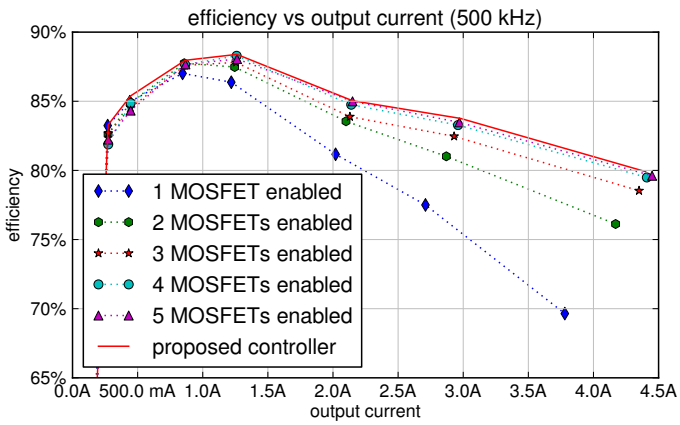

Figure 5.14: Efficiency of a prototype boost converter with a fixed number of MOSFET segments and with the automatic segment selector

structures which are needed between individual segments and between the drivers for each segment. Fortunately, for modern smart-power technologies that use DTI (Deep Trench Isolation) structures for isolation between devices, where a trench is etched in the silicon and filled with a dielectric, these isolation structures can be very area-efficient compared to the dimensions of the power devices. This limited overhead allows for a much larger number of segments than is economically and physically viable in discrete implementations, without significantly affecting the cost of the system, when compared to a non-segmented implementation. This obviously allows for a better optimization of the transistor width under different load conditions.
For the ASIC implementation a phase shifted full bridge converter application, with a $36 - 72$ V input range to a 12 V output and switching at 1 MHz was selected. The load-dependent efficiency optimization scheme was implemented on the secondary side full bridge synchronous rectifier.
The basic schematic of a phase shifted full bridge converter with a segmented synchronous full bridge rectifier is shown in Figure 5.15. Because a full bridge rectifier consists of 2 identical half bridges, only a half bridge, i.e. one leg of the full bridge is implemented per ASIC to reduce prototyping cost. Thus, a single ASIC contains both a segmented high-side and low-side MOSFET, the necessary drivers and PWM generator circuits, together with all electronics to control the MOSFET segments.

5.7.1 Power stage dimensioning

The ASIC was designed for load currents up to 3 A using the integrated power MOSFETs. The selected smart-power technology for this application is the ON Semiconductor I3T50 (50 Volt, 0.35 µm) technology [27] [28], since this technology has the appropriate technical qualifications and is available through the Europractice MPW service [17] for prototyping.
In the I3T50 technology, the most area-efficient (with the lowest Ωmm^2 product) implementation is achieved for an N channel high-voltage MOSFET with a channel width of 10000 µm divided over 20 fingers. For the low side switch, the N channel MOSFET is the default choice. For the high side switch, the use of an N channel MOSFET with an external bootstrap circuit minimizes the silicon area requirements, and only slightly increases the system size, as discussed in Chapter 3. Devices with larger channel width are implemented using multiple of these optimally sized segments in parallel. This optimum size is caused by the build-up of the devices, because even though the high-voltage N-channel devices are vertical MOSFET structures, the drain contact is brought back to the surface through a buried layer and a sinker contact. Smaller devices than these optimal dimensions have an electrically short horizontal distance between the drain and source, and have a lower channel resistance, but a relatively large area is lost through the overhead introduced by the drain contacts. For devices larger than these dimensions, the electrical distance between the sinker contact at the drain and the source contacts becomes increasingly larger and the additional series resistance is no longer compensated for by the drain contact overhead. Because the design rules require that each segment is sur-

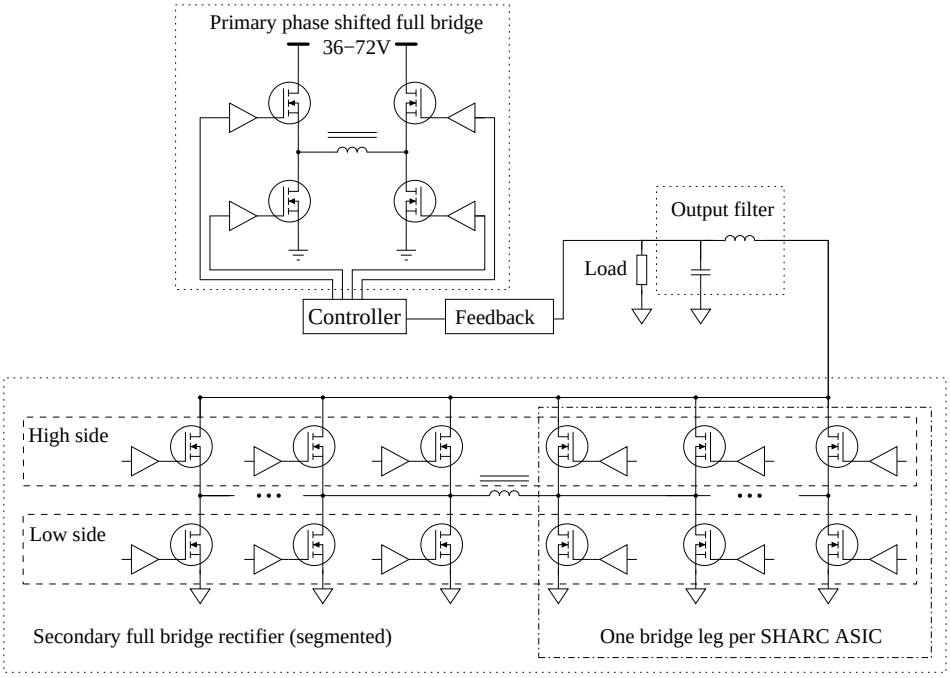

Figure 5.15: Schematic for a phase shifted full bridge converter with a synchronous full bridge rectifier

rounded by sinker and isolation structures, a segmentation with a power device channel width of $10000\ \mu\mathrm{m}$ introduces no overhead in the area requirement for the power transistors. In contrast, no such limitations exist for the low-voltage devices used in the tapered buffer driver for the power MOSFET, so a segmentation of the buffers will introduce some overhead by the requirement to provide isolation structures between each driver segment. Fortunately, the I3T50 technology uses DTI to isolate different parts of the circuit from each other, which is a very area-efficient approach [28], and relatively little overhead is introduced by segmenting the drivers.

Since a MOSFET channel width of $10000\ \mu\mathrm{m}$ corresponds with the most area-efficient implementation, and because the silicon area requirements are mainly determined by the power MOSFET dimensions, all segments are chosen to be of this most area-efficient size, and are thus equal. This has the advantage that each segment is identical, and can also use an identical tapered buffer as a driver, which simplifies the design process.

5.7.2 Optimal segmentation

For a $3\ \mathrm{A}$ output specification, as mentioned above, a good compromise between the power efficiency of the converter and the required silicon area is achieved around $600\ \mathrm{mm}$ of channel width, which corresponds with approximately 60 optimally sized segments per MOSFET. Since this already corresponds with a large optimization range over the load range, no further subdivision of these segments was performed, as this would lead to reduced area efficiency for a relatively small gain in the granularity of the optimization.

Each of these segments needs to be controlled by a PWM signal, and the routing of a separate PWM signal for each segment from a single central controller would become impractical. Therefore, a different approach is used: instead of generating the control signals for each segment from a single central segment controller, the output of the central controller is a digital bus that represents the number of activated segments, and the actual generation of the PWM signals is performed at the location of each individual driver per segment. Using this method, a 6-bit bus suffices to control the segment activation for up to 64 segments, which can be easily routed and amplified over the dimensions of the ASIC.

To achieve this, each segment is equipped with an address decoder block to provide the PWM signal to the driver. To simplify the layout, each address decoder block is identical, and the blocks are designed to be chained together back-to-back. The address decoder has 2 6-bit inputs and a 1-bit input, and 2 6-bit outputs and a 1-bit output. The first 6-bit input is the value generated by the segment controller, which is buffered and passed through to the next address decoder, using the first 6-bit output. The value on the second 6-bit input bus is used as the local address of the segment, the address value is incremented with 1, and placed on the second 6-bit output bus, for use by the next address decoder in the chain. The 1-bit input is connected to a global PWM signal, which is identical for all segments. If the local address of the address decoder is less than or equal to the value on the bus generated by the segment controller, the global PWM signal is passed through to the respective segment. If the address value is larger than the bus value, the PWM signal is suppressed, thereby disabling the segment.

Although the power MOSFETs in the I3T50 technology are high-performance devices, for increasing power levels it becomes less desirable to continue to increase the silicon area to accommodate more segments of the power devices, since doubling the current requires 4 time the silicon area for the same conduction loss, and the switching loss is approximately proportional to the silicon area. Since the dissipation in a smart-power IC is typically more limited by the thermal limits of the packaging than by the silicon area of the IC, it makes sense to implement a hybrid form between the integrated and the discrete converter for high-power levels. In this configuration, the integrated power MOSFETS, which are segmented to provide good low-load efficiency are complemented by one or more external MOSFETs that are driven by integrated drivers for high loads, thereby extending the output range beyond the output current for which the internal MOSFETs are designed. This possibility was foreseen on the IC by implementing the final segment as a high-voltage driver for an external MOSFET instead of as an additional internal MOSFET segment.

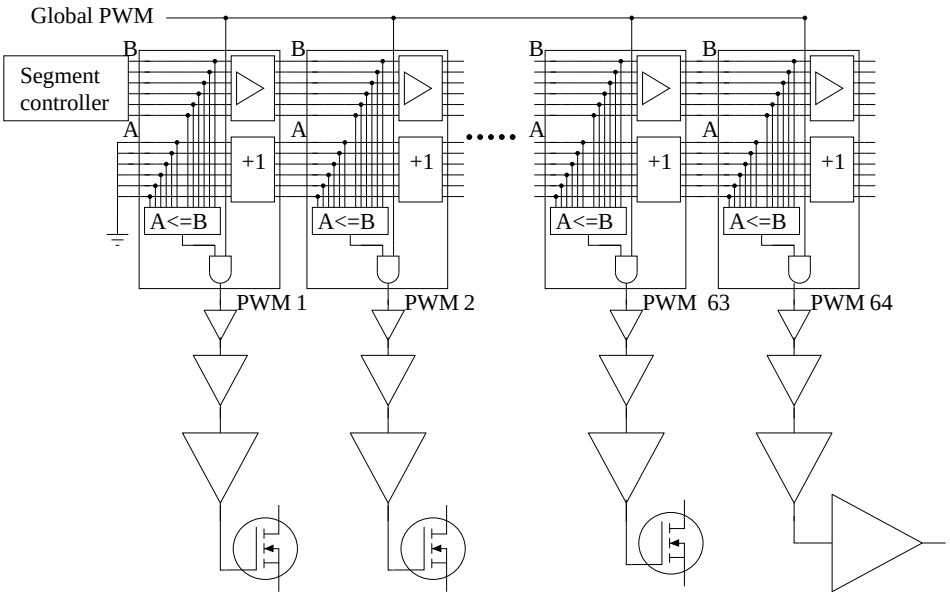

Figure 5.16: Segment addressing: PWM1 to PWM63 control integrated MOSFET segments, PWM64 controls a high-voltage driver for an external MOSFET

This allows for using the same address decoder block for the regular MOSFET segments and the high-voltage driver for the external MOSFET. For the SHARC ASIC implementation, the entire 6-bit bus was used, although this is not a strict requirement. The internal MOSFET is divided in 63 segments, which are assigned to the first 63 addresses, while the external MOSFET driver is assigned address #64. To ensure a safe start-up, even with a live load where significant current is drawn from the converter as soon as it turns on, the reset for the segment controller activates all segments on power-up. The addressing scheme is illustrated in Figure 5.16.

5.7.3 Optimized driver size and gate voltage

Since all segments and drivers are chosen to be identical, a single optimization of the driver dimensions and driver voltage is sufficient. Because the total dissipation is at a peak for the maximum output power, it was chosen to optimize the driver for the full load current of approximately $3\ \mathrm{A}$ and under worst-case conditions, where all segments are activated to minimize the conduction loss. For a total of around 60 segments for $3\ \mathrm{A}$ drain-source current, this corresponds with each segment being optimized for $50\ \mathrm{mA}$ of drain-source current, while switching a drain-source voltage of twice the nominal output voltage. This corresponds with the full bridge rectifier with a $36 - 72\ \mathrm{V}$ input range, as discussed as the $12\ \mathrm{V}$ output test-case of chapter 3 being operated at the maximum input

voltage. Because of the dependence of the MOSFET channel resistance on the temperature, and the MOSFET self-heating is most prevalent at high currents, the simulation temperature for the optimization of the driver stage is set to $127\ ^{\circ}\mathrm{C}$. Because of the relatively high switching frequency of $1\ \mathrm{MHz}$ for the high-voltage devices, the supply voltage of the gate driver and therefore also the MOSFET gate voltage was included in the optimization for the driver for each MOSFET segment.

The power MOSFET gate represents a relatively large capacitor that needs to be charged and discharged in a very short time to limit the transition time between the transistor being in the on-state and in the off-state, and therefore the driver needs to be able to deliver large currents to avoid excessive power dissipation in the power MOSFET. Obviously, the minimally-sized outputs of the logic cells that generate the PWM control signals can not deliver enough current for any reasonable switching frequency for the large power devices. Therefore, a tapered buffer consisting of consecutive stages of increasingly larger inverters, of which a 2-stage version is shown in Figure 5.6 is used to increase the drive strength of the logic circuits to an appropriate level. The final inverter stage should be able to deliver the required gate current for a rapid transition of the power MOSFET through the linear region, while the input capacitance of the first stage should be sufficiently small to be driven by minimal-dimension logic circuits. Exactly as in the actual power devices, the devices in the buffer itself should balance the conduction loss and the switching loss, since even though a larger final stage can deliver more current to the MOSFET gate to minimize the loss in the linear region, this causes additional loss because a larger gate capacitor needs to be charged by the previous stage.

In nearly all tapered buffers, a constant *taper factor* is used for consecutive stages, as this evenly distributes dissipation and delay over the stages. Depending on the application and which side-effects are taken into account, several different values have been proposed in literature, ranging from $e \approx 2.72$ to over 20 [29] [30]. Typically, a factor close to e minimizes the delay, while larger factors minimize the energy and area requirements for the buffer for high switching frequencies.

In this application, a minimum dissipation in both MOSFET and driver, combined with a reasonable area-efficiency was desirable, and the sizing of the transistors in the tapered buffer was performed using a parametric sweep using a worst-case simulation test-bench.

For the synchronous rectifier operating at $1\ \mathrm{MHz}$, this optimization leads to a 6-stage tapered buffer, with a total dissipation of approximately $7\ \mathrm{mW}$ per segment in the power device and the buffer combined. The channel widths for the individual devices are listed in Table 5.1, all gate lengths are minimal length $0.35\ \mu\mathrm{m}$, and the optimum dissipation is achieved at a driver voltage of $2.3\ \mathrm{V}$. As can be noted from the table the optimization resulted in approximately $2000\ \mu\mathrm{m}$ channel width for the final stage N-type device, taper factor 4 and a width ratio of 3 between the P-type devices and the N-type devices, to drive a high-voltage power MOSFET with a channel width of $10000\ \mu\mathrm{m}$. In silicon area, this corresponds with a high-voltage MOSFET segment of approximately $50000\ \mu\mathrm{m}^2$ combined with a driver of approximately $18000\ \mu\mathrm{m}^2$.

Simulations confirm that for a $1\ \mathrm{MHz}$ switching frequency, with an optimized driver size and constant gate drive voltage, the total power dissipation in the driver and power MOS-

Stage	N-type width (μm)	P-type width (μm)
6	2048	6144
5	512	1536
4	128	384
3	32	96
2	8	24
1	2	6

Table 5.1: Dimensions of optimized tapered buffer for 1 MOSFET segment (W=10000 μm) in the ASIC synchronous rectifier

Transistor	Channel width (μm)	Channel length(μm)
P1, P2, P3	1	3.5
P4, P5	30	10
N1, N2	30	6
N3	35	.35

Table 5.2: Dimensions of transistors in comparator

FET is minimized when the number of active segments is a linear function of the current. For each doubling of the current, approximately double the number of active segments leads to a minimum total dissipation. The simulated data for a nominal case 63-segment MOSFET and driver combination and the required digital and analog circuit is plotted in Figure 5.17. The data points of selected data-sets are represented by markers, while the solid line shows a best linear fit for the optimal number of segments for all data-sets, including those that were omitted in the graph for clarity. Because of the static power consumption of the analog and digital circuits that are required to control the segments, the dissipation never becomes zero, even for the no drain-source current situation. As can be seen in the plot, for a $40\ \mathrm{mA}$ current, the dissipation with the optimal number of segments activated compared to all segments activated is significantly reduced from $133\ \mathrm{mW}$ to $85\ \mathrm{mW}$, or a reduction of 36%, which includes the dissipation in the supporting circuits that provide the segmentation ability.

This optimum point corresponds with approximately $20 - 25\ \mathrm{mA}$ per activated segment in the typical case. The R_{on} per segment for $2.3\ \mathrm{V}$ gate voltage is approximately $2\ \Omega$, therefore the output voltage from the integrated $1.2\ \mathrm{V}$ bandgap reference is passed through a resistor divider to obtain an on-chip reference voltage which causes the comparator to trip at a drain-source voltage in the on-state of approximately $40 - 50\ \mathrm{mV}$. For the comparator, for which the schematic is shown in Figure 5.18, the transistor dimensions are listed in Table 5.2. To reliably trip the comparator at $40 - 50\ \mathrm{mV}$ in the available on-time at the desired drain-source voltage, the reference voltage is set to approximately $40\ \mathrm{mV}$.

As mentioned in the discussion of the discrete prototype, when a comparator is used to

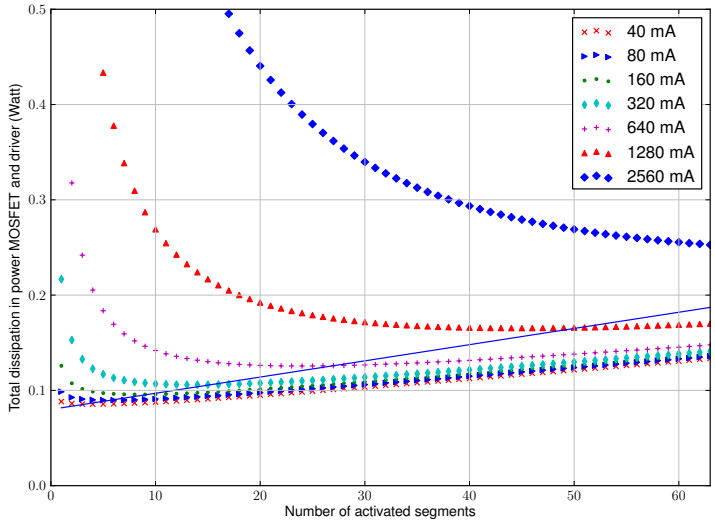

Figure 5.17: Power dissipation in MOSFET and drivers in function of the number of activated segments for different load currents

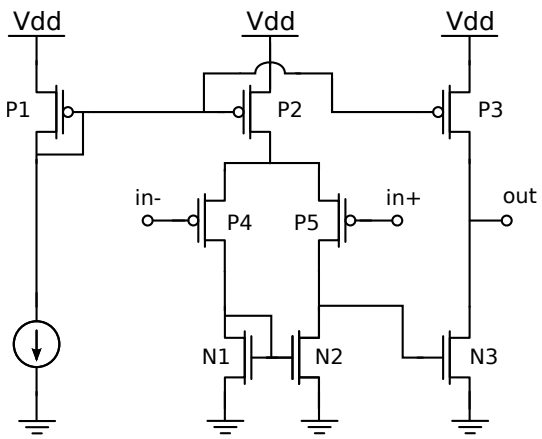

Figure 5.18: Comparator circuit for the smart-power implementation of $R_{ds,on}$ based current sensing

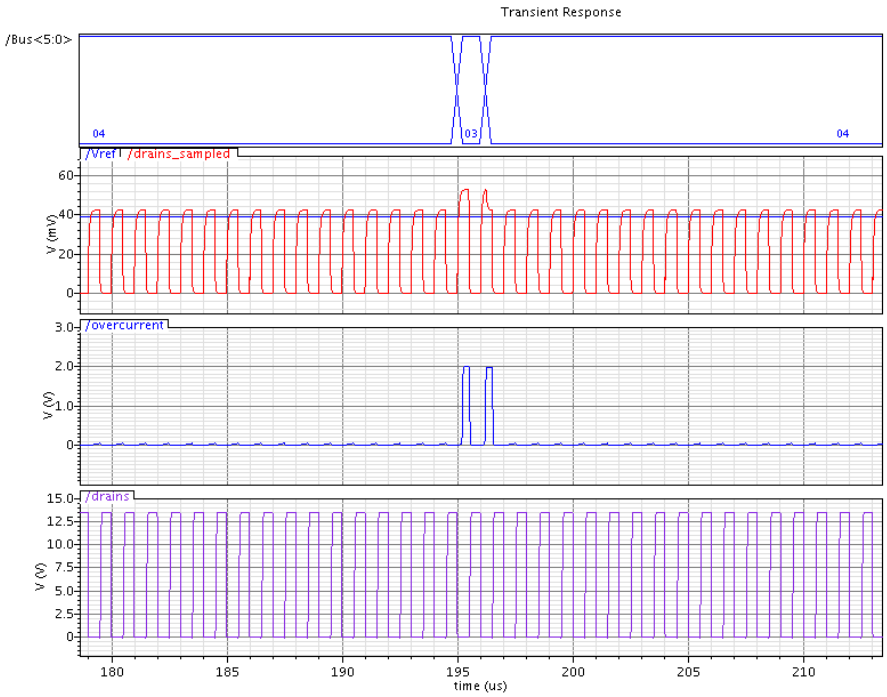

Figure 5.19: At t = 195 μs, the segment controller deactivates a segment to detect a possible decrease in current, the comparator triggers and the segment controller immediately reactivates the segment

verify whether the drain-source voltage exceeds a reference voltage and the comparator output is used by the segment controller to activate additional segments, a reduction of the current can not be detected. To overcome this, on a large time-scale the segment controller periodically deactivates a segment to verify if the current through the device has not decreased sufficiently to allow operation with less segments.

In Figure 5.19, the sequence of events is shown for a constant current of $100\ \mathrm{mA}$. With the 6-bit digital value $Bus < 5:0 >$ representing the number of activated segments, with value 00 being equal to 1 active segment, the voltage drop over these 5 parallel segments is approximately $42\ \mathrm{mV}$, which is not sufficient to trigger the comparator before the signal is blanked again. At t=195 µs, the segment controller deactivates a segment to detect a possible decrease in current, increasing the voltage drop over the 4 remaining active segments to $52\ \mathrm{mV}$. This is sufficient to trigger the comparator in the time-frame of the switching cycle, and the segment controller immediately reactivates the segment.

Transistor	Channel width (μm)
N1	2
P1	6
N2	8
P2	24
N3	32
P3	98
N4	128
P4	385
N5	516
P5	1534
N6	10000
P6	20203
N7,N8	512
P7	384
P8	2048
P9	480
P10	64

Table 5.3: Dimensions of transistors in high-voltage driver for external MOSFET

5.7.4 High-voltage driver for external MOSFET

As mentioned earlier, the possibility was foreseen to extend the load range with an external power MOSFET, which is activated when the segment controller detects that the maximum efficiency operating point for all integrated segments working in parallel is exceeded. Since most discrete power MOSFETs are designed for gate voltages of either 5 V for logic level devices, or $10 - 15$ V for regular power devices, the driver for the external MOSFET was designed for a high-voltage output, with an externally applied supply voltage for the high-voltage driver. This allows for a wide variety of external discrete power MOSFETs to be controlled by the integrated driver. To reduce the area requirements for the high-voltage driver, most transistors of the tapered buffer are implemented as low-voltage devices to directly drive the gate of the final N-stage high-voltage MOSFET. The final P-stage high-voltage MOSFET gate is driven by 2 level shifters, one to turn on the device and another to turn off the device. The schematic for the high-voltage driver is shown in Figure 5.20, the device channel widths are summarized in Table 5.3, all gate lengths are minimal length, i.e 0.35 µm for the low-voltage devices, and the fixed default value for the high-voltage devices. Transistors N6, N7, N8, and P6 are high-voltage devices, capable of switching well over the 20 V gate voltage limit for most discrete power devices, although a more typical 12 V gate drive was assumed in the optimization of the dimensions.

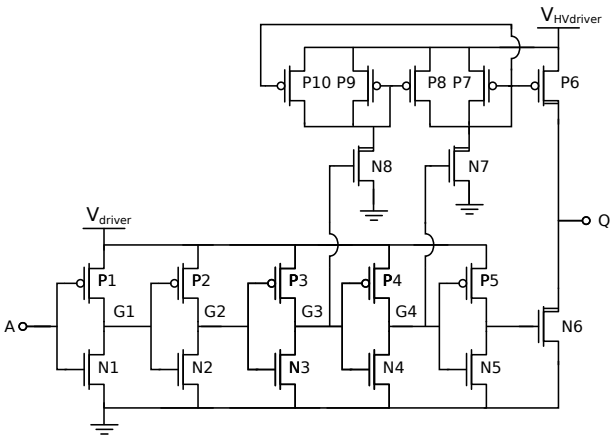

Figure 5.20: High-voltage driver for external power MOSFET

5.7.5 ASIC layout

A layout plot of the SHARC ASIC is shown in Figure 4.17. Chip dimensions are approximately $3.3 \times 3.5\ \mathrm{mm}^2$. In the high-side synchronous rectifier, a single MOSFET segment, with its associated driver and address decoder are highlighted. On the left-hand side, the segment controller, the comparator, and the bandgap voltage reference are highlighted. On the right-hand side, the driver for an optional external MOSFET is also highlighted. In the low-side synchronous rectifier, the segment addresses are indicated.

5.7.6 ASIC packaging and test-board

Although in mass production of integrated circuits it is often possible to perform wafer scale testing of the circuits before packaging, this is cost prohibitive for the small series size of IC prototypes in a research setting. In IC prototypes with standard low-voltage low-current analog and digital circuits, packaging is not always an absolute requirement, as it may be possible to test the functionality using probe-station or probe-card testing, although in many research settings the ease of handling of a packaged prototype IC is preferred, as not every lab is equipped with the required tools for this to be possible. In IC prototypes with significant power handling requirements on the other hand, probe-station or probe-card testing does not allow for verification of the full functionality, due to the parasitic resistance and capacitance introduced by probes and probe-cards. Therefore, IC prototypes for power conversion are always tested in their application, typically on a PCB (Printed Circuit Board), with the IC mounted in a chip package for ease of handling. However, the prototype packaging of a smart-power IC introduces some complications when compared to packaging of integrated circuits with either exclusively low-power analog and digital circuits, or integrated circuits with exclusively power devices.

IC package	Dissipation in package (Watt)
DIL 40	5.06
DIL 48	2.70
QFN 48	0.64
QFN 56	0.50
PGA 84	0.66
PGA 100	0.78
PGA 120	0.86
PGA 144	0.62

Table 5.4: Estimated dissipation in package and bondwires for a number of packages available through Europractice assuming a 3 A load current in the SHARC ASIC and excluding dissipation in the ASIC

All but the most simple of low-power analog or digital circuits typically require a relatively large number of I/Os (inputs/outputs) for full characterization during the prototyping phase, with a very limited current through each of these I/Os. A wide array of packages suitable for this purpose is available through the MPW prototyping services, with e.g. Europractice offering assembled packages with between 16 and 256 pin connections [17]. Pure power devices on the other hand normally only have a handful of I/Os, with significant current carrying requirements in most of these I/Os. These packages are not by default available through Europractice, and do not provide a sufficient number of I/Os for testing prototype smart-power ICs.

Therefore, prototype smart-power ICs are by necessity assembled in the standard low-power packages, with multiple package pins used in parallel for the high-current I/Os to minimize the series resistance of these I/Os to the outside world, while the low-power I/Os only use a single package pin. Because the series resistance per package pin tends to increase with the number of pins, and the optimal package is not simply the package with the most pins to connect in parallel for the high power connections, but a balance depending on the number of low-power and high-power I/Os, and the current through the devices. To facilitate the package selection during the design stage, a spreadsheet was used to approximate the power dissipation in the package depending on the current, number and length of bondwires, and number of low-power and high-power connections. To illustrate the importance of the package selection, Table 5.4 lists the estimated dissipation in the package interconnects and bondwires for the SHARC ASIC with a load current of 3 A while using 35 standard single pin connections and 3 high-current connections dividing the remainder of the available package pins. All high-current connections assume 2 parallel bondwires of maximum diameter per package pin. Packages with an insufficient number of I/Os for the prototype testing of SHARC were not included in the comparison, and the dissipation in the ASIC is excluded since this is a constant for all packages. The properties of the packages were acquired through Europractice. Based on this compari-

son, the QFN56 package was selected for the prototype packaging, and was ordered as such from Europractice. A microphotograph of the SHARC ASIC wire-bonded in this package is shown in Figure 5.21. As can be seen in the figure, a number of auxiliary bondwires are used on the chip as an additional metal layer for better distribution of the current over the power MOSFET devices.

The test-platform for the SHARC ASIC is shown in Figure 5.22. As mentioned in the design considerations for the ASIC, each ASIC only provides one leg of a full bridge secondary side rectifier to reduce prototyping cost, so 2 ASICs are required on the test-board for a complete rectifier. On the same test-board the ability to use a synchronous rectifier controlled by the primary is also foreseen to allow a comparison of the ASIC with discrete power devices controlled through an ISO7420 [31] digital isolator IC and an LM5110 [32] driver IC.

5.7.7 ASIC characterization

The ASIC design was fabricated in the ON Semiconductor I3T50 technology through an MPW run coordinated by Europractice [17]. Unfortunately, an unforeseen error in the digital segment controller block rendered the synchronous rectifier part of the ASIC non-testable, and no measurements on this implementation are available.

Although our lab had some previous experience with the synthesis and place-and-route of digital logic in older ON Semiconductor design kits, the process flow for using these tools with the current version of the design kit was undocumented and updates of the software tools and design kit build-up limited the re-usability of the in-house documentation of the older design kits. Due to a lack of familiarity with the possible verification options when data is transferred between different software tools, a human error went unnoticed, and the layout produced by the place-and-route tool for one of the digital sub-blocks did not correspond with the synthesized circuit, which was verified in both digital and mixed-mode simulations. A number of logic cells were missing in the generated layout, causing an undefined state on internal nodes which results in an oscillation on the outputs of the segment controller. Unfortunately, this issue was too complex to solve through FIB (Focused Ion Beam) manipulation, and only an expensive and time-consuming re-run would allow for further characterization. Because of time and budget constraints, this re-run was not possible and no further characterization of this implementation will be pursued.

Our internal documentation for the synthesis and place-and-route process has since been expanded and updated to include the use of several additional verification steps to avoid similar issues in future IC designs. Since then, the updated process flow has been used in other IC designs using the On Semiconductor I3T50 design kit, with successful demonstration in silicon of the digital circuit operation.

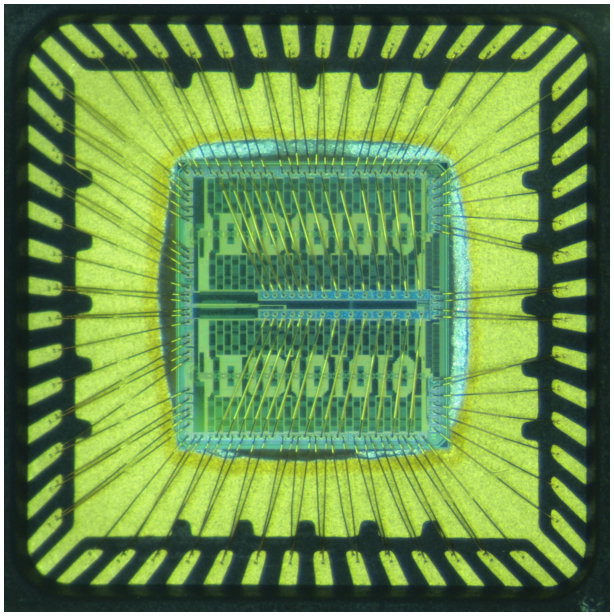

Figure 5.21: SHARC ASIC wirebonded in QFN56 package

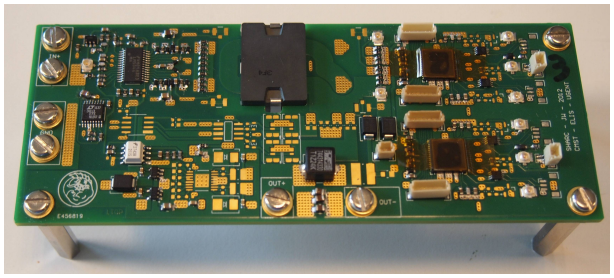

Figure 5.22: Test-platform for SHARC ASIC

5.8 Conclusions

In this chapter, we extended the optimization of the converter efficiency beyond the more basic approach in the previous chapters, where only the full load efficiency was considered. This is necessitated by the growing awareness of the wasted energy under low-load conditions. It is possible to influence the efficiency curve over the load range by a number of additions and modifications to the converter. Each of these approaches is discussed and evaluated for their potential use in a smart-power converter. Essentially, the switching loss, which is incurred at every switching cycle is the parameter to be reduced as much as possible under low-load conditions if the efficiency is to be optimized over the load range. Since the switching loss is mainly influenced by switching frequency, MOSFET gate drive voltage and MOSFET dimensions, these are the parameters that can be dynamically adjusted to optimize the low-load efficiency.

In telecommunications applications, where the quality of the signal is heavily influenced by the frequency components generated by the power supply, a dynamic adjustment of the frequency as in pulse skipping or burst mode operation is not desirable. A dynamic adjustment of the gate voltage only yields a limited potential for improvement, since a reduction in gate voltage is limited by the noise margin and the non-linear increase in conduction loss for gate drive voltages that are extremely reduced. A dynamic adjustment of the transistor dimensions does not suffer from these disadvantages, as the switching frequency and the noise margin remain constant over the load range, and the potential gain in efficiency mainly depends on the granularity of the segmentation. Due to the characteristics of IC integration, a dynamic adjustment of the transistor width lends itself especially well to implementation in smart-power converters. To improve on a downside of previous switching converter implementations of the MOSFET dimension adjustment, where it is assumed that a stream of information is available to predict the power consumption of the load, an estimation technique for the current through the device should be integrated. Several possible current estimation techniques are discussed, and based on their applicability in smart-power applications, an $R_{ds,on}$ current estimation technique is selected.

Initially, a proof-of-concept of the current estimation technique and implementation of the segmentation approach is shown in a discrete boost converter, which confirms the potential for efficiency enhancement over the load range. Despite the successful application of the technique, the gain in efficiency remains relatively low in discrete implementations, where the number of segments is limited by the overhead in cost and size for the packaging and assembly of large numbers of power devices.

In integrated converters, this disadvantage is no longer relevant, since the required silicon area to implement the necessary circuits is very limited when compared to the dimensions of drivers and power MOSFETs. Integration also allows for the use of significantly more segments than would be practical in any discrete converter, thereby further optimizing the efficiency under different load conditions.

The dynamic segmentation technique also allows for designing a hybrid form of discrete and integrated converters, where under low-load conditions only a number of segments of

the integrated MOSFETs is activated, and for load currents where integrated MOSFETs become too expensive, one or more external MOSFETs can be controlled using integrated drivers. Thereby cost and power efficiency can be balanced, as a single ASIC can be used for a variety of loads, while still allowing efficiency optimization over the load range. Finally a smart-power synchronous rectifier where these techniques to optimize the efficiency over the load range are implemented is discussed, both with and without external discrete power MOSFET devices.

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6 Conclusions and final remarks

6.1 Main achievements

In this work, we have presented a generic background for the efficient distribution of electrical energy, and have identified where smart-power technologies, which are high-voltage extensions of regular silicon CMOS technologies can be deployed to improve the performance of power conversion. Although it is possible to fully monolithically integrate efficient switching converters in semiconductor technologies without the need for any external components, the output power of these fully integrated converters is limited to a couple of Watt at best due to technological limitations of integrated components. The potential output power in converters where discrete inductors, capacitors, and power devices are used is several orders of magnitude larger, although these discrete converters use significantly more space and require much more engineering effort to implement in an application than their fully integrated counterparts. Since the performance of a converter is a delicate balance between size, cost, and efficiency, neither of these approaches is the ultimate solution for all possible converters. In this work, we investigated the use of relatively low-cost smart-power technologies for implementing a hybrid between these two types of converters, where most of the devices – including the semiconductor power devices – are monolithically integrated in the semiconductor technology, while still allowing for the use of external components when the performance or cost of integrated versions of these components becomes undesirable for the chosen output power.

Using this approach, these hybrid integrated converters can offer benefits in terms of size compared to converters using discrete devices, as a single integrated circuit can assume the function of a separate controller, one or more drivers, and one or more power devices,

while allowing for increased output power compared to fully integrated converters. Although these hybrid converters are already commercially available for a range of voltages and power levels, the effort in selecting optimal converter topologies for these converters appears to be extremely limited, and little to no use appears to be made of the potential advantage of the integrated character of these converters by providing additional functionality or optimizing the efficiency over the load range.

Through a theoretical estimation of the silicon area requirement for a given power dissipation in a number of potential topologies for these hybrid monolithic integrated converters, it was possible to formulate a cost function that allows for selecting the most appropriate topology without having to go through the entire design process for each set of design specifications in every possible topology. For converters where the ratio of input voltage to output voltage is relatively close to unity, the optimal converter topology in terms of silicon cost in affordable smart-power technologies is typically a non-isolated converter, such as a buck, buck-boost, or boost converter. For converters with a voltage conversion ratio relatively far from unity, transformer-isolated topologies allow for a more efficient smart-power integration, by using high-voltage devices at relatively low currents and low-voltage devices at relatively high currents. We have shown that within the limitations of affordable high-voltage technologies, the full bridge primary topology using a full bridge secondary side synchronous rectifier leads to an optimal efficiency for a given silicon area in transformer-isolated converters. Regardless of this optimization based on the ratio of input and output voltage, in some applications transformer isolation is part of the safety requirements for the equipment, and in those cases the full bridge primary topology using a full bridge secondary side synchronous rectifier is also the topology leading to minimum power dissipation for a given silicon area.

After this initial optimization, where a number of assumptions were made to allow for a comparison that is not needlessly over-complicated, the effects of the non-ideal behaviour of real-world components was discussed. It was shown that a major roadblock in the efficient monolithic integration of transformer-isolated converters is the voltage overshoot at the secondary side switching node or nodes for every transition, caused by the interaction of transformer leakage inductance and parasitic capacitance in the rectifiers. A number of possible solutions are discussed to limit or 'clamp' these voltage excursions. We have shown an actively controlled energy recovering voltage clamping circuit, where a significant portion of the energy from the voltage overshoot is transferred to the output of the converter. Under worst-case conditions, this clamping circuit can limit the voltage overshoot to arbitrary levels, while interfering as little as possible under other conditions, to optimize the converter efficiency under non-worst-case conditions. The operation of this clamping circuit was shown in both a discrete proof-of-concept, and in a smart-power ASIC implementation.

Finally, the efficiency of the converter for load currents that are less than the full load was also examined. Several approaches are possible to optimize the efficiency under these conditions, such as bypassing the converter with another linear or switching converter that is more efficient at light load, dynamic gate voltage adjustment, pulse skipping, or segmentation of the power devices. The segmentation approach was selected as the most

appropriate choice for hybrid integrated converters, as this can be realized without limitations on the possible loads and with minimal impact on the cost and size of the converter. We presented an automatic segment controller that can optimize the number of activated segments in function of the load current, without interrupting the current path or without a-priori information on the load current. The operating principle was shown in a discrete proof-of-concept, where the efficiency enhancement is measurable, but limited by the number of segments that can be feasibly implemented in a discrete converter because of the overhead in placing and independently driving multiple discrete power transistors. In hybrid integrated converters with integrated power transistors, the overhead of using multiple independent segments is reduced, and the number of segments can be significantly increased without incurring large penalties. Unfortunately due to a human error in the ASIC implementation, the efficiency optimization with this approach for hybrid integrated converters could only be shown in simulations. Because the segmentation approach is not necessarily limited to controlling MOSFET segments on the smart-power converter IC, it is also conceivable to extend the power handling capabilities of hybrid integrated converters by implementing one or more segments as drivers for external power devices. Although we then no longer have the large advantage in space saving when compared to converters that only use discrete switching devices, this approach still allows for a constant-frequency efficiency optimization, which is not possible in converters without integrated power devices.

6.2 Future work

On a finishing note, some potential areas for future work can also be highlighted. A potential area for improvement which we have omitted in this work is in the development of resonant-type hybrid integrated converters, where the switching losses that are incurred at every switching cycle can be significantly reduced when compared to the conventional hard-switched converter topologies that were the focus of our topology optimization. Although the voltage stress in resonant converters is relatively high, which as we have seen in the topology optimization leads to a sharp increase in conduction loss with power MOSFET devices in affordable smart-power technologies, the reduction in switching loss can enable the use of increased switching frequencies, which allows for a further shrinking of the transformers, inductors, and capacitors in the converter.

Another area for future work is extending the power handling capabilities of hybrid integrated converters by building converters that use both integrated power MOSFETs and external power devices. Since the economically feasible power handling capabilities of integrated MOSFET transistor switches in currently available affordable smart-power technologies is relatively limited when taking into account the required semiconductor area and associated cost, it could be interesting to further investigate the possibilities of converters that take advantage of the best of both worlds. In these proposed converters, the power transfer at low load could be handled using integrated MOSFET segments, with integrated drivers for one or more external power transistors to expand the capabilities at

high load. If the smart-power IC and discrete power devices are integrated in a multi-chip module, the parasitic elements in the interconnections can be reduced to improve the matching of driving circuits and power devices. From a system implementation viewpoint, where the advance in integrated circuits has always facilitated the speed and ease of implementation, a multi-chip module containing multiple smaller integrated circuits and power devices is not easily distinguishable from a single packaged integrated circuit.
By using discrete power devices in a multi-chip module which are typically more area efficient than integrated MOSFETs, a higher power handling density may be achieved. This also allows for a single ASIC to be used in combination with a range of power devices, depending on the application, although this reduces the potential gain in efficiency by having drivers that are fully matched to the power devices instead of using generic drivers.
A further high output power expansion possibility would be the use of high-performance wide bandgap external power devices, such as Gallium Nitride (GaN), Silicon Carbide (SiC), diamond etc. for which the theoretical power handling capabilities is an order of magnitude over what is possible with silicon. The development of these wide bandgap devices has been a hot topic since the performance of silicon power devices began to approach the theoretical limits. Although the production of these devices on a scale comparable to power MOSFET devices is still years away at best, the devices are gradually becoming more mature and affordable, and it is to be expected that switching converters will be one of the first applications to take advantage of the improved power handling of these exciting new devices.