Energy Consumption by Reversible Circuits in the 130 nm and 65 nm nodes

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ABSTRACT

As previous studies in the CMOS 350 nm technology node showed, adiabatic dual-line pass-transistor reversible CMOS circuits *may be of real interest, especially for human-machine interaction applications such as video, sound and all embedded functions where low-power, low-consumption are mandatory and where frequencies are not the main concern. But the question of viability, suitability and consumption of the quantum-inspired adiabatic reversible CMOS technology with the reduction of the feature size is often asked. With the reduction of transistor sizes, comes an increase of gate leakage that may have a negative impact both on the computation reliability and on the consumption. In another hand, size reduction may allow a gain in performance for an equivalent energy consumption. This paper gives a first evaluation on the consumption by the adiabatic reversible circuit in the 130 nm and 65 nm technology nodes. We show that both 130 nm and 65 nm technologies are suitable for reversible computation. Even better, compared to longer transistor nodes, both small sizes allow to reduce the energy consumption bellow 1 pJ per transistor and per cycle.*

Keywords: Reversible computation, adiabatic signal, energy, consumption, CMOS technology, 350 nm, 130 nm, 65 nm, threshold voltage, design, implementation, ripple-carry adder, quantum computing.

INTRODUCTION AND CONTEXT OF THE WORK

Reversible computing is useful for both lossless classical computing [1] and quantum computing [2].

Discrete linear transformations are important tools in information processing. These circuit are of particular interest for applications in the field of injective transforms where they are prime candidates for hardware implementation. These reversible circuits are able to perform both the forward (computation) transform and the inverse (uncomputation) transform simply by physically selecting the direction of calculation (direction of the data signal flow) [3].

These last years, we successfully designed, fabricated and tested several prototypes and proofs of concept of CMOS reversible (quantum-inspired) digital circuits[4] such as a 4 bits reversible ripple-carry adder based on Cuccaro's design [5–7], a reversible arithmetic logic unit (ALU) designed by Thomsen at *Al.* [8], or a 4 times 4 bits inputs to 6 bits outputs H.264/AVC encoder[9, 10].

We demonstrated in [3] that the CMOS reversible circuits, can easily be interfaced with and even driven by conventional restoring computation circuits. This may be of particular interest in embedded applications as for example for video coding and decoding where the two functions can be done using the same chip[9, 10]. Quantum-inspired reversible circuits are particularly suitable (but not only) for integer linear transforms [10], especially when "perfect determinants" are used when coding the function matrix, which allows the implementation of a linear transform without creation of garbage numbers [9] *(We call "Perfect determinants" coding matrix determinants of the form $\pm 2^k$ where k is an integer).*

Despite conventional restoring computing, which is based on logically-irreversible elementary operations leading to the destruction of many information during the computation steps and thus to an increase of entropy, reversible circuits focus on thermodynamically-reversible operations allowing to reach very low consumption in comparison [11–13]. Hardwares implementing *adiabatic dual-line pass-transistor reversible CMOS circuits* have already shown to be energetically economic. Simulations predict a drastic reduction of energy consumption close to 1/20 with about 95 % of energy recovered during the uncomputation phase [14]. This study was performed based on a 350 nm technology which is very little used today.

In order to obtain experimental data on the power consumption of CMOS reversible circuits, we recently designed and tested reversible full-adders using two smaller technology nodes: the UMC 130 nm and UMC 65 nm. For this study, the UMC 130 nm High speed (HS) and UMC 65 nm Low Leakage and Low Threshold Voltage (65-LL-LVT) technologies have been chosen.

A very frequent question is whether or not small technologies are suitable for reversible circuits. This is not obvious as with smaller technologies come larger gate leakage currents

leading to higher consumption and undesirable impact on the reliability. In another hand, smaller technology nodes should allow better performances in particular when considering the computing frequency range accessible.

This paper will propose some answers to these questions based on a first study of *adiabatic dual-line pass-transistor reversible CMOS circuits* in the 130 nm and 65 nm technology nodes.

FULL-ADDER CIRCUIT

The reversible full-adder used in this paper is the optimal version already presented in [14] (*Fig.5d*). Its Quantum diagram is presented Fig.1.
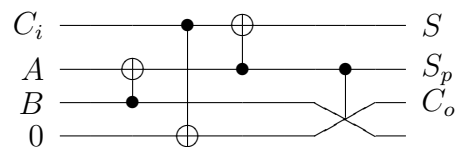

Figure 1. Quantum diagram of the studied reversible full-adder.

The reversible full-adder has three inputs A, B and C_i which is the carry-in bit. An extra line is used with zero at input to first copy the carry-in bit C_i and then compute the carry-out bit C_o. Output $S = A \oplus B \oplus C_i$ is the sum bit taking into account the carry-in (least significant bit of the sum), C_o is the carry-out (most significant bit of the sum) and S_p is the partial sum $A \oplus B$. The last output is a garbage.

The Cadence^{TM} core cell layouts for 65 nm and 130 nm are given in Fig.2 and Fig.3 respectively. Due to different design rules, the layout of the 65 nm full-adder is not merely a shrinking of the 130 nm one. Nevertheless, similar topologies are used in order to have as close as possible circuit layouts. A photo of the 130 nm reversible full-adder can be seen in Fig.4.

Size and composition of each circuit as well as minimal sizes of transistors and their threshold voltages are sumarized in Tab.1. Let us notice the large difference of threshold

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voltage (V_{th}) for the two technology nodes. For computation reliability purpose, we recommanded to use signals with amplitude about twice as large as the threshold voltage, if there are large parasitic signals. Nevertheless, in very protected environment, the signal amplitude can event be smaller than V_{th} [6, 15]. While for the 130 nm V_{th} is around 0.500 V, it is closer to 0.300 V for the 65 nm node. Therefore, the signal amplitude can be drastically reduced for the smaller node. For the 130 nm node, a signal amplitude of 1.000 V would be generally used while a signal amplitude of about 0.600 V would be used for the 65 nm's one. As in the present study the reliability of computation is not a concern, for purpose of comparison, a similar signal voltage of 500 mV has been used in both cases.

SIMPLE MEASUREMENT SETUP

Goals of the tests

In order to first evaluate the power consumption of our reversible circuits, several directions have been explored. The direct measurement of very small dynamic currents is challenging. While the most accurate apparatus on the market can only measure quasistatic currents due to long integration times mandatory for accurate measurement, transient measurement in a frequency range of few hundreds of Hertz up to few kilohertz is limited in accuracy to few microamperes except for very expensive systems.
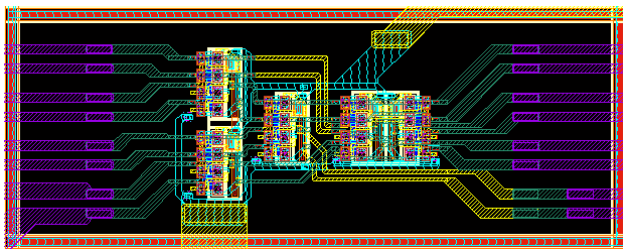

Figure 2. Layout of the CMOS 65 nm reversible full-adder.

We then choose to first evaluate the current consumption of our cell by indirect method. The aim of these measurements are twofold: first is to evaluate the current level flowing
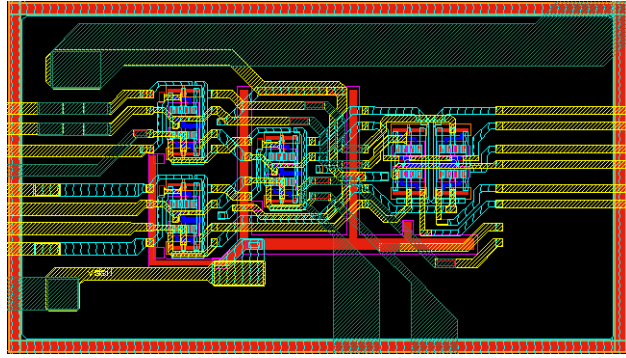
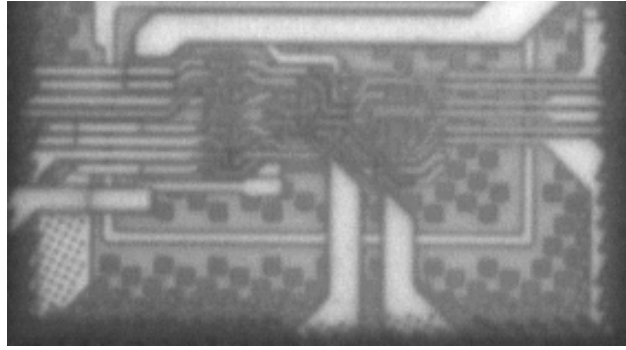Figure 3. Layout of the CMOS 130 nm reversible full-adder.

Figure 4. Photo of the processed CMOS 130 nm circuit. Dual lines are clearly visible.

through the circuit during the two phases of computation: the computation phase occuring during the raising amplitude of signals, and the uncomputation phase occuring when the signal amplitude decreases back to zero (Cf.[3, 6, 15] for details on the applied adiabatic signals). During the first phase, the circuit consumption is positive. The computation is done, the whole implemented function at once. During the second phase, the circuit will "uncompute" the calculation, bringing the energy stored in the circuit back to the source. This consumption is partly negative and has never been fully evaluated yet.

This study will be made on open output circuits. In other words, no output is connected to another device. The energy brought back to the source will then fully come from energy stored in the reversible circuit during the computation phase.

The second goal of this experiment is to see whether the reversible circuit can be modelised

Technology : 130 UMC HS

MinimalTransistor size : $\quad$ L = 120 nm $\quad$ $W_n = 160$ nm $V_{th_n} = 0.58$ V
$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad W_p = 480$ nm $V_{th_p} = $ -0.52 V

Technology : 65 UMC LL-LVT

MinimalTransistor size : $\quad$ L = 60 nm $\quad$ $W_n = 180$ nm $V_{th_n} = 0.28$ V
$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad W_p = 270$ nm $V_{th_p} = $ -0.29 V

Cell Name	130 nm Size X x Y (μm)	65 nm Size X x Y (μm)	Number of Transistors
Transmission Gate			1 + 1
Feynman Gate	5.08 x 5.31	3.080 x 3.780	4 x 2
Fredkin Gate	8.20 x 9.00	5.600 x 3.850	8 x 2
Reversible Full-Adder	22.80 x 11.98	14.500 x 8.100	**40** (3 Feynman + 1 Fredkin)

Table 1. Minimal sizes and threshold voltages of transistors used in the 130 nm and 65 nm full-adders and composition and sizes of sub-parts of the core cell.

by a very simple equivalent circuit regarding its consumption. This will simply be made by modeling the reversible circuit as a parallel RC circuit.

Measurements setup

Most of the time, in order to calculate very small input currents, a load resistor is used to measure the voltage drop between its terminals. This solution is efficient but requires first to know the load resistor value accurately – which can simply be done by measuring its value – and to be able to accurately measure the two load resistor terminal voltages. The difficulty starts when, as it is the case for reversible circuits, the impedance of the measured circuit is so large that the probe drains a non negligible current, which causes the load current to increase and the input voltage to drop. Even worse is the fact that the reversible circuit impedance is not constant. Moreover, as dual signals are used, the test has to be done for

both the logic "1" (positive voltage signals) and logic "0" (negative voltage signals). The total power consumption being the sum of the two contributions.

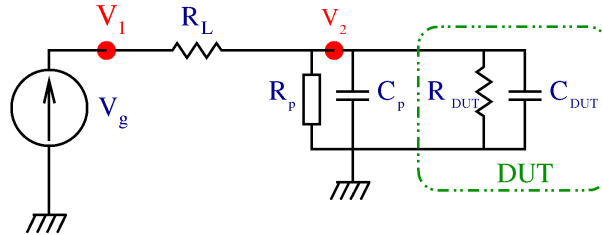A simplified schematic of the test bench is presented Fig.5.

Figure 5. Simplified schematic of the test circuit. The DUT reversible circuit is represented by a resistor and a capacitor in parallel which will be used for modeling.

The load resistor value R_L has been empirically determined to about 330 $k\Omega$ to be not too large in order to limit its influence on the input signal, but large enough to have a sufficient voltage differential to evaluate the load current. The measurement is performed using a DSO-X 2002A HP oscilloscope with two 10 $M\Omega$ and 15 pF probes. The load resistors have been accurately measured using a Fluke 175 multimeter in ohmmeter mode.

As the device under test (DUT) functions in open output mode, its impedance is supposed to be very high. In effect, having no device cascaded at output will imply the minimal input resistance to be of the order of gate resistance. Thus, the DUT resistance value should be the serial contributions of the interconnects, the channel of transistors and gate resistances. Some capacitive contributions should also provide from transistor parasitic capacitances, interconnects and transistor gates themselves.

As the transistor gate resistances are supposed to be higher than the probe impedance, the influence of the probe measuring the DUT input voltage, cannot be neglected in the calculation of the DUT input current. At the opposite, at the source side, the probe influence can be neglected as its impedance is directly in parallel with the source internal impedance $(R_g \simeq 50\ \Omega)$ which is very small in comparison.

In Fig.5, V_g designs the generator voltage setpoint. $V_g = 0.5\ V$ for both the 130 nm and

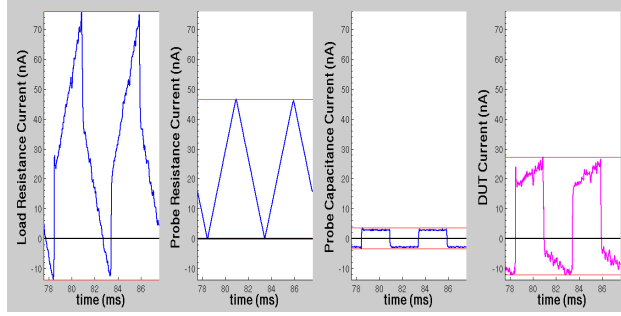Figure 6. **For 130 nm, f = 200 Hz**, from left to right:
measured load current i_{R_L}, calculated probe resistor current i_{R_p}, calculated probe capacitance current i_{C_p} and calculated DUT input current i_{DUT}.
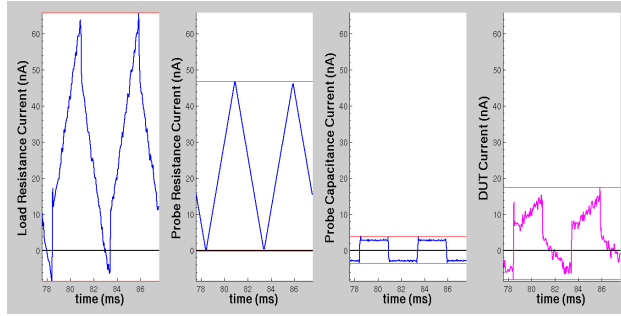

Figure 7. **For 65 nm, f = 200 Hz**, from left to right:
measured load current i_{R_L}, calculated probe resistor current i_{R_p}, calculated probe capacitance current i_{C_p} and calculated DUT input current i_{DUT}.

the 65 nm nodes. R_L is the load resistor empirically found to be best around 330 $k\Omega$, R_p and C_p are the probe resistance and capacitance respectively: $R_p = 10\ M\Omega$ and $C_p = 15\ pF$. The calculated equivalent resistance and capacitance used to modelise the reversible circuits are R_{DUT} and C_{DUT}. V_1 is the measured source voltage while V_2 is the measured DUT input voltage.

ENERGY CONSUMPTION EXTRACTION

The extraction algorithm has been developed in Matlab® and makes use of some classical implemented functions such as interpolation and smoothing, derivation or trapezoidal

integration we will not develop in this paper.

From the measured voltages V_1 and V_2, the load current i_{R_L} is first calculated. Then, the influence of the probe is removed. The probe resistive and capacitive currents i_{R_p} and i_{C_p} are both dependent on the DUT input voltage V_2. The probe capacitive current will also depend on the frequency f of the signals. We then have the obvious equations:

$$i_{DUT} = i_L - i_{R_p} - i_{C_p} \tag{1}$$

with

$$i_{R_L} = \frac{V_1 - V_2}{R_L} \tag{2}$$

$$i_{R_p} = \frac{V_2}{R_p} \tag{3}$$

$$i_{C_p} = C_p . \frac{\partial V_2}{\partial t} \tag{4}$$

As the derivative of V_2 will increase uncertainties due to the measurement noise, a pretreatment such as smoothing or averaging may be necessary, at least for the first evaluation of the value of C_{DUT}.

Two examples of the four currents i_{R_L}, i_{R_p}, i_{C_p} and i_{DUT} are given respectively in Fig.6 for the 130 nm and in Fig.7 for the 65 nm, both for a work frequency $f = 200\ Hz$. The two sets of curves are very similar. For both, the load current is around $i_{R_L} \sim 70\ nA$ but the final DUT input current is a lot smaller for the 65 nm node: $i_{DUT} \sim 30\ nA$ for the 130 nm and less than $20\ nA$ for the 65 nm node.

Let us underline the large probe influence. The probe resistor current contributes for both technologies to more than half the load current ($i_{R_p} \sim 45\ nA$). Even the probe capacitor current is not negligible as its amplitude corresponds to about a quarter of the input DUT current. Most interesting is to notice for both technology nodes, that a non negligible part of the DUT input current is negative, meaning that a part of the energy stored in the circuit during the computation phase is sent back to the source during the uncomputation one. Let

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us remind that the generator voltage V_g is always positive for logic "1" signals and always negative for logic "0" ones.

Knowing the DUT input voltage and input current, the instant power consumption can now be calculated:

$$P_{DUT} = V_2.i_{DUT} \quad . \tag{5}$$

Fig.8 and 9 present the instant power curves in linear scale for the 130 nm node and for logic "1" signals and 65 nm nodes on logic "0" signals, calculated for a work frequency $f = 200\ Hz$ and $f = 500\ Hz$ respectively.

The instant power curves plotted in linear scale reflect the triangular shape of the adiabatic signal. Nevertheless, the power curves are not symmetrical triangles. The slope of the signal during the uncomputation phase is drasticly increased as during this phase, the power consumption is reduced by the energy sent back to the source. This can be seen by comparison of the triangular signal drawn on Fig.8 and 9, representing an image of the source voltage (no scale). The negative energy contribution corresponds to the uncomputation phase. This restitution of stored energy ends at the begining of the next computation step, when the power consumption switches to positive again.

We can see in these two figures that a better restitution of the stored energy is given back for the 65 nm node. Even better, for the smaller node, the power curves for logic "0" and logic "1" are very similar while for the 130 nm node, logic "1" signals bring less energy back to the source than logic "0" which look like the case presented for 65 nm in Fig.9.

The maximum instant powers injected into and recovered from the reversible full-adder increase with frequency and technology size, as summarized in Tab.2.

The instant power peaks for 65 nm and 130 nm are very different, increasing in both cases with frequency. It seems nevertheless that for the lowest frequencies (few Hertz), the power peaks are larger than for few hundreds of Hertz and that no obvious rules allow to predict the obtained power peak values.

Better information is given by the calculation of involved energy by cycle of computation. The total energy dissipation and recovering is calculated by integrating the power over time
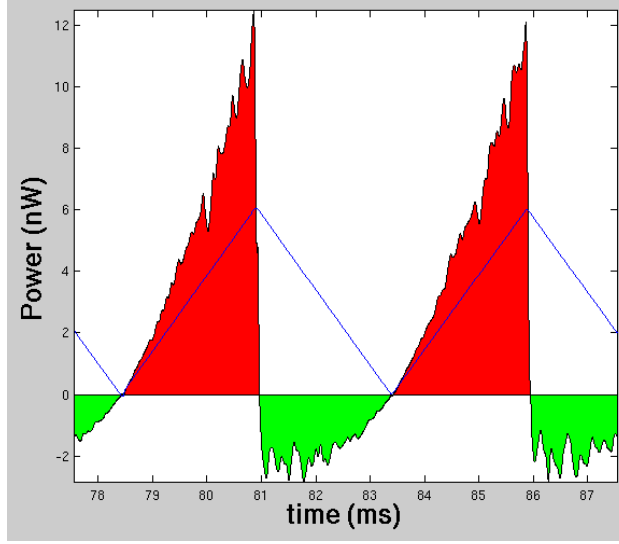
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Figure 8. 130 nm DUT Power consumption calculated for logic "1" signals and $f = 200\ Hz$. The filled areas represent the total energy injected in the circuit (positive) and recovered from it (negative). The triangular signal is an image of the source voltage V_g.

for one or several computation cycles:

$$E_{DUT_{Injected}} = \int_0^T P_{DUT_{Positive}} \cdot dt \qquad (6)$$

$$E_{DUT_{Recovered}} = \int_0^T P_{DUT_{Negative}} \cdot dt \qquad (7)$$

Tab.3 provides the total and partial variations of the DUT injected and recovered energy involved by cycle for the two technology nodes, for different frequencies and for the complementary adiabatic signals. As previously, the lowest energy consumption is found for the two technologies for a frequency close to 200 Hz. Surprisingly, for the 130 nm node, the recovering energies involved for logical "0" are found larger than the injected energies, which is not the case for the 65 nm node. This effect is not yet explained and may be related to parasitic couplings between dual lines. Nevertheless, both technology nodes provide better recovering energies for logical "0" than for logical "1". This may probably be related to the transistor type transmitting the signal. In effect, logical "0" signals are transmitted by n-Type transistors while logical "1" are transmitted by p-Type transistors. In order to
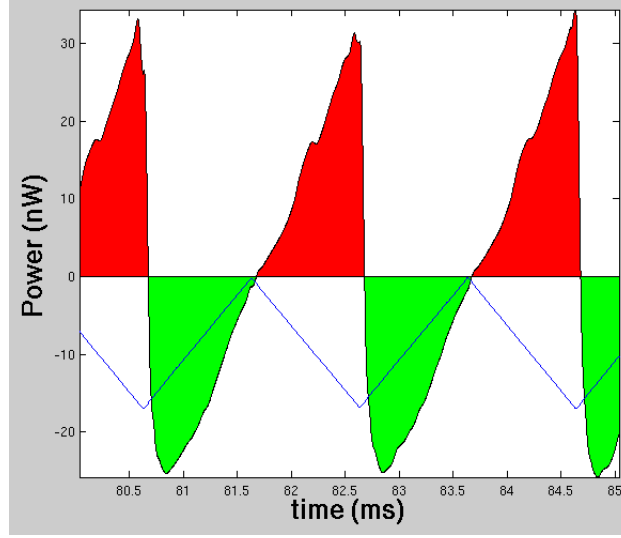
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Figure 9. 65 nm DUT Power consumption calculated for logic "0" signals and $f = 500\ Hz$. The filled areas represent the total energy injected in the circuit (positive) and recovered from it (negative). The triangular signal is an image of the source voltage V_g.

compensate the mobility difference of carriers in the transistors, p-Type transistors are wider than n-Type ones, enlarging also the parasitic capacitances.

In any case, when calculating the total energy injected and recovered, taking all the dual signals together, the injected energy is always larger than the recovered energy, as shown in the last part of Tab.3.

The total energy E_{total} consumed by the reversible full-adder, given a specific technology node and work frequency and its corresponding recovered energy ratio η are defined by:

$$
\begin{aligned}
E_{DUT_{total_f}} = \left(E_{DUT_{injected_f}} - E_{DUT_{recovered_f}} \right)_{"1"} \\
+ \left(E_{DUT_{injected_f}} - E_{DUT_{recovered_f}} \right)_{"0"}
\end{aligned}
\tag{8}
$$

and

$$
\eta = \frac{E_{DUT_{recovered_{f"0"}}} + E_{DUT_{recovered_{f"1"}}}}{E_{DUT_{injected_{f"0"}}} + E_{DUT_{injected_{f"1"}}}}
\tag{9}
$$

Tab.4 gives the total energy consumption by cycle and the recovered energy ratios of the

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Technology Node	Frequency (Hz)	Logic Signal	Injected Peak Power (nW)	Recovered Peak Power (nW)
65 nm	2	"1"	10	4
	200	"1"	8	1
	500	"1"	40	21
	2	"0"	5	4
	200	"0"	19	10
	500	"0"	34	26
130 nm	2	"1"	8.6	6.3
	200	"1"	12	3
	500	"1"	12	3
	2	"0"	6	6
	200	"0"	16	15
	500	"0"	51	3

Table 2. Variation of the DUT injected and recovered peak power for the two technology nodes, for different frequencies and for the complementary adiabatic signal.

reversible full-adder, for the two technology nodes and for the different frequencies.

For both technologies, the minimal energy consumption is found around 200 Hz.

Discussion

In order to allow comparison to other circuits and other technologies, we propose to use $pJ.gate^{-1}.cycle^{-1}$ as dimensional unit. We then need only this energy consumption value together with the frequency to have a good image of performances of the circuit. As our circuit is composed of four logic gates and as the energy consumption is already expressed in $pJ\,/\,cycle$, we then obtain 4 $pJ.gate^{-1}.cycle^{-1}$ and 2.5 $pJ.gate^{-1}.cycle^{-1}$ respectively for the 65 nm and 130 nm nodes. Let us remark that this corresponds in both cases to less than 1 $pJ.transistor^{-1}.cycle^{-1}$.

According to Tab.3 and Tab.4, very low frequencies such as 2 Hz drastically increase the energy consumption. This is quite obvious as for low frequencies, the capacitive effect in

Technology Node	Frequency (Hz)	Logic Signal	Max Injected Energy (pJ)	Max Recovered Energy (pJ)
65 nm	2	"0"	832	530
		"1"	1335	110
	200	"0"	33	31
		"1"	15	1
	500	"0"	45.2	37.9
		"1"	51	29
130 nm	2	"0"	221	974
		"1"	1900	55
	200	"0"	34	42
		"1"	26	8
	500	"0"	50.9	48.3
		"1"	26	8
65 nm	2	Σ	2167	640
	200	Σ	48	32
	500	Σ	96	67
130 nm	2	Σ	2121	1029
	200	Σ	60	50
	500	Σ	77	56

Table 3. Total and partial variation of the DUT injected and recovered energy involved by cycle for the two technology nodes, for different frequencies and for the complementary adiabatic signals.

the reversible CMOS circuit is almost inexistant, preventing much energy to be stored in the circuit. In effect, the small amount of energy stored is almost totally consumed in the resistive parts of the circuit. The reversible circuit can then be approximated by a pure resistive circuit. The longer the signal period, the larger the resistive energy dissipation. Very low frequencies are then not suitable for **CMOS** dual-line pass-transistor reversible technology. For high frequencies, the voltage slope being steeper, the capacitive effects are amplified, bringing more current into the circuit. This important current together with non reducible resistors (such as interconnects and channel of transistors) explains larger power

Technology Node	Frequency (Hz)	Total Energy (pJ)	Recovered Energy ratio (%)
	2	83	30
65 nm	200	16	70
	500	29	71
	2	1100	49
130 nm	200	10	83
	500	21	73

Table 4. Total DUT energy consumption by cycle and recovered energy ratio for the two technology nodes and for different frequencies.

peaks (and larger load current amplitude). The circuit will thus dissipate more energy with the current increase, reducing the recovering ratio η.

For the 130 nm node, a decrease of η is already visible at 500 Hz while for the 65 nm node, η is still stable around 70 % in the range of few hundreds of Hertz. This is less than the recovering ratio of 95 % predicted in [14], that was not taking into account in their simulations, the parasitics introduced by interconnect couplings.

As triangular pulses are composed of harmonic signals, we believe that consumption may also be reduced if using sine signals. For non sine signals, higher frequencies are filtered by the circuit and an extra amount of energy is dissipated even for low frequencies. Nevertheless, this energy loss has not been calculated yet, as precise circuit dependent $\eta(f)$ curves have to be first measured which is still work in progress.

The optimal frequency of 200 Hz indeed is low, but this is an **optimal** value. As said above, with our non-optimized circuit and measurement bench, excellent signal shapes can be conserved up to 44 kHz when measured with commercial probes on a simple bread board and even far above with minimal capacitive output charges and optimized printed board. Nevertheless, discussion is open on a definition of adiabaticity in real circuits.

Let us remind that the word adiabaticity comes from the Ancient Greek word "ἀδιάβατος" ("*adiabatos*") which means **impassible**. In physics and chemistry, a process is called adiabatic when occurring without exchange of heat (impassible) of the system with its environ-

ment. For the case of our reversible circuit, adiabatic computation is obtained when heat dissipation can be neglected. This occurs only when capacitive effects are maximized while resistive ones are minimized, such that heat dissipation is also minimized. For an electronic circuit to be adiabatic, the computation must be done in such a way that the signals are smooth enough for the circuit to consume the minimum energy (transformed into heat by the electronics) while performing a correct computation. We see in the present paper, that according to this definition, very low frequencies are less adiabatic (dissipate less heat) than higher frequencies of few hundreds of Hertz which are more adiabatic than higher frequencies. In the same idea, sine signals should be more adiabatic than the ones composed of linear segments, but a pure sine signal may be less adiabatic than one optimized pulse composed of sine segments taking into account the variation of circuit impedance as a function of the signal amplitude (as for example taking into account the transistor regime: sub or super-threshold regime).

As a final remark, let us say that if increasing the frequency range is always interesting in order to perform more computations by period of time, one may remark that circuit architecture may also bring computation power without the need to increase the signal frequencies. As an example, in the wonderfull and powerfull computer that is the human brain, wave frequencies only range from 4 Hz up to a maximum of about 100 Hz. In the future, circuits based on devices such as (but not exclusively) carbon nanotubes, may allow to merge both adiabaticity and reconfigurability[16] at the same time.

CONCLUSION

Saying that a technology node is better than another for the reversible circuit is not obvious. The 130 nm node globally allows lower power peaks than the 65 nm node which results also in slightly smaller total energy consumption with slightly better recovering ratios. However, the difference is small. This means that both technologies are suitable for reversible computing with optimum found in the frequency range of few hundreds of Hertz.

As expected, the 65 nm begins to be better if the application needs some frequency ranges above 500 Hz. In this case, one will have to take into account some other effects that may appear[6, 15]. Anyway, computation at frequencies far above 44 kHz is still possible if very small capacitive charges are placed at the output of the circuit.

The optimal frequency range will be probably drastically improved if an extra effort is done on reducing both capacitive parasitics and resistive interconnects. But will such functionning be still close to adiabaticity?

%section*Acknowledgment

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