5 x 20 Gb/s Heterogeneously Integrated III-V on Silicon Electro-absorption Modulator Array with Arrayed Waveguide Grating Multiplexer

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Abstract: We present a five-channel wavelength division multiplexed modulator module that heterogeneously integrates a 200GHz channel-spacing silicon arrayed-waveguide grating multiplexer and a 20Gbps electro -absorption modulator array, showing the potential for 100 Gbps transmission capacity on a 1.5x0.5 mm^2 footprint.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (250.7360) Waveguide modulators

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1. Introduction

Wavelength division multiplexing (WDM) modules are of key importance for realizing high aggregate bitrate optical networks and optical interconnects. WDM transmitters and receivers require low cost and high performance devices for maximal bandwidth usage and high energy-efficiency. For the key opto-electronic components in a WDM system, both silicon and III-V based devices are available. Potentially CMOS compatible, low-cost, monolithic silicon WDM modulator chips have been reported [1, 2]. However, an optically broadband silicon-based modulator usually has a large footprint and requires a relatively high driving voltage and hence high power consumption for sufficient extinction ratio [3]. Alternatively, purely III-V WDM modulator chips have been demonstrated [4, 5]. Although they are more efficient than silicon modulators, the monolithic integration with passive wavelength division multiplexing devices, e.g. arrayed waveguide gratings (AWG) and etched diffractive gratings (EDG) is not straightforward. In order to overcome these issues, a hybrid silicon platform that combines the advantages of III-V based materials and silicon is being studied. III-V/Si hybrid active devices with excellent performance, such as hybrid silicon narrow linewidth lasers [6], high-speed modulators [7], and high-speed detectors [8] have already been demonstrated. The highest speed modulators on silicon were achieved by transferring a III-V epitaxy stack onto a SOI wafer to realize a 67GHz bandwidth traveling-wave hybrid silicon electro-absorption modulator (EAM) [7]. These hybrid devices can be integrated together to build up more complex on-chip photonic modules [9, 10] on silicon-based substrates, which shows its potential for high density, high performance WDM transmitters and receivers for optical communication networks and multi-CPU optical interconnects in the future.

In this paper, a silicon AWG and an array of five III-V EAMs are heterogeneously integrated using adhesive bonding technology [11]. The (lumped) III-V EAMs show 17GHz E/O bandwidth and can operate up to 28Gb/s. A five-channel wavelength division multiplexed modulator module with an ultracompact size (1.5x0.5 mm^2), a low driving voltage (~2.5Vpp), and a large extinction ratio (4.9-6.9dB) is obtained with 100Gbps capacity.

2. Design

Figure 1 shows the schematic of the chip layout. On each channel of the AWG, a separate EAM is integrated. The AWG is formed by 220nm height silicon waveguides and it has five channels with 200GHz channel spacing. The III-V layer stack used for the EAM is shown in Table 1. The InAlGaAs multiple-quantum-well (MQW) stack is sandwiched between two separate confinement heterostructure layers (SCHs). It's composed of 10 compressively strained wells and 11 tensile strained barriers and has its photoluminescence (PL) peak at 1480 nm. Compared with InGaAsP MQWs, the InAlGaAs MQWs gives a stronger quantum confined stark effect (QCSE) and hence a better modulation efficiency, due to its larger conduction band offset [12]. The layer stack is designed for transverse electric (TE) polarization [13] in the C-band, compatible with conventional semiconductor diode lasers. The superlattice layer structure is incorporated to prevent the propagation of dislocations into the active region due to the bonding.

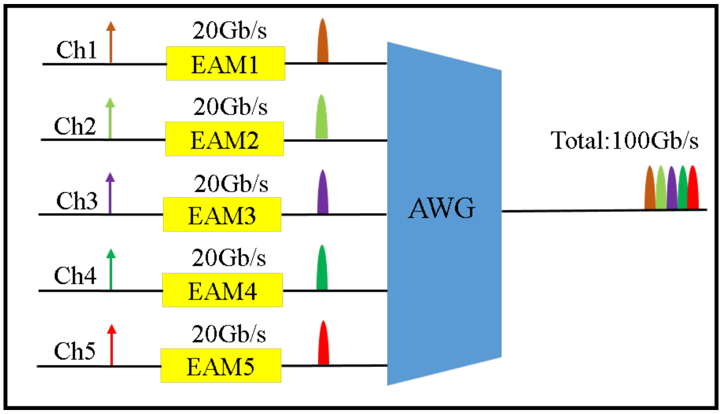


Fig. 1. The schematic diagram of the chip layout.

Layer	Composition	Thickness(nm)
P contact	$In_{0.53}Ga_{0.47}As$	100
Cladding	InP	1500
SCH	$In_{0.52}Al_{0.16}Ga_{0.32}As$	150
MQW	$In_{0.47}Al_{0.2}Ga_{0.33}As$ (11X)	7
(λ_{PL}～1.48μm)	$In_{0.59}Al_{0.08}Ga_{0.33}As$ (10X)	11
SCH	$In_{0.52}Al_{0.16}Ga_{0.32}As$	100
N contact	InP	110
Super lattice	$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$ (2X)	7.5
	InP (2X)	7.5
Bonding layer	InP	10

Table 1. Detailed III-V epitaxy stack

Figure 2 (a) and (b) are the cross-sectional view and top view of the EAM, respectively. The length of the active modulator section is 100μm and it is 2μm wide. Benzocyclobutene (DVS-BCB) is used for passivation and for decreasing the parasitic capacitance. A lumped electrode structure is adopted, which means the RC time constant limits the high speed performance of the EAM. The passive silicon waveguide underneath is a rib waveguide with 1.5μm width and is 220 nm shallowly etched into the 380 nm silicon layer. The optical coupling between the silicon device layer and the III-V epitaxial stack is realized using a bi-level taper consisting of two linearly tapered sections in the III-V structure. In the first taper section, the optical mode is converted from the silicon waveguide to the MQW (including SCH layers) waveguide without the thick p-cladding layer. Then, the second taper section adiabatically transforms the waveguide mode to that of the full III-V structure. We analyze the performance of the tapers for different values of L_{t1}, L_{t2} and the BCB bonding layer thickness h_{BCB}, using a commercial software FimmWave [14]. Fig. 3(a) and 3(b) show the coupling efficiency as a function of the lengths L_{t1}, L_{t2}, when h_{BCB} varies. Here we assume W_{tip1}=W_{tip2}=0.2μm, and while one taper is investigated, the other taper is set to be long enough for adiabatic conversion. From the figures we can find that the smaller h_{BCB}, the better the coupling efficiency and the shorter the taper length. However, thinner BCB bonding layers reduce the yield of the bonding process and hence a trade-off needs to be made is selecting the bonding layer thickness.

In our design, we assume L_{t1}=30μm, L_{t2}=15μm and h_{BCB}=0.03μm. The mode transformation under this condition is presented in Fig. 3(c). The coupling efficiency from the passive silicon waveguide to the III-V waveguide using this 45μm long taper can be more than 95%.

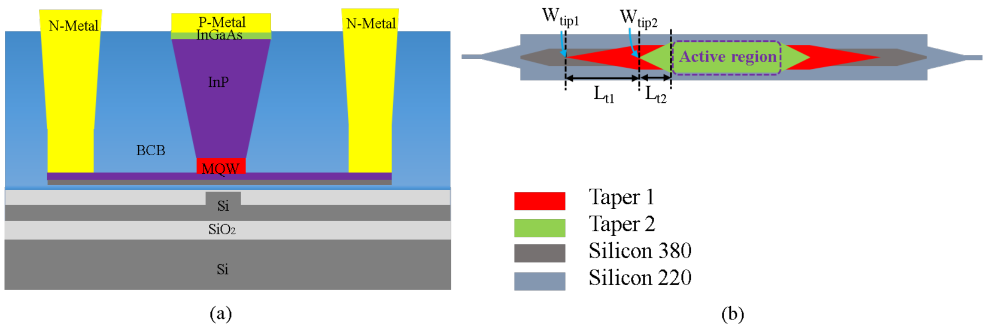


Fig. 2. (a) Schematic cross-sectional view; (b) top-view of the structure.

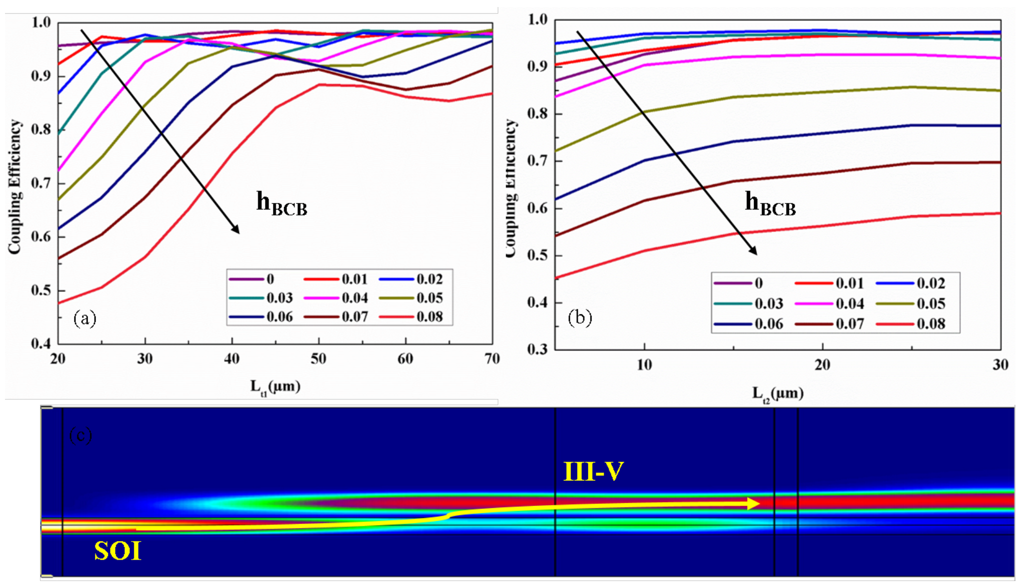


Fig. 3. (a) The coupling efficiency as L_{t1} varies for different thicknesses of the BCB layer (from 0 to 0.08µm) when L_{t2}=20µm; (b) The coupling efficiency as L_{t2} varies for different thicknesses of the BCB layer (from 0 to 0.08µm) when L_{t2}=30µm; (c) Mode transformation in the bi-sectional tapered coupler with L_{t1}=30µm, L_{t2}=15µm, h_{BCB}=0.03µm.

3. Fabrication

Figure 4 shows a schematic diagram of the fabrication process. The silicon photonic components are defined on 200mm silicon-on-insulator (SOI) wafers with a 380 nm thick silicon layer using 193nm deep UV lithography. The rib silicon waveguides are etched 160 nm deep using inductively-coupled-plasma (ICP) dry etching. The silicon waveguide circuits are then planarized through SiO_2 PECVD deposition followed by chemical mechanical polishing down to the silicon device layer. The III-V layer stack is adhesively bonded to this silicon waveguide using a 30nm thick DVS-BCB layer. HCl is then used to remove the InP substrate.

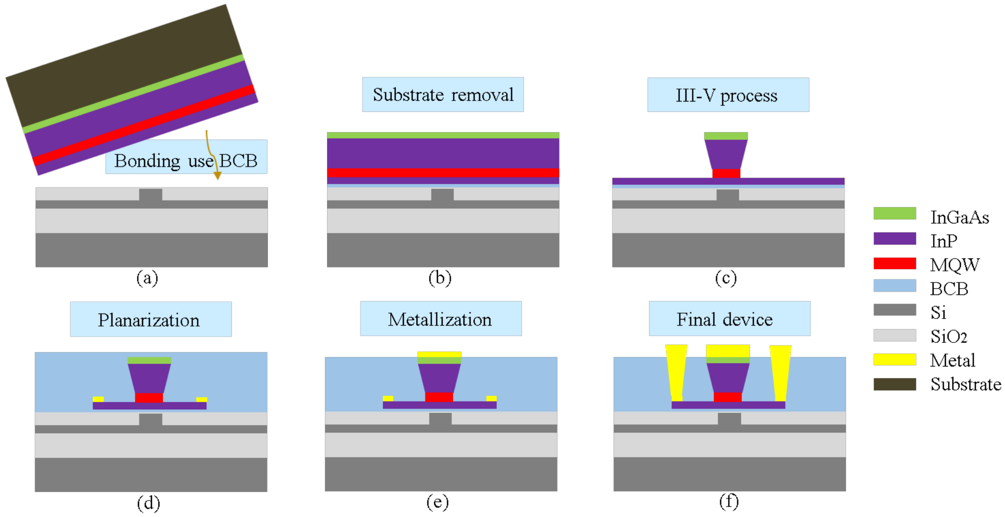


Fig. 4. Schematic diagram of the fabrication process (a) BCB bonding; (b) Substrate removal; (c) III-V process;(d) Planarization;(e) Metallization;(f) Final device.

The p-InP mesa with a width of 3.5 µm is defined by using the top p-metal (Ti/Au) as a hard mask. The 100nm InGaAs layer and 1.5µm InP p-doped layer are etched using selective wet chemical etching with $1H_3PO_4$: $1H_2O_2$: $20H_2O$ and 1HCl:$1H_2O$, respectively. The width of the p-InP at the bottom is reduced to 2µm as the orientation of the EAM mesa with respect to the InP crystal planes introduces an inverted trapezoidal mesa. Afterwards, a 5µm wide SiN mask is defined using UV lithography. 20CitricAcid: $1H_2O_2$ is used for wet etching of the MQW layer and the MQW is underetched to 2µm in width. The widths of the tips (W_{tip1}=W_{tip2}=0.2µm) are quite critical for a good coupling. In this work, such narrow taper tips are defined using UV lithography and carefully controlled by wet chemical etching, which demonstrates the manufacturability of these components in standard III-V processing lines. When the III-V mesa is defined, the n-type layer is etched using HCl. Then Ni/Ge/Au is deposited for the n-contacts. In the next step, the III-V structure is encapsulated with DVS-BCB for passivation to decrease parasitic capacitance. Reactive ion etching (RIE) is used to etch through the DVS-BCB layer to open the n-contacts and the p-contacts. Finally, ground-signal-ground (GSG) metal contact pads with 100µm pitch are formed for the RF ports. The SEM pictures of the top view and cross section of the EAM are shown in Fig. 5 (a) and (b), respectively. The inset of Figure 5(a) shows the narrow taper tip.

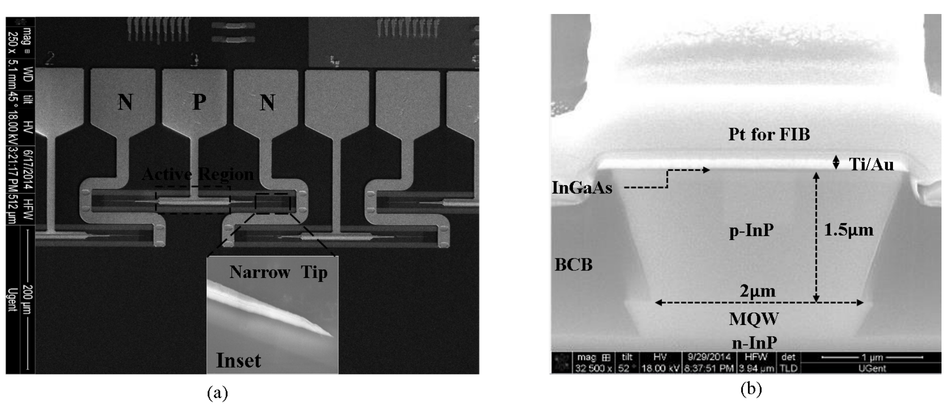


Fig. 5. (a) SEM picture of the top-view of a III-V on silicon EAM, the inset shows the narrow taper tips; (b) SEM picture of the cross section.

4. Experimental results

The normalized transmission spectra of the 5-channel multiplexer before and after the heterogeneous integration of EAMs are shown in Fig. 6. The channel spacing of the AWG is 1.6nm and the device has an insertion loss less than 3dB. However, after EAM integration the insertion loss varies from between -9.3dB to -3.4dB (measured after passing through the EAMs), which is attributed to non-uniform insertion losses of the fabricated EAMs. The minimum insertion loss of the EAM at 0V bias is measured to be 1.2dB. Fig. 7 illustrates the measured static extinction ratio of the 100µm-long EAMs under different reverse biases. More than 12 dB extinction ratio can be achieved when the bias is changed from 0 V to -2.5 V.

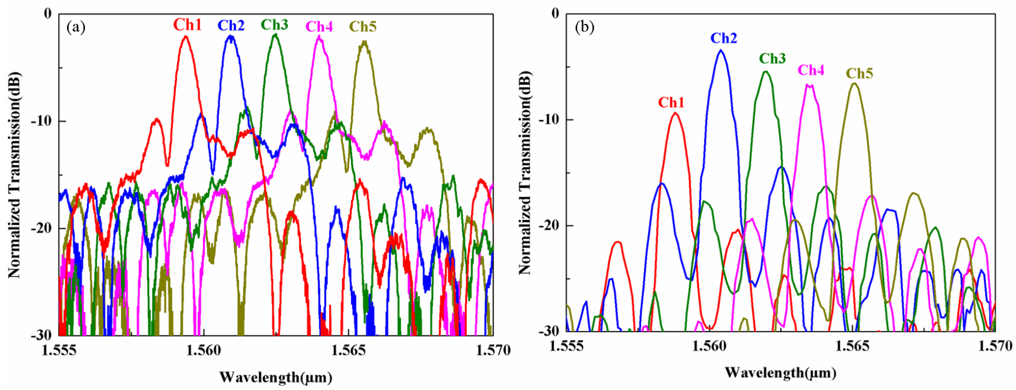


Fig. 6. Optical spectra of the AWG before (a) and after (b) the heterogeneous integration (including the EAMs).

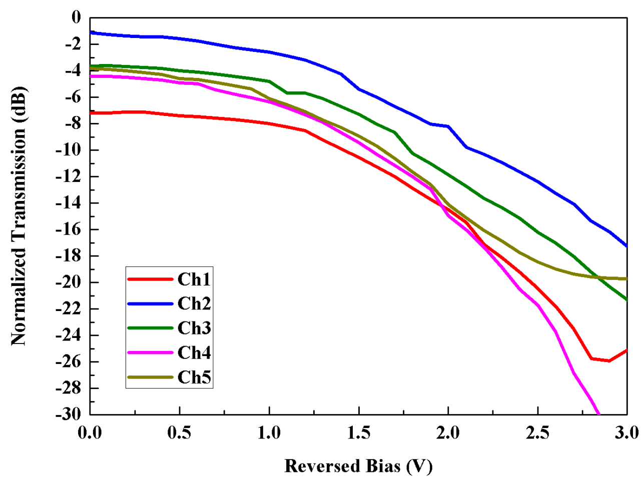


Fig. 7. Bias dependent normalized transmission of each channel.

The small-signal modulation of the hybrid EAMs was measured using a vector network analyzer. Fig. 8 shows the typical electro/optical (E/O) modulation response and the microwave reflection (S_{11}) to the RF source for an EAM under a reverse bias of -2V. The measurement indicates the E/O 3dB bandwidth is 17GHz. The red lines in the figures are the fitting results of the measured data according to an equivalent electrical circuit model [15] of the modulator (see the inset of Fig.8 (b)). In the circuit diagram, Z_s is 50Ω impedance, L_m is the inductance, R_a is the device resistance, C_a is the junction capacitance, R_j is the device junction leakage resistance and C_e is the parasitic capacitance between the electrodes. Besides, we also consider the resistance and capacitance between the electrodes and the Si substrate

R_{sub} and C_{sub}. The junction capacitance C_a is fitted to be 0.145pF. As the electrodes of the modulators are lumped electrodes, it suffers from strong microwave reflection.

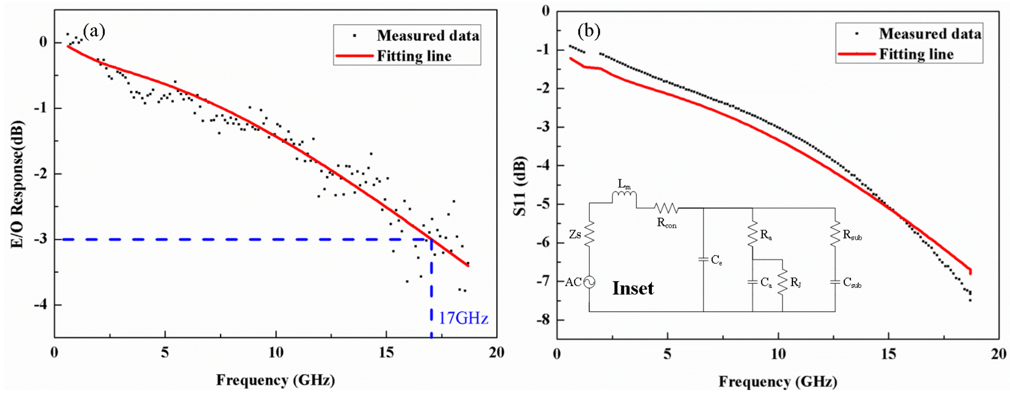
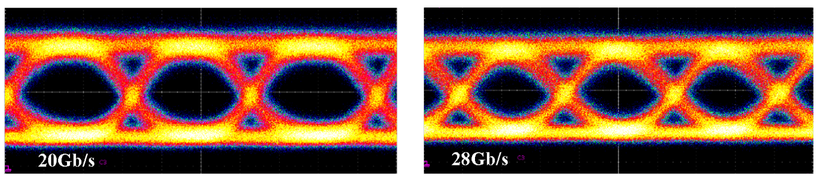


Fig. 8. (a) Small signal E/O response and (b) the microwave reflection to the RF source (S_{11}) for the hybrid EAM of channel 2, the inset of (b) shows the equivalent circuit.



(a) (b)

Fig. 9. Eye diagram of channel 2 at (a) 20Gb/s; (b) 28Gb/s.

For the large signal modulation measurements, a tunable continuous wave (CW) laser was aligned to each channel of the AWG. A Tektronix pattern generator followed by a driving amplifier and a bias tee produces a PRBS signal with 2.3 to 2.6Vpp with a DC offset of -1.5V to -2V to drive the EAMs. The modulated light was boosted by an erbium-doped fiber amplifier (EDFA). A narrow optical filter is inserted to remove the amplified spontaneous emission (ASE) noise generated by the EDFA. Finally, eye diagrams are obtained with a Tektronix 8300A digital series analyzer. The 20Gb/s and 28Gb/s eye diagram of the EAM on channel 2 are displayed in Figure 9(a) and (b), respectively. Fig. 10 shows the eye diagrams at 20Gbps for the five different channels. The dynamic extinction ratios vary between 4.9dB and 6.9dB.

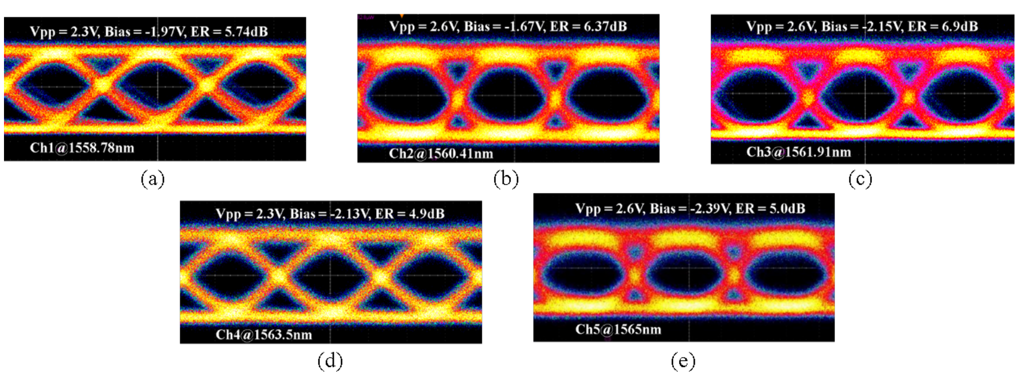


Fig.10. Optical eye diagrams at 20 Gb/s for each channel.

5. Conclusion

We report a five-channel WDM modulator module that heterogeneously integrates a 200GHz channel-spacing arrayed waveguide grating multiplexer and a 20Gbps electro-absorption modulator array reaching 100Gbps capacity. The total size of the device is 1.5x0.5 mm^2. The bandwidth of each modulator is around 17GHz. The realization of the module on a hybrid silicon photonic platform allows in a next step to co-integrate the laser sources as well. It can also be used as WDM receiver by strongly reverse biasing the EAM devices.

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