

Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters

Andreas De Groote^{1,2,*}, Paolo Cardile³, Ananth Z. Subramanian^{1,2},
Alin M. Fecioru⁴, Christopher Bower⁵, Danae Delbeke^{1,2},
Roel Baets^{1,2}, Günther Roelkens^{1,2}

¹Photonics Research Group, Department of Information Technology, Ghent University - imec, Ghent, Belgium

²Center for Nano- and Biophotonics (NB-Photonics), Ghent University, Ghent, Belgium

³Center for Microsystems Technology, Ghent University - IMEC, Ghent, Belgium

⁴X-Celeprint Limited, Cork, Ireland

⁵X-Celeprint Inc., Research Triangle Park, NC, USA

*andreasdegroote@intec.ugent.be

Abstract: We present the first III-V opto-electronic components transfer printed on and coupled to a silicon photonic integrated circuit. Thin InP-based membranes are transferred to an SOI waveguide circuit, after which a single-spatial-mode broadband light source is fabricated. The process flow to create transfer print-ready coupons is discussed. Aqueous FeCl₃ at 5°C was found to be the best release agent in combination with the photoresist anchoring structures that were used. A thin DVS-BCB layer provides a strong bond, accommodating the post-processing of the membranes. The resulting optically pumped LED has a 3 dB bandwidth of 130 nm, comparable to devices realized using a traditional die-to-wafer bonding method.

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1. Introduction

Though originally conceived for telecom and datacom applications, silicon photonics is now also emerging as a platform for the integration of optical sensors. Relying on CMOS fabrication technology, such a platform offers an opportunity for low-cost, mass-manufactured, miniaturized, monolithic optical sensor systems. The wide transparency range of silicon-on-insulator waveguides (1.2-4 μm) allows for chip-scale integration of sensing systems based on vibrational spectroscopy [1], provided an integrated light source and integrated photodetectors are available. To overcome the indirect band gap of silicon several approaches have been developed for the integration of the light source on a silicon photonic integrated circuit. One option is to use an external light source coupled to the chip, but this approach complicates the packaging and increases cost and size of the final solution. Heterogeneous integration of III-V semiconductors through a bonding technique on the other hand is a scalable approach, in which case the alignment is lithographically determined on wafer scale, reducing the cost for light source integration. Classical heterogeneous integration approaches rely on die-to-wafer or wafer-to-wafer bonding for the integration of the III-V material [2]. In many cases however, such an approach is not efficient in terms of usage of III-V material, especially when only a small fraction of the total silicon chip area requires III-V material. Moreover, integrating different III-V layer stacks is problematic because of the minimal size needed for the bonded dies. In 2004 Menard et al. [3] proposed a novel technique, transfer printing, where thin film components could be transferred from a source substrate to a target substrate, providing a scalable approach for device integration making efficient use of the source material. Several devices were successfully fabricated using this approach, such as a stacked nano-membrane laser on silicon [4] and light emitting diodes on diamond and glass [5]. Next to this, also Fabry-Pérot lasers have been transfer printed to silicon substrates [6]. This technique can be an enabling technology for the cost-effective integration of III-V semiconductor materials or devices on silicon photonic integrated circuits, as one only provides III-V where it is needed, irrespective of the required density of active devices.

In this paper we demonstrate the first III-V opto-electronic components transfer printed on and coupled to a silicon-on-insulator waveguide circuit. Thin membranes of InP-based material are transfer-printed to an SOI optical circuit, after which an optically-pumped, single-spatial-mode broadband light emitter is realized in the transferred membrane. The LED is pumped by a 1310 nm laser through the underlying single mode silicon waveguide coupling to the III-V membrane. The generated spontaneous emission is captured and coupled to the same SOI waveguide, achieving a 3 dB bandwidth of 130 nm, enabling its integration with on-chip high-resolution, small footprint spectrometers. The paper is organized as follows. We first discuss the technology to realize transfer-print ready InP-based membrane components, the III-V transfer printing process and the process flow to realize suitable devices. Next, the design of the optically pumped LED is discussed and experimental results are presented.

2. Transfer printing

In transfer printing, a thin-film material stack or device (hereafter referred to as a coupon) is transferred from a source substrate to a target substrate. The coupons are prepared such that they can be picked by a soft elastomeric PDMS stamp. As described in [7] the adhesion of the elastomeric stamp depends on the velocity of the stamp. The coupon can be picked up from the native substrate by moving up the stamp rapidly (thus exerting a force greater than the adhesion to the native substrate), and printed to an SOI chip by releasing the stamp slowly. While showing similarities with a pick-and-place technique, the main advantage of the transfer printing approach is that coupons can be transfer printed in a massively parallel way, by picking up and putting down large arrays of coupons at the same time. This allows for a high-throughput integration process. The use of a patterned stamp, which only makes contact to source and target substrate in selected positions, also allows for so-called area magnification, where the pitch of the coupons on the source substrate can be made much more dense than the pitch required on the target wafer. This area magnification allows for the efficient usage of the III-V source material. This concept is illustrated in Fig. 1, where coupons processed on a 2 inch InP wafer are transfer printed to a 200 mm or 300 mm SOI target wafer, 4 at a time. The next target dies could be done similarly, shifting the stamp by the coupon pitch when picking up and by the corresponding pitch on the target wafer when printing. The patterned stamp that is used in this case is also shown. For clarity the size of the III-V coupons was exaggerated, in reality many SOI wafers can be populated using the thousands of coupons that can be fabricated on a single 2 inch III-V wafer. Also, much larger arrays of III-V coupons can be simultaneously transferred. The technique is also not limited to the use of a single source material. Coupons from different source wafers can be co-integrated in an intimate way on a silicon photonic integrated circuit,

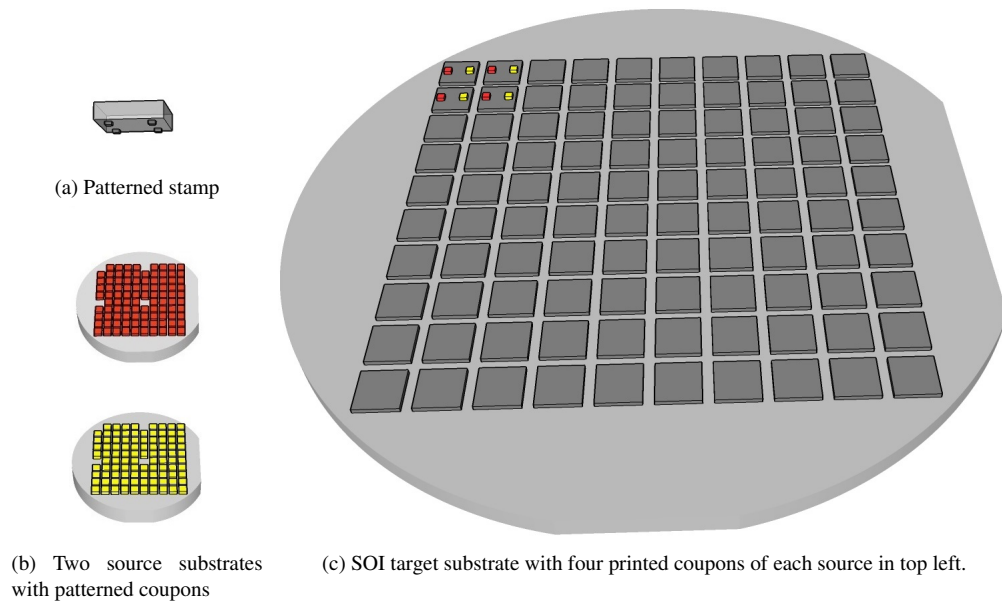


Fig. 1: Illustration of area magnification in transfer printing III-V coupons from the III-V source substrate to the SOI target substrate. The coupons from the first source wafer are indicated in red. The coupons from the second source wafer are illustrated in yellow. The patterned stamp used for this purpose is also schematically shown.

given the small size of the individual coupon (tens to hundreds of microns). This is difficult to realize using classical die-to-wafer bonding processes, where typically millimeter-sized III-V dies are being bonded [8]. Similar to die-to-wafer bonding the III-V opto-electronic devices are fabricated after transfer on wafer-scale, making the alignment of the coupons to the underlying SOI waveguide circuits non-critical. Nevertheless, using the proper markers, an alignment accuracy of $\pm 1.5\mu\text{m}$ 3σ can be obtained [9].

3. Transfer printing process flow

In this paper, InP-based membranes are transfer printed onto a processed SOI chip. The III-V membrane consists of two 60nm thick InP layers, with an InGaAsP multi-quantum-well layer stack in between, resulting in a total membrane thickness of only 200 nm. As a target substrate, planarized SOI waveguide circuits are used. A 50 nm thick DVS-BCB layer is spin-coated on the SOI target wafer serving as the bonding agent for the transfer printed coupons. The transfer printing process flow is described in Fig. 2. On the InP wafer, the membrane layer stack is grown on top of a $1\mu\text{m}$ thick InGaAs sacrificial layer. In order to make the coupon mechanically more robust and prevent buckling of the membrane when on the stamp, an InGaAs(100 nm) / InP($1\mu\text{m}$) sacrificial layer pair is grown on top of the membrane LED stack, which will be removed after transfer printing. Dense arrays of III-V coupons are defined by using a double mesa etch in the III-V device layer as shown in Fig. 2b. Next, anchoring locations for the coupon are defined by etching through the InGaAs release layer into the substrate. Finally, a photoresist coating was applied and patterned to protect all epitaxial layers above the sacrificial InGaAs layer, while at the same time anchoring the coupon to the substrate. A top view of single coupon after this step is shown in Fig. 2d. Aqueous FeCl_3 was used to undercut the $40\mu\text{m}$ wide coupons. At this moment the coupons are ready for transfer printing. The coupons are picked from the InP substrate by retracting a patterned PDMS stamp rapidly, after which they are transferred to the DVS-BCB coated SOI target wafer by attaching the coupons and releasing the stamp slowly. After removing the photoresist encapsulation using an oxygen plasma and the InP-InGaAs sacrificial layer pair by wet etching, the membrane is ready for further processing, lithographically aligned to the underlying SOI waveguide circuit. The process should render a sufficiently strong bond to withstand strong acids and make sure that the III-V waveguide is close enough to the silicon waveguide in order to allow optical coupling through tapers.

An important issue in the release of InP-based coupons is to find an etchant that can undercut the sacrificial InGaAs layer with enough selectivity to a thin InP bottom layer on the coupon (60 nm thin in this case). Several chemicals were tested, which are summarized in Table 1. The coupons were oriented with the $40\mu\text{m}$ short side along the (110) crystal axis.

The first three options failed to undercut the complete structure of $40\mu\text{m}$ wide. This is because of anisotropic etching, where a slow etching crystal plane is being exposed when the coupons are aligned along the crystal axes. The HF-based and citric-acid-based etch mixtures rendered a full undercut, but attacked the photoresist based anchors and encapsulation layer. While this could be resolved by using other encapsulation layers, because of the poor selectivity and slow etching speed respectively, these etching solutions were discarded as well. Figure 3 shows the height variation along the coupon - due to the limited etching selectivity - when undercut with the tartaric acid based solution or with the room temperature / 5°C FeCl_3 solution. One can see that for $40\mu\text{m}$ wide devices the height variation ranges from 60 nm to 20 nm, based on the selected etchant. Based on this, the cold FeCl_3 was identified as the best solution. Using this etchant it takes 2 hours to undercut the $40\mu\text{m}$ wide coupons.

After identifying the release etchant coupons were transferred to planarized SOI waveguide circuits. Microscope images of the source wafer after coupon definition, a coupon on a post of a

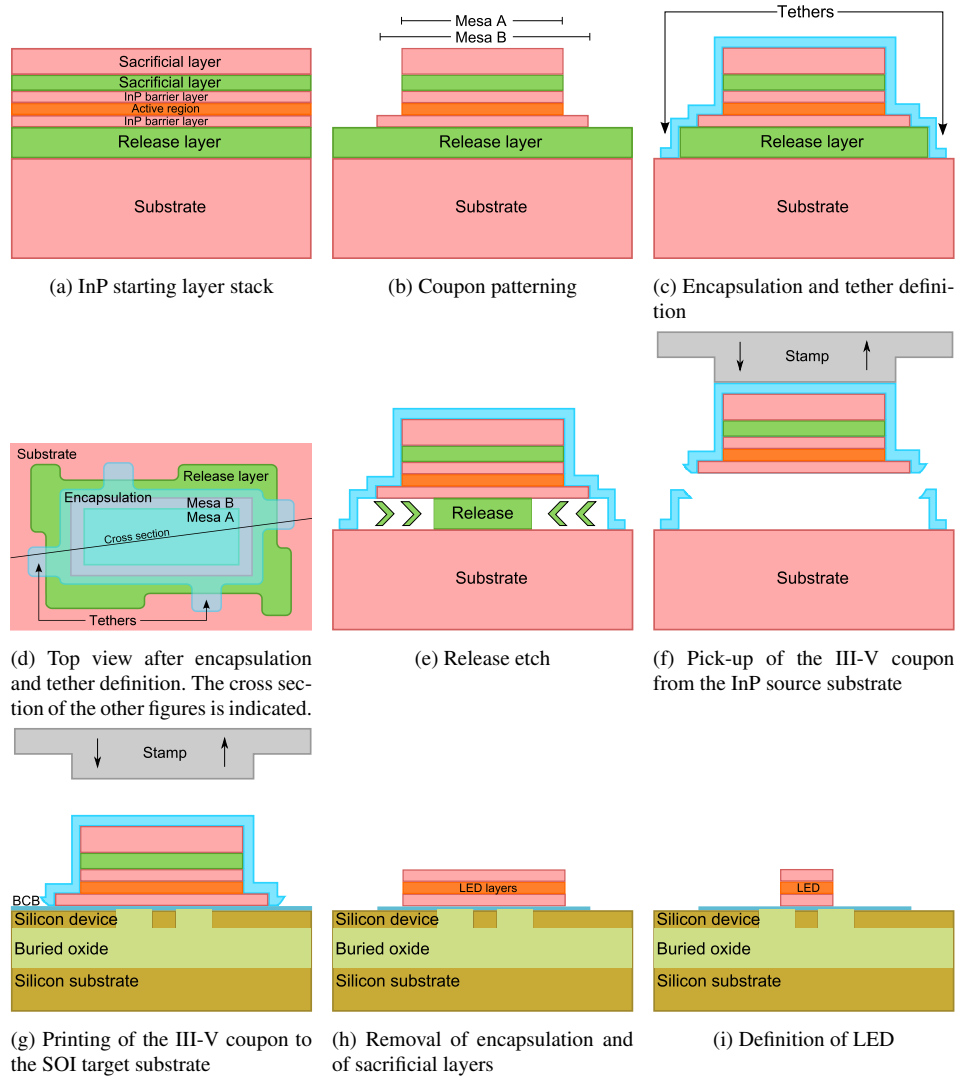


Fig. 2: Process flow of transfer printed, optically pumped LED

PDMS stamp and after transfer printing onto the target wafer is shown in Fig. 4. For the transfer to planarized SOI waveguide circuits both Van der Waals bonding and adhesive bonding were compared, a FIB cross section of which is shown in Figs. 5a and 5b respectively. As the CMP planarization of the silicon waveguide circuit leaves steps of ~ 20 nm on the surface, in the case of Van der Waals direct bonding voids at the bonding interface can be observed. This issue is resolved by using a thin DVS-BCB adhesive bonding layer. Note that this low-index adhesive layer is also beneficial for the taper structure [10]. After transfer printing the coupon to the DVS-BCB coated SOI waveguide circuit at room temperature, the sacrificial InP-InGaAs layer pair has to be removed by wet etching using $\text{HCl}:\text{H}_2\text{O}$ and $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ respectively. The photoresist encapsulation is first removed by an oxygen plasma, after which the DVS-BCB bonding layer is fully cured at 250°C for 1 hour. After curing the coupons could be exposed to the HCl -based and H_2SO_4 based etchants, without delamination. Van der Waals bonded

Etchant	Observations
H ₂ SO ₄ :H ₂ O ₂ :H ₂ O (1:1:18)	Partial undercutting
H ₃ PO ₄ :H ₂ O ₂ :H ₂ O (1:1:20)	Partial undercutting
Chromium etchant	Partial undercutting
HF:H ₂ O ₂ :H ₂ O (1:1:10)	Full undercutting
	Poor selectivity
	Encapsulation delaminates
Citric acid : H ₂ O ₂ (1:10)	Full undercutting
	Slow etching speed
	Anchors delaminate
Tartaric acid : H ₂ O ₂ (1:1)	Full undercutting
	Selectivity to InP >500
FeCl ₃ :H ₂ O (3 mol/l) @ RT	Full undercutting
	Selectivity to InP >500
FeCl ₃ :H ₂ O (3 mol/l) @ 5°C	Full undercutting
	Selectivity to InP >2000

Table 1: Chemicals tested for undercutting and the observed etching behavior.

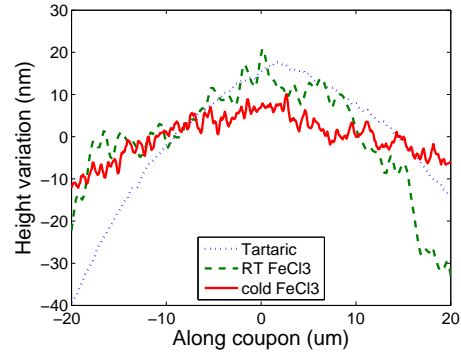


Fig. 3: Height variation along coupon for different etchants

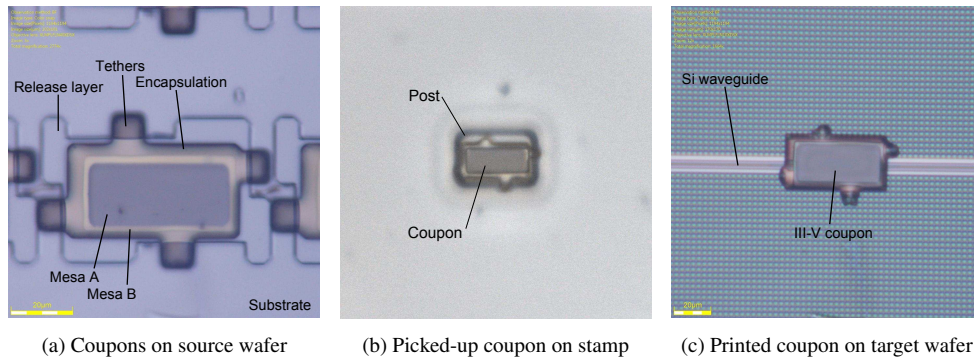


Fig. 4: Microscope images of the coupons before, during and after transfer printing

samples did delaminate, even after extensive annealing, highlighting the beneficial impact of using a thin adhesive bonding layer.

4. Transfer printed light emitting device

As a proof-of-principle for the transfer printing of III-V opto-electronic components to SOI waveguide circuits, a single-spatial-mode broadband light emitting device was designed and fabricated using the transfer printed membrane. Such a component is of great interest for on-chip spectroscopic sensing applications, as it is a low-power consumption, low-cost and robust source compared to tunable lasers and superluminescent LEDs. While tunable lasers provide the highest spectral resolution, they are complex devices, sensitive to environmental fluctuations and external feedback. Superluminescent LEDs are more robust devices but have low efficiency, the main reason for the latter being that only a small fraction of the spontaneous emission couples to the waveguide mode. A spectroscopic system based on superluminescent LEDs requires an integrated spectrometer, which can be done in silicon relying on the CMOS compatible fabrication technology. Also, the fabrication process flow of both tunable lasers and superluminescent LEDs is quite involved. Therefore we have proposed a novel device geometry: by integrating thin high index contrast III-V membranes, an efficient and low-power

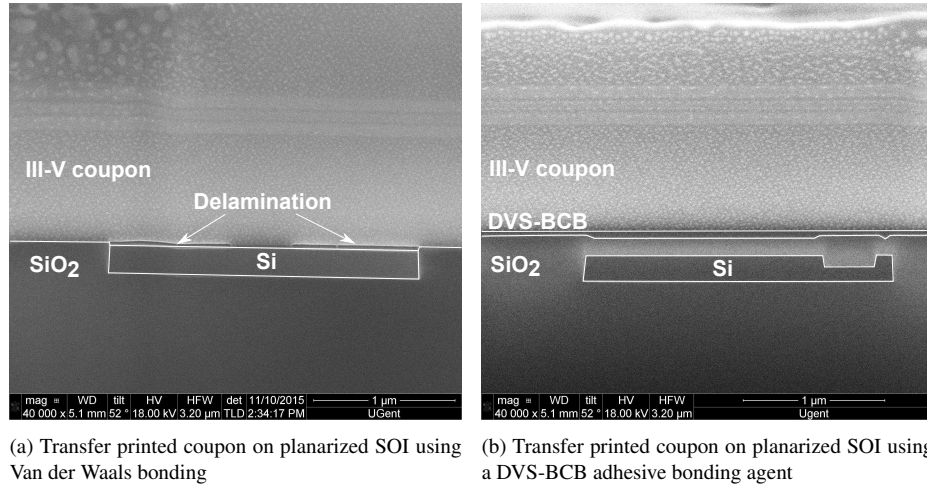


Fig. 5: Cross sections of transfer printed coupons on planarized SOI waveguide circuits

optically-pumped LED can be realized [10]. The proposed device is illustrated in Fig. 6.

A 1310 nm pump laser pumps the LED through the single mode silicon waveguide. The pump light couples up to the high contrast membrane through an adiabatic taper, where it is strongly absorbed. Of the resulting spontaneous emission (around 1550 nm for the quantum well stack used in this experiment), a large fraction ($\sim 10\%$ for transverse electric polarized light in the 200 nm thick III-V membrane used in this work as simulated by FDTD simulations) will couple to the co-propagating and counter-propagating fundamental mode. This fundamental mode couples back down through the same taper into the silicon waveguide [10]. The modal confinement in the active region is simulated to be 38%, ensuring very efficient absorption of the injected pump light. The adiabatic taper structure is a double taper where the III-V membrane waveguide tapers from 500 nm to 1 μm width and the 220 nm thick silicon waveguide from 700 nm to 150 nm width. For a III-V / silicon separation of 150 nm, comprised of 100 nm SiO₂ and 50 nm BCB top cladding and a taper length of 18 μm , as used in the experiment, the simulated transmission between silicon waveguide and III-V membrane waveguide is better than -0.5 dB.

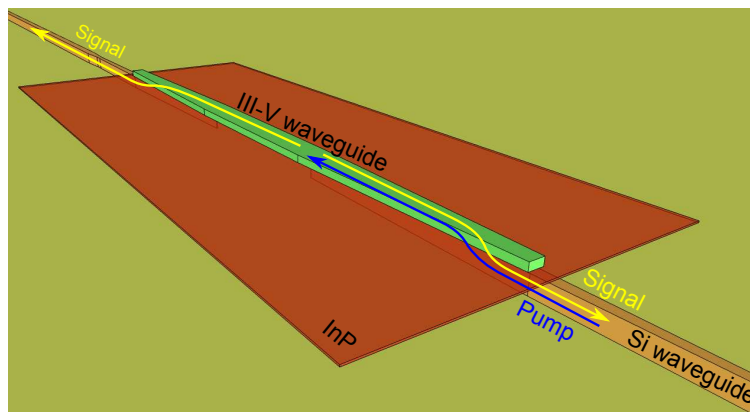


Fig. 6: Illustration of the optically pumped LED.

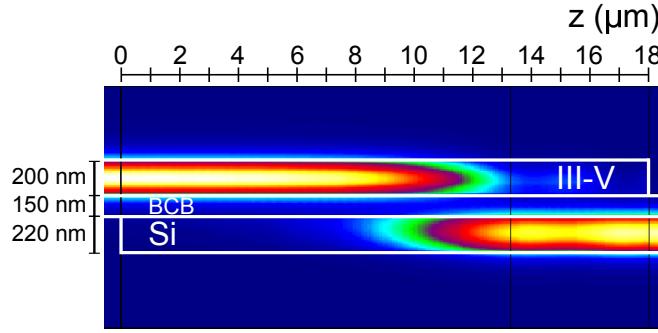


Fig. 7: Sideview of the taper coupling structure intensity profile. 1550 nm light is coupled adiabatically from III-V to silicon waveguide

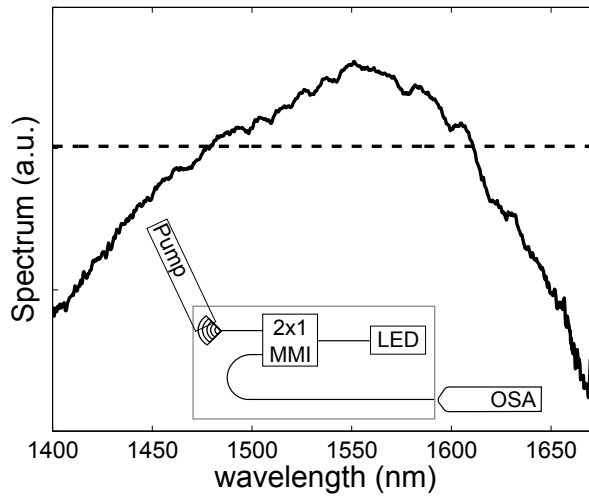


Fig. 8: Measured spectrum of transfer printed, optically pumped LED.

Figure 7 shows the intensity profile of the spontaneously emitted light at a wavelength of 1550 nm being coupled from the III-V membrane waveguide into the silicon waveguide.

The SOI circuit was fabricated in the *imec* CMOS pilot line on 200 mm SOI wafers. After planarizing the photonic integrated circuit down to the silicon device layer, 100nm of SiO₂ was deposited with PECVD, after which a 50 nm thick DVS-BCB layer was spin coated in order to reach the designed bonding layer thickness. III-V coupons were then transfer printed onto the target SOI waveguide circuit using the approach described in the previous section.

To pump the LED, a 1310 nm pump laser was coupled into the waveguide circuit using a grating coupler. After passing through a 2x1 MMI, the LED is pumped. The spontaneous emission that couples to the counter-propagating fundamental mode, travels back to the MMI, where it can be measured on the second port of the MMI, after being coupled through the silicon waveguide facet to a lensed optical fiber. The emitted spectrum from the transfer-printed spatially single mode LED is plotted in Fig. 8. While it was hard to exactly measure the power efficiency in our devices, we are convinced they are of the same order as previously reported by traditional III-V-on-silicon bonding. The 3 dB bandwidth of 130 nm is large, and comparable

as well to previously reported results [10].

5. Conclusion

In this paper, we presented the first III-V opto-electronic components transfer printed on and coupled to a silicon photonic integrated circuit. The transfer printing process flow is discussed. Especially the process to release the III-V coupons from their source substrate is critical. $\text{FeCl}_3\cdot\text{H}_2\text{O}$ at 5°C was found to provide the best etching selectivity and a reasonable undercut etching time for $40\ \mu\text{m}$ wide coupons. To have a good bond of the III-V coupon to the planarized SOI waveguide circuit, a 50 nm thick DVS-BCB bonding layer was used. Successful demonstration of a transfer printed light emitting device is reported. This work forms a stepping stone towards the cost-effective integration of III-V opto-electronic components onto silicon photonic integrated circuits, including lasers, semiconductor optical amplifiers and electro-absorption modulators.

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