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A Technology Based Complexity Model for Reversible Cuccaro Ripple-Carry Adder

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Quantum computing and circuits are of growing interest and so is reversible logic as it plays an important role in the synthesis of quantum circuits. Moreover, reversible logic provides an alternative to classical computing machines, that may overcome many of the power dissipation problems in the near future. In effect, the applied adiabatic signals are known to allow the signal energy stored on the various capacitances of the circuit to be redistributed rather than being dissipated as heat. They additionally avoid calculation errors introduced by the use of conventional rectangular pulses. Some ripple-carry adders based on a do-spy-undo structure have been designed and tested reversibly. This paper presents a simple complexity model taking into account some physical aspects of the technology, from the study of a cascade of Cuccaro adders processed in standard 0.35 μm CMOS technology and used in true reversible calculation (computations being performed forwards and backwards such that addition and subtraction are made reversibly with the same chip), through both, simulations and experimental results. This paper provides a simple physical complexity model as basis for future cost models.

Keywords: Reversible Computing, Complexity, Logical Depth, Pass-Transistor Logic, Ripple-Carry Adder, Sum-Difference Block, Quantum Computation, Adiabatic Signal, Test and Measurement, Error Propagation.

1. INTRODUCTION

Reversible computing has useful applications both in lossless classical computing[1] and in quantum computing.[2] Besides, the power consumption by reversible circuits is low compared to the consumption by conventional restoring circuits.[3–7]

Nevertheless, reversible computation functioning we are implementing is based on reversible dual-line complementary pass-transistor CMOS logic[8] and does not make use of a buffer of any sort nor level restorer. This is different from conventional restoring circuits. Thus, several models such as complexity models, cost models and even electrical simulations of pass-transistor gates have been found either to lack precision or to be inappropriate for reversible circuits.[9] Moreover, little documentation is provided concerning cost models and complexity models for reversible circuits. The aim of the paper is to bring additional information on the impact of the reversible circuit structure on the signal reliability and to provide a basis for a first physical complexity model.

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A cascade of our well documented reversible adder will serve as a basis to propose a first model aiming at presenting the complexity of reversible circuits. The main performances of the adder may be found in Refs. [10, 11]. In a first section, we will briefly summarize the history of the circuit and describe its structure. A second section will introduce the model applied to the reversible circuit inner blocks. A third part will compare simulations and measurements.

2. SHORT HISTORY AND DESCRIPTION OF THE REVERSIBLE ADDER CASCADE CIRCUIT

2.1. Short History

In 2005, Cuccaro et al.[12] presented a new linear-depth ripple-carry quantum addition circuit making use only of controlled-NOT (CNOT or Feynman) gates and controlled–controlled-NOT (CCNOT or Toffoli) gates. In 2010, Takahashi et al.[13] presented an adder with smaller depth. Both circuits are an improved version of a V-shaped reversible adder presented by Ref. [14]. In 2008,[15] presented the synthesis and design of a reversible Fourier

transform making use of such a reversible adder, but using a do-spy-undo (majority–unmajority) scheme structure as firstly presented by Ref. [16]. This design was making use only of controlled-NOT (Feynman) gates and controlled-SWAP (Fredkin) gates.[a] This adder has been extended in larger components such as a multipliers[17,18] and, embedded more recently, in a H264/AVC encoder[19,20] and widely studied in Refs. [7, 9–11]. Extra details about synthesis discussion, structure and theoretical consumption can be found in Refs. [13, 21].

2.2. Cascade of Adder Structure

Figure 1 presents the quantum diagram of a 2 bits Cuccaro adder. Let us assume the data flow from left to right. The forward calculation, from left to right, performs an addition with carry-in c_{in} of two words a and b of $n = 2$ bits.

The result output is the sum S, the carry-out C_{out} and an extra ancilla word A which is a copy of the input a, provided for reversibility such that in reverse computation, the subtraction with carry $S - A$ can be performed. The subtractor may be obtained either by reversing the data flow or by horizontally mirroring the circuit such that the outputs of the adder become the inputs of the subtractor. When cascading an adder and a subtractor, a new block is obtained that performs the identity function by computing the sum and uncomputing it (subtraction), such that the outputs should equal the input.[b]

The implemented cascade chip embeds two sub-blocks: the former is formed by a cascade of 2 identity blocks (4 Cuccaro adders in total), the latter is composed of a cascaded of 4 identity blocks (8 Cuccaro adders in total). Each identity block as a depth of $n = 4$ bits. The appropriate sub-block length can be selected via a selection bit l commuting reversible multiplexers such as those used in Ref. [22]. The 2 identity blocks is selected when $l = 0$ and the 4 identity blocks when $l = 1$ respectively.

A photography of the core cell of the chip is given Figure 2.

We can easily recognize the 4 and 8 adders sub-blocks in the center of the photo as well as the two multiplexer lines, the former at the top right corner, the latter at the bottom left corner.

3. DESIGN AND REALIZATION

The studied Cuccaro adders have been designed using the Cadence© computer-aided design environment software. Each electrical simulation has been performed using its Cadence Spectre© simulator.

[a]Both Fredkin and Toffoli gates are universal gates, which means that any logical or arithmetic operation can be constructed entirely of one of those gates.

[b]Of course, this is true only from a mathematical point of view as in reality, the circuit has an influence on the physical signals that can be measured. The output signals are modified by the computation as discussed in the third section.

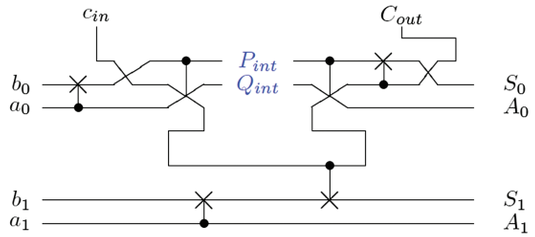


Fig. 1. Full quantum diagram of a 2 bits Cuccaro adder.

The cascade of 4 bits adder chip has been processed at ONSemiconductor through the Europractice/IMEC consortium in 350 nm standard CMOS technology. Figure 2 presents a photography of the realized circuit (approximately 1290 μm $\times$ 345 μm). The transistor lengths used are $L = 350$ nm, both for n-type and p-type transistors, while widths are respectively $W_n = 500$ nm and $W_p = 1500$ nm. The chip contains a total of 2064 transistors (1032 n-type and 1032 p-type).

4. PHYSICAL COMPLEXITY OF THE CUCCARO ADDERS

For simplicity, the model will be presented on the basis of only one Cuccaro adder, while in Section 4.3, the study will be extended to a cascade of several chips such that a cascade of up to 128 adders will be discussed.

In Refs. [9–11], we already explained that the most extreme case for computation with do-undo structured circuits is found when the signal c_{in} has to propagate through the whole computation flow from c_{in} to C_{out} (adder) or from C_{out} to c_{in} (subtractor), as it has to be transmitted twice at each stage of the calculation.

Let us define the signal complexity ${}^tC$ of a gate, block or cell, as the number of basic gates (either Feynman or Fredkin), one given signal has to pass through from input to output. This complexity number should not take into account the gate if the signal only passes the control point of a gate. This corresponds to the gate cost of the corresponding gate, block or cell, from the point of view of a given signal. This complexity ${}^tC$ will, of course, depend on the design of the chosen circuit but also on the inputs as "*reversible circuits built of transmission gates may be considered as reconfigurable circuits, reprogrammed at each calculation step by their input data themselves, the data*

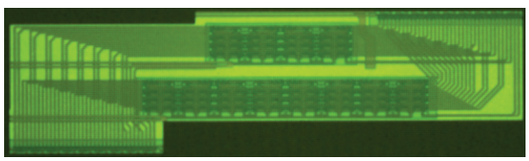


Fig. 2. Photography of the processed cascade of reversible adders (approximately 1400 μm $\times$ 350 μm). The two sub-blocks are visible, as well as the two multiplexer lines.

propagation flow also being the reprogrammation data flow."[11]

We will see later that it may be useful to introduce an extra complexity number related to the number of gate control points (GCP) one signal activates. This complexity number will be notes ${}^{c}C$.

Let us define now the global complexity ${}^{g}C$ of a gate, block or cell as the highest value found among all signal complexities ${}^{t}C$ for one given input signal. We then have ${}^{g}C = f(\max[({}^{t}C + {}^{c}C)_i])$ where i is the number of possible input combinations. The function f will be defined later in the experimental part. We will show that each circuit has a maximal global complexity limitating the number of such gates that may be cascaded. If the total complexity of a cascaded circuit is reached, the output signals are no more properly defined, risking computation errors by wrong output levels.

In addition to ${}^{t}C$ and ${}^{g}C$ let us define a third complexity number ${}^{p}C$ defining the number of times one same signal is passing through a gate, block or chip.

The maximum complexity numbers found experimentally, will be respectively noted C_{tx}, C_{gx} and C_{px}. They will give the experimental limits to the size of a given reversible circuit. In effect, if one wants a reversible circuit to functionate properly, its global complexity, for example, should be inferior or equal to the experimental complexity C_{gx}.

4.1. Complexity of Majority–Unmajority Blocks

Depending on the input vector, the Majority–Unmajority (MU) block will have a different logical equivalent quantum circuit. Let us check the different possibilities and search for their corresponding complexities.

In the adder (subtractor), as the do-spy-undo structure is used, each bit, except the most significant bit (MSB), necessitates one do-undo circuit. Let us recall from Ref. [11], the schematics of the 3 inputs majority do circuit and the 3 inputs unmajority undo circuit respectively in Figures 3 and 4.

The do-undo block constitutes a one bit adder when used forward and a one bit subtractor if used backward. When an addition is computed (forward calculation), the internal bits C_{int} are used for carry transmission from one stage to the next during the majority operations, while the input C_{int} of the undo block computes C_{out} during the

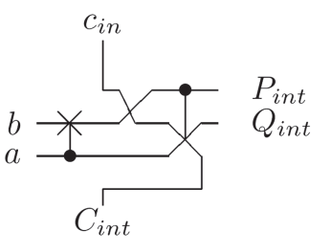


Fig. 3. Quantum diagram of a majority (do) block.

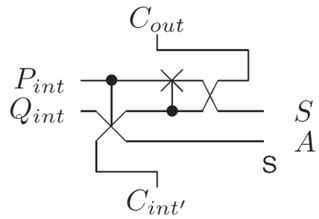
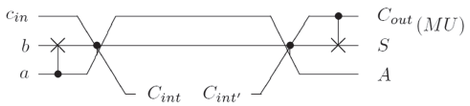


Fig. 4. Quantum diagram of an unmajority (undo) block.

undo operations. The inverse process occurs when backward computation is done, leading to the calculation of the difference.

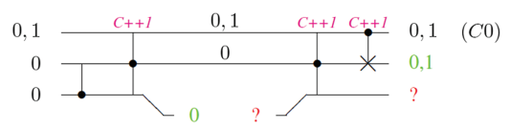
For 1 bit calculation, C_{int} would be directly connected to C_{int} whereas if the adder size $n \geq 2$, the most significant bits addition is performed by using only two Feynman gates; one is used to compute the bit sum XOR ($\oplus$) and the other to sum-up the carry to the final result. Each extra bit addition is realized by cascading supplementary do-undo blocks, linked together by connecting C_{int} to c_{in} and C_{out} to C_{int} as presented in the full schematic of the 2 bits adder in Figure 1. A 4 bits Cuccaro adder necessitates three do-undo blocks. The quantum schematic of an isolated Majority–Unmajority (MU) Block is given below:



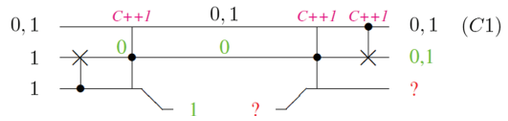
We easily recognize, now connected together, both the Majority and Unmajority Blocks already presented respectively in Figures 3 and 4. The internal carry C_{int} being sent to the next bit weight, either can it be modified and sent back to C_{int0} or sent once more to a next stage and so on until it is eventually sent back into C_{int0} or propagated to S or A in one of the stages.

A peculiarity induced by the use of dual signals, is that the negation of a signal corresponds to the swapping of the two lines that constitute the data. As for example, the signal $(a0; a0)$, after computation, is found either at $(A0; A0)$ or at its complement $(A0; A0)$.

If the input vector $(b; a) = (0; 0)$, the Majority–Unmajority block's equivalent quantum circuit becomes:

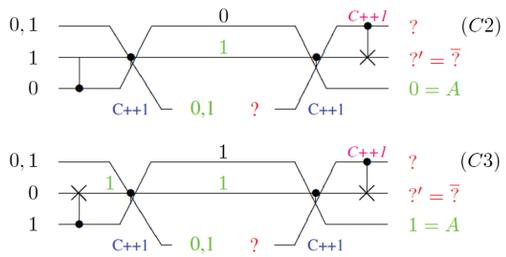


In the same manner, if the input vector $(b; a) = (1; 1)$, its equivalent quantum circuit becomes:



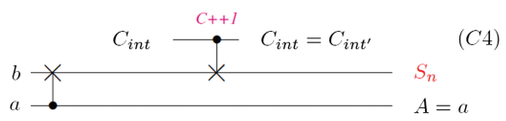
For both cases (C0 and C1), a complexity $Cp = 1$ is found. Indeed, the carry c_{in} crosses the Majority–Unmajority block once from input to output. Despite this, a complexity ${}^{t}C = 2$ has to be assigned to for the carry signal, as, within the block, it has to pass through two inactive Fredkin gates, one in the Majority block and one in a Unmajority block. The carry c_{in} being straightly transmitted from input c_{in} to output C_{out}, we can suppose that for these two cases, the number of circuits possibly cascaded will be high, what is indeed verified experimentaly, as discussed below. For both cases, ${}^{c}C = 1$ as the Feynman gate is controlled by c_{in} in the Unmajority block.

Different equivalent quantum circuits are found with the input vector $(b; a) = (1; 0)$ in case (C2) or $(b; a) = (0; 1)$ in case (C3):



In both cases (C2 and C3), the signal c_{in} is sent to the upper bit weight C_{int} and is recovered after the partial computation (signal C_{int0}). Thus, for that input vector $(b; a) = (1; 0)$ and considering the carry signal only, the complexities ${}^{p}C = 2$ and ${}^{t}C$ is found to be equal to 2 also, as for one Majority–Unmajority block c_{in} has to pass one active Fredkin gate in the Majority block, and another active Fredkin gate in the Unmajority block (C_{int} becoming C_{int0}). In (C2) and (C3), ${}^{c}C$ is also equal to *1*, just like for (C0) and (C1), as the carry signal has to pass the Feynman's gate control point of the Unmajority block.

The Most Significant Bit of the Cuccaro adder is built with a termination block composed of only two Feynman gates (C4). Thus, this block needs to be considered separately from the others.



Whatever its input vector may be, this layer has no impact on the complexity if we consider-as we did so far–that the control of a gate has not to be taken into account in the incrementation of the complexity. Thus, ${}^{t}C = 0$ and ${}^{c}C = 1$ for the termination block and for the carry signal point of view.

If in a first rough approximation we consider that the gate control point has no influence on the signal, we can exclude ${}^{c}C$ from the calculation of ${}^{g}C$. We then obtain ${}^{g}C = {}^{t}C$. In the opposite, if we consider that a gate control point has exactly the same influence as passing through the gate, then we obtain ${}^{g}C = {}^{t}C + {}^{c}C$. The reality is probably somewhere in between, as a gate control point is, on the physical circuit, the physical gate of a transistor, thus introducing extra capacitances on the physical signal line. Nevertheless, its influence should be small in comparison with the physical signal propagating through a logical gate as in this case, the physical signal has to go through at least one transistor channel, which introduces larger capacitance effects as well as extra resistive effects.

The Table I summarizes the different results according to the input vectors for the two extreme cases ${}^{g}C = {}^{t}C$ (controls not included) and ${}^{g}C = {}^{t}C + {}^{c}C$ (controls included).

We now are able to calculate the complexities for the Cuccaro adder and for the carry signal, given a particular input vector.

4.2. Complexity of One Cuccaro Adder

Let us consider the simple case of a 3 bits Cuccaro adder.

When looking at the input bits from the Least Significant Bit (LSB) up to the Most Significant Bit (MSB), each time $a_i = b_i$, means that the carry propagates to the next bit weight $I + 1$ calculation block, thus increasing the signal complexity ${}^{t}C$ for the first i found. By the way, this increases the cell complexity ${}^{g}C$ for the carry signal.

As for example, when considering the addition of the two binaries $a = 001$ and $b = 010$ will lead to a complexity ${}^{t}C = 2$ for the LSB, ${}^{t}C = 2 + 0 = 2$ for the middle bit and 0 for the MSB. The complexity ${}^{g}C$ is then found to be equal to 2 if ${}^{c}C$ is neglected. If we take into account the controls in this calculation, ${}^{c}C = 1$ for the LSB, ${}^{c}C = 1$ for the next bit and ${}^{c}C = 1$ for the MSB, such that ${}^{g}C$ becomes $\max(3; 4; 1) = 4$.

In addition, taking a physical point of view, the difference between the ^{t}C introduced by a cell can be preponderated according to its physical impact on the real signal. The impact of a control is to introduce a capacitance on the signal line whereas the impact of a Feynman gate or a Fredkin gate is to introduce the transconductance

Table I. Complexities of the majority–unmajority and termination blocks for the carry signal, as a function of the input vector when the gate control points are either taken into account or not for the calculation of the global complexity.

Input vectors	Cases	Complexity numbers			Controls excluded	Controls included
(b, a)	(MU)	${}^{t}C$	${}^{p}C$	${}^{c}C$	${}^{g}C$	${}^{g}C$
(0, 0)	C0	2	1	1	2	3
(1, 1)	C1	2	1	1	2	3
(1, 0)	C2	2	2	1	2	3
(0, 1)	C3	2	2	1	2	3
(b, a)	C4	0	1	1	0	1

of one transmission gate in addition to the corresponding capacitances.

In reality, the cascade of gates is similar to the series connection of impedances. We then have several potential dividers in the circuit. The transistors being active, their impedance is not linear with the charge. As far as the voltage is high enough through all the voltage dividers, the transistor will act as a good open circuit and a correct output signal is found. But if the impedances become too important, one voltage divider may pull one transistor in its linear characteristic. Then, a drastic reduction of the output signal occurs with, as a consequence, a cascade of bad signals propagating through the circuits, causing some other transistors to work in their linear regime. The circuit is no more a cascade of open or closed switches but a cascade of resistors, leading the output signals to be somehow randomly modified with a drastic reduction of their level according to these voltage dividers as described in Ref. [11].

4.3. Complexity of Unmajority–Majority Blocks

The same study has to be done for the reverse calculation (subtraction) if the circuit is not perfectly symmetric as it is generally the case. It suffices to flip the circuits right to left in order to obtain the schematics (C1 to C9) with the corresponding Table II.

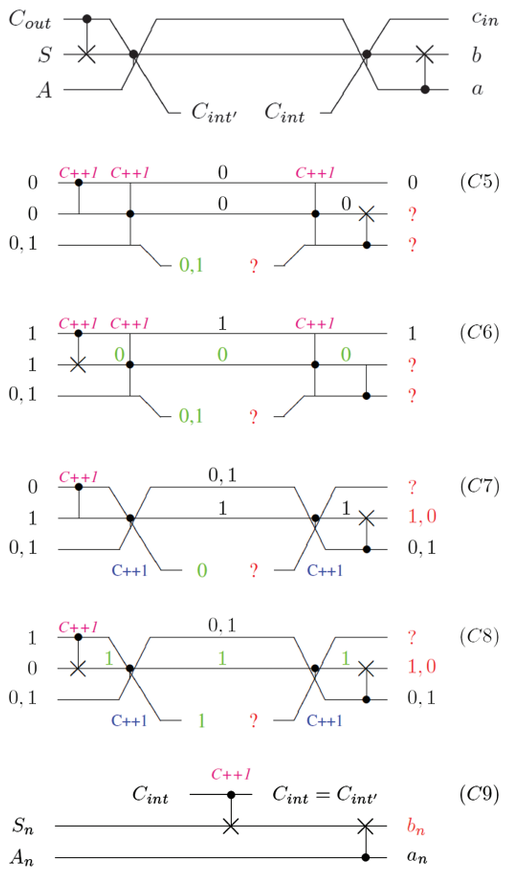


Table II. Complexities of the unmajority–majority and termination blocks for the carry signal, as a function of the input vector when the gate control points are either taken into account or not for the calculation of the global complexity.

Input vectors	Cases	Complexity numbers			Controls excluded	Controls included
(C_{out}, S)	(UM)	${}^{t}C$	${}^{p}C$	${}^{c}C$	${}^{g}C$	${}^{g}C$
(0,0)	C5	2	1	1	2	3
(1,1)	C6	2	1	1	2	3
(1,0)	C7	2	2	1	2	3
(0,1)	C8	2	2	1	2	3
(b, a)	C9	0	1	1	0	1

4.4. Complexity of Chip Cascaded Cuccaro Adders

In order to find the experimental ${}^{n}M$ a circuit can support, we can cascade several identical circuits. Cascading identity blocks (computed and uncomputed function), allows to quickly check the computed output. If the logical result should be identical to input, the physical output signal will be slightly modified until the output vector turns wrong.

One can choose, instead of trying randomly different input vectors, the ones giving the theoretically highest complexity ${}^{g}C$ which should corresponds to the worst case. For the 4 bits Cuccaro identity circuit, this is found when the cases (C2) or (C3) are activated by the input vectors at each stage of the adder circuit. The second part of the identity block being just the mirroring of the adder, the cases (C7) or (C8) will automatically be activated for the subtractor. These constraints are obtained among the calculations performed with input vectors realizing $a_i = b_i$. In these computations, the carry will propagate at each stage of the circuit, such that the global complexity number will be maximal.

For the 4 bits identity circuit, whenever $a_i = b_i$, each Majority–Unmajority block as well as their mirrored Unmajority–Majority ones will increment ${}^{g}C$ by 2 or 3 units, depending on the inclusion of the GCP. The last stage will increment ${}^{g}C$ by *1* only if the GCP are included:

$$ {}^{g}C = 2 \times (3 \times 2 + 0) = 12 \quad \text{when CGP are excluded} \quad (1) $$

$$ {}^{g}C = 2 \times (3 \times 3 + 1) = 20 \quad \text{when CGP are included} \quad (2) $$

If $a_i = b_i$, then we obtain $12 \leq {}^{g}C \leq 20$. In the opposite, the best case is obtained when the carry do not propagate to another stage, thus ${}^{g}C = 2$ for the carry signal.

This means that a coefficient 6 or 10 is found between the two extreme cases, depending on the inclusion of GCP. The range of ${}^{g}C$ can be reduced, only if a more accurate ratio is known between ${}^{c}C$ and ${}^{t}C$ such that:

$$ \beta = {}^{c}C/{}^{t}C \quad (3) $$

$$ \alpha = 1 + \beta \quad (4) $$

$$ \Rightarrow \quad {}^{g}C = \alpha.{}^{t}C \quad (5) $$

5. EXPERIMENTAL RESULTS FOR THE CASCADE OF UNITY BLOCKS CIRCUITS

When properly measured alone, the cascaded identity blocks chip gives very good results, introducing no error whatever are the chosen input vectors. This was expected from simulation, even if, as explained in introduction, the best simulation tools found their limits with pass-transistor technology. In DC simulation, the expected number of possible cascaded gate appears to be huge. In effect, according to Figure 5 presenting Spectre simulations of a cascaded of several cascade of identity block chips, the voltage output variation is very slow when plotted as a function of the number of chip cascaded. Even when $l = 1$, meaning that a cascade of 4 identity blocks (8 Cuccaro adders) is selected inside the chips, the variation after 9 chips is less than 1%.

The experimental measurements presented Figure 6, have been performed using a simple oscilloscope Tektronix TDS 210 with a classical $\times 1$ or $\times 10$ probe. The $\times 1$ probe can be represented as a 72 pF capacitance in parallel to a 1 MΩ resistor. The $\times 10$ probe can be represented as a 22 pF capacitance in parallel to a 10 MΩ resistor.

These measurements present a drop of 6% of the output signal. They are performed using best case input vectors: all the inputs are defined to 1 such that $a0 = b0 = a1 = b1 = a2 = b2 = a3 = b3 = 1$. Thus, only (C1) stage configurations are used for the Majority–Unmajority blocks. Nevertheless, a 10% drop of the output voltage amplitude is only found after 15 cascaded chips, which corresponds to 120 cascaded Cuccaro adders. By extrapolation, a maximal acceptable drop of about 40% of the output signal[9] would be found around approximately 55 cascaded chips (440 Cuccaro adders).

When considering the worst cases, this number is to be divided by 6 to 10, as previously calculated, leaving respectively only 5 to 9 possibly cascaded chips. This illustrates the impact of the the propagation of the carry through all the stages of the circuit.

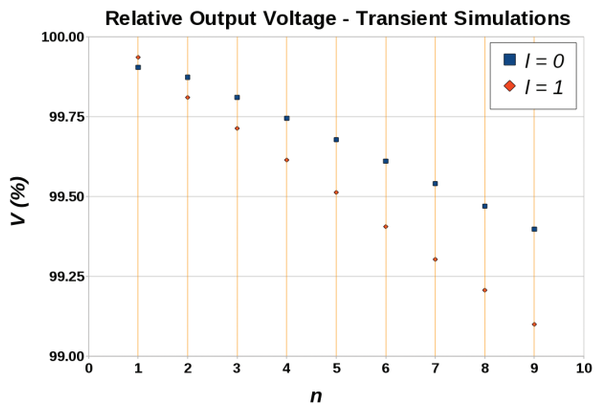


Fig. 5. Spectre DC simulation of a cascade of cascaded identity blocks chip.

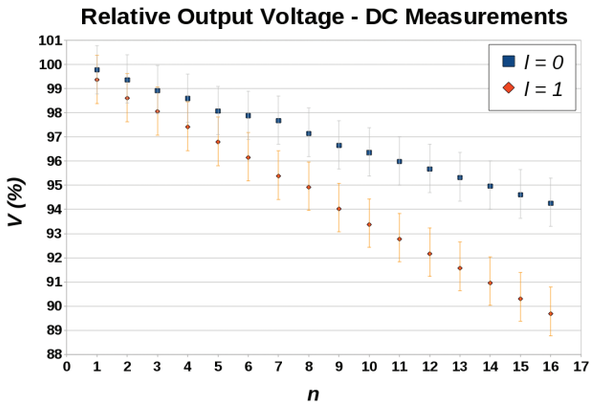


Fig. 6. Experimental measurement of a cascade of cascaded identity blocks chip.

Moreover, in adiabatic calculation, all the capacitance effects will occur, drastically reducing the maximal number of chips possibly cascaded. As one of the worst cases, $a_i = b_i$, the values $c_{in} = 0$, $a = 15$ and $b = 0$ have been taken (i.e., $[Cin_0 = Cin_1 = Cin_2 = Cin_3 = 0]$, $[a_0 = a_1 = a_2 = a_3 = 1]$ and $[b_0 = b_1 = b_2 = b_3 = 0]$ respectively).

The frequency used for adiabatic computation is 100 Hz for an input voltage amplitude of 1.5 V.

Under these conditions, the experimental maximum possibly cascaded chips found, now drops down to 2 (8 identity blocks, 16 Cuccaro adders).

Nevertheless, this small number is not to be directly used for the calculation of ${}^{n}M$. In effect, the measurement probe itself, has a non-negligible impact on the circuit, causing an undervaluation of the true number. This can easily be verified by performing measurements using different probes. By simulation also, we found that the capacitance value of the probes used for measurement lead to earlier computation errors, thus reducing the maximum number of possibly cascaded circuits. The $\times 1$ probe having a larger capacitance, its influence on the measurement is larger compared to the use of the $\times 10$ probe.

Nevertheless, even a $\times 10$ probe impacts the results. The use of an operational amplifier mounted as a follower does help, but only slightly improve the results, even if its input capacitance is smaller than the probes one. This allows anyway to increase ${}^{n}M$ closer to the values calculated previously. As we can see, finding the real experimental ${}^{n}M$ value of a circuit without the probe influence, is experimentally not simple. A better solution would be to include inside the processed chip, at the end of the cascade of identity circuits, a local measurement block with a minimal capacitance.

Reducing the range of ${}^{g}C$ values necessitates to obtain a good approximation of the value. In this optic, let us notice that ${}^{c}C$ occurs, when a physical signal will activate a gate: in other words, when the signal is applied to the gate of a transistor. ${}^{t}C$, occurs when the physical signal is passing through the channel of a transistor.

From this, we see that the resistance contribution to be considered for evaluating ${}^{c}C$ is composed of a small resistances due to wires and gate metalisations, which are of the order of few tens on ohms, while for ${}^{t}C$, the resistance will correspond to the access resistances to the source and drain of the transistors with additional channel resistances. The total resistance will be in this later case, of the order of few kiloohms.

We can deduce from the DC measurements, that if we consider only the resistive aspects, this would lead to neglect ${}^{c}C$ in the calculation of ${}^{g}C$.[c] Thus, the main physical parameter to take into account for the evaluation of ${}^{g}C$ is the capacitance effect.

A solution to evaluate the experimental capacitances of the circuit is proposed in Ref. [7] and will not be develop in the present paper. Another possibility, is to use the model of the transistor to compare the influence of the capacitances, both from the point of view of one physical signal activating a GCP and from the point of view of one physical signal passing through the gate.

We may approximate their contributions, based on the well known simplified schematic of the capacitances of the MOS transistor presented Figure 7.

In Figure 7, *G* designs the Gate of the transistor, *S* the source, *D* the drain, and *B* the Bulk. The five considered capacitances link respectively two of these transistor terminals. From the Gate, the total capacitance to be considered is formed of the two capacitances *CGD* and *CGS* in parallel, with the additional *CGB* such that:

$$C_{\text{Gate}} = (C_{\text{GS}} + C_{\text{GD}}) + C_{\text{GB}} \tag{6}$$

From the transistor channel, the total capacitance to be considered is more complicated as in addition to the previous capacitances, we find the two capacitances C_{SB} and C_{DB} in parallel such that:

$$C_{\text{channel}} = (C_{\text{GS}} + C_{\text{GD}}) + (C_{\text{SB}} + C_{\text{DB}}) \tag{7}$$

In a first approximation, if we consider the complexity parameter directly linked together with the capacitances, the parameter can be calculated as:

$$\beta = \frac{C_{\text{Gate}}}{C_{\text{Channel}}} \tag{8}$$

$$= \frac{(C_{\text{GS}} + C_{\text{GC}}) + C_{\text{GB}}}{(C_{\text{GS}} + C_{\text{GD}}) + (C_{\text{SB}} + C_{\text{DB}})} \tag{9}$$

During the reading of the computed results, the transistor used in the pass-transistor gates will work in the triode mode. In other words, the gate–source voltage v_{GS} is larger than the threshold voltage v_T and the drain to source voltage v_{DS} is almost null thus inferior to the saturation voltage v_{DSsat}. In that regime, C_{GB} can be neglected, thus $C_{\text{GB}} = 0$. This lead to the simplified equation:

$$\beta = \frac{(C_{\text{GS}} + C_{\text{GC}})}{(C_{\text{GS}} + C_{\text{GD}}) + (C_{\text{SB}} + C_{\text{DB}})} \tag{10}$$

When neglecting the gate overlap capacitances, we also have:

$$C_{\text{GS}} = C_{\text{GD}} = \frac{1}{2} \cdot W \cdot L \cdot C_{\text{ox}} \tag{11}$$

where W is the transistor width, L its length and C_{ox} the oxide capacitance of the transistor Gate. this lead to:

$$C_{\text{Gate}} = (C_{\text{GS}} + C_{\text{GD}}) + C_{\text{GB}} \tag{12}$$

$$\simeq 2 \cdot \frac{1}{2} \cdot W \cdot L \cdot C_{\text{ox}} + 0 \tag{13}$$

$$= W \cdot L \cdot C_{\text{ox}} \tag{14}$$

On the channel point of view, C_{SB} and C_{DB} must be added. In bulk technologies, they both correspond to the diffusion junction capacitances under source and drain respectively. If the side-wall capacitances are neglected we obtain:

$$C_{\text{SB}} \simeq C_{j0} \cdot \left(1 + \frac{V_{\text{SB}}}{\psi_0}\right)^{-M_j} \tag{15}$$

$$C_{\text{DB}} \simeq C_{j0} \cdot \left(1 + \frac{V_{\text{DB}}}{\psi_0}\right)^{-M_j} \tag{16}$$

where C_{j0} is the junction capacitance at zero bias. C_{j0} is highly process dependent. M_j is the junction grading coefficient, typically given between 0.5 and 0.33 depending on the abruptness of the diffusion junction. Ψ_0 is the built-in potential depending on the doping levels such that:

$$\psi_0 = \nu_T \cdot \ln\left(\frac{N_A \cdot N_D}{N_i^2}\right) \tag{17}$$

where N_A and N_D are the doping level of the body and source/drain diffusion region respectively and N_i the intrinsic carrier concentration in undoped silicon.

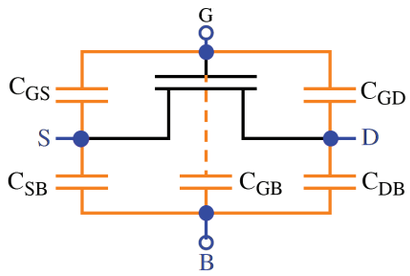


Fig. 7. Simplified schematic of the main capacitances of a MOS transistor.

[c]The serial resistance of reversible circuit can easily be found both in DC and adiabatic calculation. The DC measurement Figure 6 allow to avoid all the capacitance effects such that we can estimate the resistive impact of each adder to 10 kΩ/adder which is coherent with previous results provided in Ref. [11] and also closer to simulation results than the previous evaluation.

As we can see, all these parameters are highly process dependent. Anyway, C_{SB} and C_{DB} are typically few times as larger than the gate capacitance such that $\beta \leq 1/3$, but hardly less than 2/9 on optimized technologies.

But let us assume, for the purpose of the modeling, that 4 is the maximum number of chips that can be cascaded when the charge at the output of the circuit is negligible. ${}^{N}M_x = 16$ is then the experimental maximal number of identity circuit possibly cascaded. As the worst case is used, we can define ${}^{C}M_x = {}^{n}M_{x.}{}^{g}C = {}^{n}M_{x.}\alpha.{}^{t}C = 192.\alpha$.

6. CONCLUSION

The present paper presents a simple complexity model for dual-line pass-transistor architecture circuits, discussing links between some parameters of the process technology used and the maximal number of possibly cascaded gates. The model has been applied to simulations and experimental measurements of a cascade of V-shape Cuccaro ripple carry adder fabricated in the 350 nm CMOS technology and used in both directions: forward adder and backward subtractor.

This model tends to confirm that V-shape circuits may not be appropriate to pass-transistor reversible circuits as they drastically increase the complexity of circuits by propagating the carry through several stages of the circuit.

The maximal complexity ${}^{C}M$ will depend on the chosen technology where capacitances and resistances introduced by the transistors are different, but whether or not ${}^{C}M$ is independent on the circuit structure for a given technology is still work in progress.

This well documented Cuccaro circuit already fabricated in several technological nodes may serve as a basis to propose a first technology dependent cost model.

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