# The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time ΣΔ Modulators

Bart De Vuyst, Pieter Rombouts, Jeroen De Maeyer, and Georges Gielen

This document is an author's draft version submitted for publication at IEEE TCASII
The actual version was published as:
Bart De Vuyst, Pieter Rombouts, Jeroen De Maeyer, and Georges Gielen "The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time ΣΔ Modulators," IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMSII: EXPRESS BRIEFS, VOL. 57, NO. 6, JUNE 2010

# The Nyquist Criterion: a Useful Tool for the Robust Design of Continuous-Time $\Sigma\Delta$ Modulators

Bart De Vuyst, Pieter Rombouts, Jeroen De Maeyer and Georges Gielen

***Abstract*—In this paper we introduce a figure of merit for the robustness of continuous-time $\Sigma\Delta$ modulators. It is based on the Nyquist criterion for the equivalent discrete-time (DT) loop filter. We show how continuous-time modulators can be designed by optimizing this figure of merit. This way we obtain modulators with increased robustness against variations in the noise-transfer-function (NTF) parameters. This is particularly useful for constrained systems, where the system order exceeds the number of design parameters. This situation occurs for example due to the effect of excess loop delay (ELD) or finite gain bandwidth (GBW) of the opamps.**

**Additionally, it is shown that the optimization is equivalent to the minimization of $\mathcal{H}_\infty$, the maximum out-of-band gain of the NTF. This explains why conventional design strategies that are based on $\mathcal{H}_\infty$, such as Schreier's approach, provide quite robust modulator designs in the case of unconstrained architectures.**

***Index Terms*—analog-to-digital (A/D) conversion, continuous-time sigma-delta ($\Sigma\Delta$) modulation, Nyquist stability criterion, robust stability.**

## I. Introduction

TODAY'S wireless and wire-line communication requires analog-to-digital (A/D) converters with 12-bit accuracy or more. Due to oversampling and noise-shaping, $\Sigma\Delta$-modulation A/D-converters are well-suited for these applications. Discrete-time (DT) $\Sigma\Delta$ modulators have become very mature because of the implementation with switched-capacitor (SC) circuits. They have dominated the $\Sigma\Delta$ modulator designs for many years [1]. Furthermore, the existence of well known design strategies has even enhanced their popularity [2]. However, in today's submicron CMOS technologies it is no longer straightforward to implement SC circuits due to the limited supply voltage. Special techniques such as bootstrapping are inevitable to obtain good performance [1].

Continuous-time (CT) $\Sigma\Delta$ modulators have attracted more attention because of their possibility of extending the signal bandwidth further into the wide MHz range. Here the unity gain bandwidths (GBWs) of the operational amplifiers only have to exceed the sample frequency by a factor 2 or less [3]. This is in contrast with DT modulators where usually a factor 5 or more is used [1]. CT modulators with large signal bandwidths and high accuracy are usually achieved by combining a low oversampling ratio (OSR) with a multi-bit quantizer. In the rest of this paper we will assume the use of multi-bit quantization. In that case replacing the quantizer by an additive white-noise source is well justified.

This work was supported by the Fund for Scientific Research (F.W.O.-Vlaanderen). Bart De Vuyst and Pieter Rombouts are with the Electronics and Information Systems Laboratory (ELIS), Ghent University, B-9000 Gent, Belgium (e-mail: bart.devuyst@elis.ugent.be). Jeroen De Maeyer is with the Electrical Energy, Systems and Automation Laboratory (EESA), Ghent University, B-9000 Gent, Belgium. Georges Gielen is with the Microelectronics and Sensors Division (MICAS), Department of Electrical Engineering (ESAT), Katholieke Universiteit Leuven, 3001 Heverlee, Belgium.

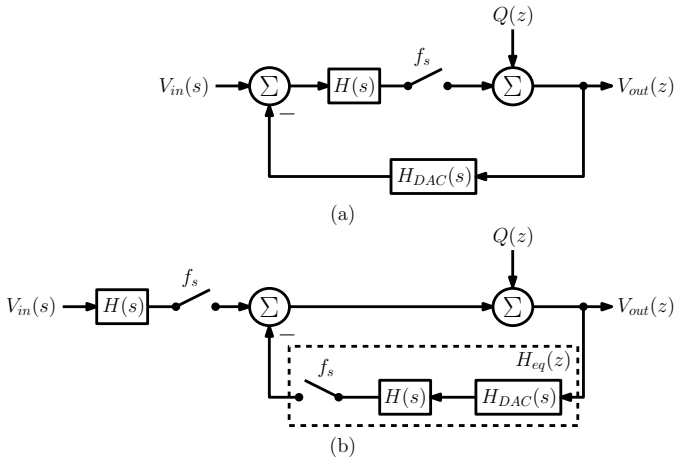


Fig. 1. Linear block diagram of a CT $\Sigma\Delta$ modulator (a) and identification of the equivalent DT loop filter (b).

In fig. 1 (a) the linearized block diagram of a CT $\Sigma\Delta$ modulator is shown. $V_{in}(s)$ equals the continuous-time analog input, $V_{out}(z)$ the digital output and $Q(z)$ represents the discrete-time quantization noise input. One can identify the loop filter $H(s)$, the feedback digital-to-analog converter (DAC) $H_{DAC}(s)$ and the sampler with sample frequency $f_s = \frac{1}{T_s}$. In the rest of this paper $f_s$ will be normalized to 1 for notational simplification. The block diagram can be rearranged as in fig. 1 (b). The loop filter $H(s)$ and sampler are shifted into the feedback path and the input is now sampled before entering the loop. This way, the whole loop can be described by an equivalent discrete-time loop filter $H_{eq}(z)$ as indicated by the dashed rectangle. The cascade of $H_{DAC}(s)$, $H(s)$ and the sampler can be converted to $H_{eq}(z)$ using the impulse-invariant-transformation (IIT):

$$\begin{aligned} H_{eq}(z) &= \text{IIT}\{H(s)H_{DAC}(s)\} \\ &= \mathcal{Z}[\mathcal{L}^{-1}(H(s)H_{DAC}(s))|_{t=nT_s}] \end{aligned} \tag{1}$$

Mathematically, it is obtained by taking the inverse Laplace transformation ($\mathcal{L}^{-1}$) of $H(s)H_{DAC}(s)$, sampling the result and finally performing the $\mathcal{Z}$-transform. This way a similar definition for the noise-transfer-function (NTF) as for the case of a DT $\Sigma\Delta$ modulator can be adopted:

$$NTF(z) = \frac{1}{1 + H_{eq}(z)} \tag{2}$$

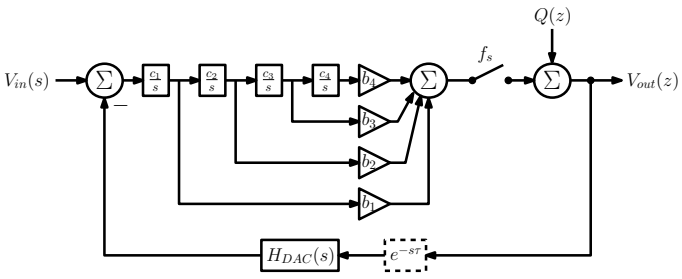


Fig. 2. A fourth-order CT $\Sigma\Delta$ modulator in FF topology with the effect of excess loop delay indicated by the dashed rectangle.

This well known relation allows us to use a unified framework for both DT and CT $\Sigma\Delta$ modulators with respect to their noise shaping. Using the $*$-operator to denote the sample operation as in [4], the output can now be written as:

$$V_{out}(z) = \big[\underbrace{H(s)NTF(e^s)}_{STF(s)} V_{in}(s)\big]^* + NTF(z)Q(z) \quad (3)$$

The response to the input is denoted by the signal-transfer-function (STF), which should be close to unity in the signal band [5]. The system behaves slightly differently than a DT modulator, as the input is lowpass filtered before being sampled. This clearly reveals the implicit anti-aliasing filter advantage of CT modulators [6].

Equations (1) and (2) reveal that the design of CT $\Sigma\Delta$ modulators could be completely mapped on the well known design strategies for DT modulators. In section II this straightforward design strategy is analyzed. We will see however that it will not always give satisfactory results, as it ignores some important parasitic effects of CT $\Sigma\Delta$ modulators. In some cases it can even lead to unexpected instability. Therefore, in section III we will investigate stability robustness against these parasitic effects based on the Nyquist criterion. With this knowledge, a new design strategy is proposed in section IV and some design examples are given.

## II. Straightforward Design Strategy for Continuous-Time $\Sigma\Delta$ Modulators

Using equations (1) and (2), the straightforward design strategy unfolds in two steps. The first step is the selection of a NTF, based on the required specifications. Because of its popularity, we will focus on Schreier's algorithm for this purpose [2]. This algorithm places the NTF poles in a Butterworth position. The only design parameter is $\mathcal{H}_\infty$, the maximum out-of-band gain of the NTF. Its value symbolizes a tradeoff between system performance and instability due to quantizer overloading. In the second step, a continuous-time loop filter is determined which implements the chosen NTF. This is done by using equation (2) and the inverse IIT. Assuming that all the NTF zeros are located at DC ($z = 1$), the loop filter looks like:

$$H(s) = \frac{a_{N-1}s^{N-1} + a_{N-2}s^{N-2} + \ldots + a_1 s + a_0}{s^N} \quad (4)$$

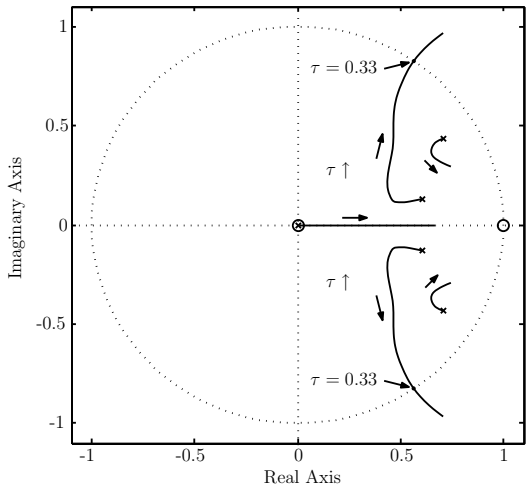


Fig. 3. Root locus of the NTF of a fourth-order CT $\Sigma\Delta$ modulator with rising loop delay. The x-marks indicate the pole locations when $\tau = 0$.

with $N$ the order of the modulator. The NTF pole locations are determined by the coefficients $a_i$. This loop filter is constructed as a cascade of $N$ integrators. There are two popular implementations: the feedforward (FF) and the feedback (FB) topology. In the rest of this paper we will use the FF topology. However, all results are equally valid in the case of a FB topology. The FF topology is illustrated in fig. 2 for a fourth-order CT $\Sigma\Delta$ modulator. The $a_i$'s are now combinations of the integrator coefficients $c_i$ and the feedforward coefficients $b_i$.

Although the straightforward design strategy is mathematically correct, some important parasitic effects that always occur in practical implementations, are not taken into account. We will divide the parasitic effects in two categories: undesired loop dynamics and parameter variations. Both effects will alter the actual CT loop filter and hence the NTF, so that it differs from the intended design. This will influence the performance and can even lead to unexpected instability. For DT modulators these effects tend to be less pronounced and they are typically neglected in the design of the modulator's NTF [1].

### A. Undesired Loop Dynamics

Undesired loop dynamics is a collective term for all parasitic effects of the CT loop filter which generate extra poles and zeros in the resulting NTF. This way the system order increases, while the number of design parameters $a_i$ remains $N$. The extra poles and zeros cannot be set independently anymore and we will speak of a *constrained system*. In the other case where the number of NTF poles exactly equals the number of design parameters, full control over the pole positions can be obtained and we have an *unconstrained system*.

A well known example of undesired loop dynamics is the effect of excess loop delay (ELD) [7]. ELD models the finite decision time of a real-life quantizer. In the block diagram it can be included by introducing an analog delay time $\tau$ in front of the feedback DAC as indicated by the dashed rectangle in fig. 2. For multi-bit quantization it can also include the delay of dynamic element matching (DEM) techniques, necessary to improve the feedback DAC performance. In fig. 3 the root

locus of the NTF for a fourth-order CT $\Sigma\Delta$ modulator is shown when $\tau$ is rising. One can see that the system order is increased by one, through the appearance of an extra pole on the real axis and a zero at $z = 0$. For $\tau = 0$ this pole and zero cancel at $z = 0$, but for rising $\tau$ the extra pole moves along the real axis. The other poles also shift positions for rising $\tau$, while the zeros always remain at their initial positions. Eventually, for a loop delay exceeding approximately one third of the sampling rate, the system becomes unstable.

In reality, the loop delay is not fixed but depends on the quantizer input level. Typically the quantizer delay will be larger for smaller input signals. Therefore the system behaviour will become signal dependent and spurious tones will appear in the output spectrum. A possible solution to make the loop delay fixed is the introduction of a synchronization latch in front of the feedback DAC [3]. The clock signal for this latch is usually a delayed version of the system clock by a half or a quarter of the clock period. This way only the delay of the feedback DAC contributes to the variable part of the loop delay, which can be made small by design.

Another important example of undesired loop dynamics is the effect of finite GBW when using active-$RC$ integrators. These integrators are constructed with local feedback around an operational amplifier. As the current consumption of an operational amplifier typically rises with the GBW, we want to keep it as low as possible. In practice, especially the GBW of the first integrator in the loop filter is important. Due to thermal noise considerations, this integrator typically consumes most of the current and thus reducing the GBW here is most effective. Due to its finite GBW the transfer function of the first integrator includes an extra pole [8]:

$$ITF_{GBW} \approx \frac{c_1}{s} \frac{\omega_{GBW}}{s + \omega_{GBW} + c_1} \tag{5}$$

This will also result in an extra pole and zero in the NTF. In contrast with loop delay, the designer has (nearly) full control on the opamp's GBW and hence it can be included as an extra design parameter. In [8] it was shown that finite GBW can be approximated by an equivalent extra loop delay. Therefore the resulting root locus of the NTF is very similar to fig. 3.

### B. Parameter Variations

In practice, the integrators are implemented either with active $RC$ or $g_mC$ circuits. In both cases the integrator coefficient is formed by the product of a resistor value (or the reciprocal of a transconductance) and a capacitor value. As these coefficients reside from two elements of a different type, there is a large inaccuracy on their exact values. Deviations can be up to 20 % in modern CMOS technologies. Hence, the actual value of an integrator coefficient can be modeled as:

$$c_{i,act} = c_{i,nom}(1 \pm \delta) \qquad \delta \leq 20\,\% \tag{6}$$

The deviation parameter $\delta$ is in fact a statistical variable, originating from a zero mean Gaussian distribution. Since devices of the same type can be matched with an accuracy of 0.1 % in modern CMOS technologies, $\delta$ can be considered equal for all integrator coefficients within the same modulator.

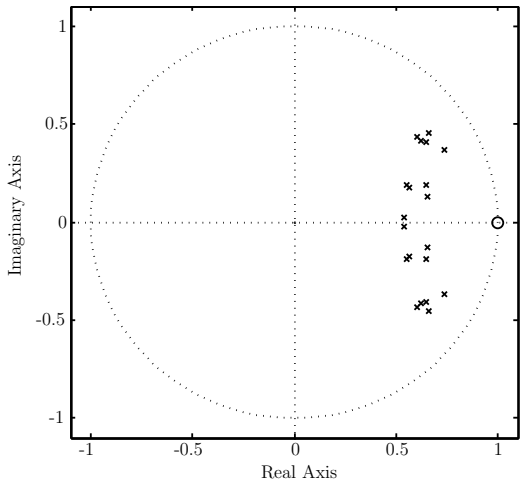


Fig. 4. NTF pole-zero plot of 5 actual implementations for a fourth-order CT $\Sigma\Delta$ modulator with parameter variations.

Fig. 4 shows a pole-zero plot of 5 NTFs for a fourth-order CT $\Sigma\Delta$ modulator with parameter variations. Only the pole locations are shifted now, but the system order is not increased. The zeros remain at DC as they originate from the analog integrator poles at $s = 0$. The actual performance can be quite different than expected. Variations in peak signal-to-noise ratio (SNR) up to 20 dB were found for this particular example.

A DT $\Sigma\Delta$ modulator suffers much less from parameter variations because its coefficients are now only susceptible to capacitor mismatch, which can achieve an accuracy of 0.1 %.

## III. Nyquist Criterion For Robust Stability

The stability of CT $\Sigma\Delta$ modulators is examined here with the Nyquist criterion for the equivalent discrete-time loop filter. A stability robustness figure of merit is also introduced to express the system's sensitivity to parameter variations.

### A. Discrete-time Nyquist Criterion

Similar to continuous-time systems, the stability of a closed-loop discrete-time system can be investigated by means of the open-loop transfer function. For CT $\Sigma\Delta$ modulators we are interested in the Nyquist plot of $H_{eq}(z)$. This Nyquist plot is constructed by evaluating the equivalent loop filter at $z = e^{j\omega}$, where $\omega$ goes from $-\pi$ to $\pi$, and plotting the result in the complex plane. In fig. 5 the DT Nyquist plot of $H_{eq}(z)$ for a fourth-order CT $\Sigma\Delta$ modulator is shown. At $\omega = \pi$ the Nyquist plot ends on the real axis. This is in contrast with CT systems where the Nyquist plot always ends in the origin for $\omega \to \infty$. Also due to the four resonant poles at $z = 1$, the Nyquist plot closes at infinity, indicated by the dashed lines in fig. 5. The arrows indicate the direction of rising frequency.

The number of unstable poles of the closed-loop system can now be identified by the following equation [9]:

$$Z = P - N \tag{7}$$

where $Z$ is the number of unstable closed-loop poles, $P$ is the number of unstable open-loop poles and $N$ is the net number

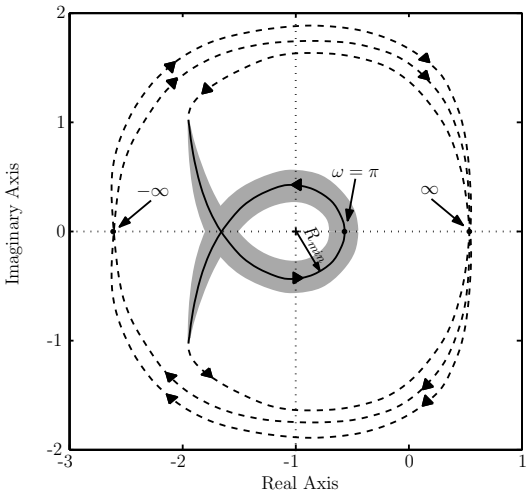


Fig. 5. Nyquist plot of $H_{eq}(z)$ for a fourth-order CT $\Sigma\Delta$ modulator. The dashed lines indicate the encirclements at $\infty$ due to the resonant poles. The gray band around the nominal curve shows the effect of parameter variations.

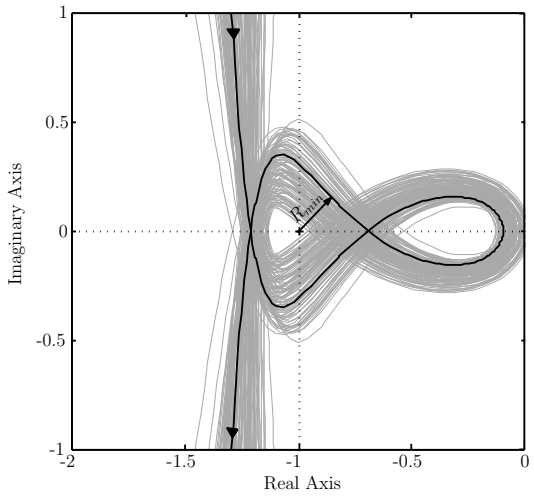


Fig. 6. Nyquist plot of the optimized $H_{eq}(z)$ for the fourth-order design example with inclusion of ELD and finite GBW of the first integrator in the nominal design. The arrow indicates the $R_{min}$ value of the nominal design. The gray curves are the Nyquist plots due to parameter variations.

of counterclockwise encirclements of the critical point $-1$. As resonant poles (poles on the unity circle) do not account for unstable open-loop poles, the net number of encirclements for practical CT $\Sigma\Delta$ modulators should be zero. This is the case in fig. 5 when also including the encirclements at infinity.

### *B. Stability Robustness Figure of Merit*

In the previous section we saw that parameter variations slightly shift the NTF pole locations. It is however important that the modulator always remains stable. Therefore a stability figure of merit needs to be introduced to denote the system's robustness against parameter variations. Popular stability figures are gain margin and phase margin [9]. They indicate the system's robustness against extra gain in the loop and extra phase shift respectively. However, in this case we expect the variations to be complex combinations of both gain and phase changes. Therefore we choose the minimum distance $R_{min}$ from the Nyquist curve to the critical point $-1$ as a stability robustness figure (indicated with an arrow in fig. 5):

$$R_{min} = \min_{\omega} |1 + H_{eq}(e^{j\omega})| \tag{8}$$

As stability is determined by the number of encirclements of $-1$, a dangerous situation occurs when the Nyquist curve comes close to this critical point. In that case parameter variations, which create a band of Nyquist curves around the nominal curve as indicated in gray in fig. 5, can very easily change the number of encirclements and hence create instability. We conclude that large values of $R_{min}$ will thus give rise to better robustness against parameter variations.

### *C. Relation to $\mathcal{H}_\infty$ Design*

Surprisingly the value of $R_{min}$ can also be linked to $\mathcal{H}_\infty$, the maximum out-of-band gain of the NTF, as:

$$\mathcal{H}_\infty = \max_{\omega} |NTF(e^{j\omega})| = \left[\min_{\omega} |1+H_{eq}(e^{j\omega})|\right]^{-1} = \frac{1}{R_{min}} \tag{9}$$

Hence designing with the $R_{min}$ criterion is in fact equivalent to using $\mathcal{H}_\infty$ as design parameter. This means that even in the multi-bit case, $\mathcal{H}_\infty$ is a good parameter to indicate the system's stability robustness.

## IV. Application to Design

### *A. Design Strategy*

From section III it is clear that undesired loop dynamics can have a detrimental effect on the actual modulator performance. Therefore it is our opinion that these effects should already be taken into account in the nominal design. The actual modulator then only deviates from this nominal design by parameter variations. As this can still lead to unexpected instability we will try to make the nominal design as robust as possible against these parameter variations. For this purpose we will maximize the $R_{min}$ robustness criterion from the previous section. Equivalently, this boils down to the minimization of $\mathcal{H}_\infty$. Similar to Schreier's algorithm, $\mathcal{H}_\infty$ is thus the key parameter in the design strategy. However, in Schreier's case only unconstrained systems are considered and a choice for $\mathcal{H}_\infty$ automatically implies a pole constellation. These poles are chosen such that they give rise to a maximally flat NTF. In our proposed approach we will vary the pole constellation until we have found the one which leads to the most robust design (i.e. with the smallest $\mathcal{H}_\infty$). This way our approach can deal with any type of undesired loop dynamics.

In practice the optimization of $\mathcal{H}_\infty$ is performed numerically. In our experiments we have found that standard gradient-based optimization did not perform well in practical cases. This is partially due to the fact that $\mathcal{H}_\infty$ cannot be determined analytically. Therefore we have used a genetic optimizer [10].

### *B. Design Examples*

To illustrate our design strategy we consider a fourth-order design example. We target for 80 dB peak SNR performance. All four NTF zeros are placed at DC ($z = 1$). An oversampling

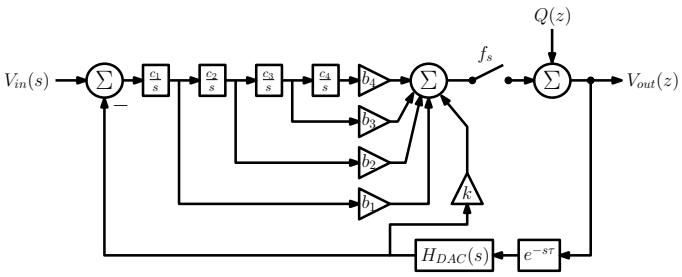


Fig. 7. CT $\Sigma\Delta$ modulator with extra direct feedback path.

ratio (OSR) of 16 is combined with a 4-bit quantizer. The feedback DAC generates a non-return-to-zero (NRZ) pulse. The loop delay is fixed by a synchronization latch to $0.25\,T_s$ and the GBW of the first integrator is set to $f_s$. Let us now consider the design problem of sizing the loop filter coefficients for the architecture of fig. 2 in the presence of these undesired loop dynamics. It is noteworthy that there does not exists a prior-art solution for this problem. E.g. if we set the coefficients to the values for the case without undesired loop dynamics, the resulting modulator is already unstable. However our design strategy provides a simple criterion for tackling this problem by sizing the loop filter coefficients such that the robustness ($R_{min}$) is maximized. This optimization is performed with the boundary constraint that the SNR should be over 80 dB. The result of this procedure gives a value for $R_{min}$ of 0.2 ($\mathcal{H}_\infty = 5$). To investigate the robust stability of the design, a family of 100 modulators with a randomly varied parameter variation $\delta$ (uniformly distributed between $\pm 20\,\%$) of the integrator coefficients was generated. The feedforward coefficients were all set to 1 and are assumed to be free of parameter variations. In fig. 6 the resulting Nyquist plots are shown. The black curve represents the Nyquist plot of the nominal system and the gray curves are the Nyquist plots due to parameter variations. None of the gray curves crosses the critical point and thus all modulators remain stable.

It is common practice to avoid the constraintness of the system by the introduction of an extra direct feedback path [3]. This feedback path is situated directly at the input of the quantizer as illustrated in fig. 7. An extra design parameter $k$ is now present. Since the finite GBW of the first integrator is approximately equivalent to an additional loop delay [8], the combined effect of an actual loop delay and finite GBW only gives rise to one extra pole in the resulting NTF. Hence, the value of $k$ can be used to change the position of this pole and the resulting system is unconstrained. If we apply our optimization strategy to this system with the extra feedback path, there is one extra design parameter, and clearly the resulting design will be more robust than the previous one. The result of the optimization procedure now gives a value of 0.47 for $R_{min}$ ($\mathcal{H}_\infty = 2.1$). As the system is now unconstrained, Schreier's maximally flat NTF can also be implemented. With the numerical values of this example, Schreier's approach requires that $\mathcal{H}_\infty$ should be equal to 2.3 ($R_{min} = 0.43$) for 80 dB peak SNR. Obviously this is only slightly less robust than our optimized design. This way we expect that the maximally flat NTF will be nearly as robust as our optimized design. To asses this, the same Monte Carlo simulations as for the constrained case were performed and it was found that for both design strategies all modulators were stable even with parameter variations as large as $40\,\%$.

This way, we have provided a mathematical argument why Schreier's design approach gives good results in the case where the NTF is unconstrained. In practical cases, the undesired loop dynamics cannot always be approximated sufficiently accurate by an extra loop delay. Hence the extra feedback path does not always ensure unconstrainedness. In this case, a Schreier design is not possible but our approach provides a mathematically sound criterion leading to robust designs.

## V. Conclusion

In this paper a new design strategy for robust continuous-time $\Sigma\Delta$ modulators has been presented. A key element in this strategy is the fact that undesired loop dynamics like excess loop delay and finite unity gain bandwidth of the first integrator are included in the nominal design. Based on the Nyquist criterion, we introduce $R_{min}$ as a stability robustness figure of merit. Next we have shown that this figure of merit is equivalent to $\mathcal{H}_\infty$, the maximum out-of-band gain of the NTF. This is an important result, as it indicates that traditional design approaches that are based on $\mathcal{H}_\infty$ can also give rise to quite robust designs. Obviously these design approaches are only applicable to unconstrained architectures. To overcome this limitation, we propose to determine the loop filter by maximizing the robustness ($R_{min}$). Of course, in the unconstrained case, our new approach can also be used. But here, the resulting modulators are only slightly more robust than modulators designed with the well known Schreier design approach. Numerical examples on fourth order modulators confirm the validity of the approach.

## References

[1] P. Balmelli and Q. Huang, "A 25-MS/s 14-b 200-mW $\Sigma\Delta$ Modulator in 0.18-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2161–2169, 2004.

[2] R. Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 40, no. 8, pp. 461–466, 1993.

[3] G. Mitteregger et al., "A 20-mW 640-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 20-MHz Signal Bandwith, 80-dB Dynamic Range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, 2006.

[4] J. De Maeyer, P. Rombouts, and L. Weyten, "Efficient Multibit Quantization in Continuous-Time $\Sigma\Delta$ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 4, pp. 757–767, Apr. 2007.

[5] J. De Maeyer et al., "Controlled behaviour of STF in CT $\Sigma\Delta$ modulators," *Electron. Lett.*, vol. 41, no. 16, pp. 896–897, 2005.

[6] E. van der Zwan et al., "A 10.7-MHz IF-to-Baseband $\Sigma\Delta$ A/D Conversion System for AM/FM Radio Receivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1810–1819, Dec. 2000.

[7] M. Keller et al., "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma-Delta Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 55, no. 11, pp. 3480–3487, 2008.

[8] M. Ortmanns, F. Gerfers, and Y. Manoli, "Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time $\Sigma\Delta$ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 51, no. 6, pp. 1088–1099, 2004.

[9] G. F. Franklin, J. D. Powell, and M. Workman, *Digital Control of Dynamic Systems*, 3rd ed. Addison Wesley, 1998.

[10] R. Storn and K. Price, "Differential evolution - A simple and efficient heuristic for global optimization over continuous spaces," *Journal of Global Optimization*, vol. 11, no. 4, pp. 341–359, 1997.