# Active asynchronous secondary side voltage clamping

# J. Windels and J. Doutreloigne

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Abstract—An asynchronous active voltage clamp for the secondary side of switching dc-dc converters is proposed. The control of the proposed clamping circuit is independent from the main converter, thus allowing use of a physically small inductor and offering increased control over the clamping operation. Measurements on a 1 MHz implementation of the asynchronous active voltage clamp on the secondary side of a prototype 220 kHz phase shifted full bridge DC-DC converter confirm the effectiveness of the voltage clamping and the improved converter efficiency.

## I. INTRODUCTION

In transformer isolated switching power converters, the secondary side transformer leakage inductance forms a resonant network with the parasitic capacitance of both the transformer and the rectifier. Since ohmic losses in the conductors and transformer windings are low in most switching converters, the ringing phenomenon that occurs at the time of switching has high voltage amplitudes and long settling times. Therefore, either the breakdown voltage of the rectifying devices must be significantly over-dimensioned, which increases the cost and conduction losses of the converter, or a voltage clamp must be added to absorb the ringing energy.

The voltage is clamped by transferring most of the the ringing energy to a clamping capacitor. This capacitor is typically much larger than the parasitic capacitances, thereby limiting the rise in voltage. In steady state conditions, the absorbed energy must be removed from the clamp capacitor by the next switching cycle. Dissipative clamps simply dissipate the energy[1], whereas non-dissipative clamps recover most of the energy to the input or output of the converter[2], [3], [4], [5]. Generally, low power converters can suffice with a simple dissipative clamp, whereas the resistor dissipation in medium and high power converters may warrant the additional complexity of a non-dissipative clamp[1].

At least one inductive element, either an inductor or transformer, is required to transfer the energy away from the capacitor in the non-dissipative clamps. In other clamping circuits, the capacitor reset operation is typically synchronized with the converter[2], [3], [4], [5], thereby imposing a lower limit on the inductor size. The proposed clamping circuit operates asynchronously from the main converter, thereby enabling use of a higher switching frequency and drastically shrinking the size of the passive components in the clamping circuit.

#### II. THE ASYNCHRONOUS VOLTAGE CLAMP

The proposed voltage clamp resets the clamping capacitor to the desired voltage by transferring the excess energy to the output of the converter, using a small auxiliary dc-dc converter. The topology selection for this auxiliary converter will be discussed next.

Even without the ringing phenomenon, the rectified voltage amplitude always exceeds the output voltage, since the PWM modulated signal is passed through a low pass filter. To avoid unwanted conduction through the clamping circuit, the clamp capacitor voltage must be at least equal to the rectified voltage in the idealised converter. Therefore, a voltage downconversion is required to transfer energy from the clamping capacitor to the output of the converter. Because the auxiliary converter only transfers a limited amount of power, a low parts count and cost are critical design parameters. Galvanic separation between the input and output of the auxiliary converter is not required, making the buck converter a straightforward choice. The fly-back converter is the only other topology to satisfy the cost and size criteria, but is typically less efficient than a buck converter under similar input and output conditions.

The well known transfer functions of the idealised buck converter in continuous and discontinuous mode remain valid to describe the relation between the duty cycle, input voltage, and output voltage of the converter. However, in this application the output capacitor of the auxiliary converter – which is shared with the main converter – is several orders of magnitude larger than the clamping capacitor. Therefore, adjusting the duty cycle of the auxiliary converter regulates the clamping capacitor voltage instead of the output capacitor voltage.

The UVLO (under-voltage-lockout) feature of most commercially available buck converter IC can be used to regulate the clamping capacitor voltage. The regular feedback network for the IC is dimensioned to ensure the duty cycle remains sufficiently large under all operating conditions. With this control strategy, the switcher IC burst-wise discharges the clamp capacitor to the UVLO voltage. Once the UVLO voltage is reached, the IC is shut down to a low power state for one or more cycles of the main converter, depending on the amount of hysteresis in the UVLO implementation.

Using a non-dissipative clamping circuit allows for an aggressive reduction of the peak voltages in the circuit compared to dissipative clamps, without an excessive negative impact on the converter efficiency. The proposed clamping circuit shares this property with other non-dissipative clamping circuits, while allowing the use of a smaller inductor. In addition, the proposed clamping circuit allows for an intelligent control of the energy absorbed by the clamping capacitor. Other voltage clamping circuits operate regardless of the voltage on the

clamping capacitor, thereby causing unnecessary losses in the clamp resistor or in the non-ideal non-dissipative clamping circuit. By setting an appropriate offset on the UVLO feature, the auxiliary converter discharges the clamping capacitor when required, and shuts down to a low power state for the remainder of the time. This increases the efficiency of the converter by reducing the switching losses in the clamping circuit at lower input voltages.

## III. MEASUREMENTS

The proposed voltage clamp can be implemented on the secondary side of virtually all transformer isolated converters. We present measurements on a prototype phase shifted full bridge converter switching at approximately 220 kHz. The schematic is shown in Figure 1. The secondary side rectifier is implemented as a self-driven synchronous rectifier using MOSFETs, but is shown in the Figure as a diode bridge to simplify the drawing. The active clamp is implemented using an LM3103 buck converter IC with an integrated active rectifier, operating at 1 MHz, combined with a 3 mm x 3 mm x 1.5 mm SMT inductor.

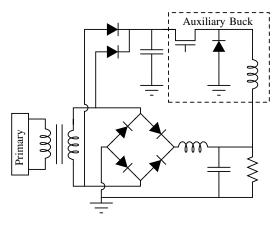


Fig. 1. Converter secondary with auxiliary buck converter to discharge clamp capacitor

TABLE I
COMPARISON OF SECONDARY SIDE VOLTAGE STRESS AND EFFICIENCY OF
THE CONVERTER WITHOUT CLAMP, WITH SEVERAL RESISTOR VALUES IN
AN RCD CLAMP, AND WITH SEVERAL OFFSETS TO THE PROPOSED ACTIVE
CLAMP(AC)

	$V_{ m in}=10V$		$V_{in} = 14V$		$V_{ m in}=20V$	
	$\eta$	$V_{stress}$	$\eta$	$V_{stress}$	$\eta$	$V_{stress}$
Unclamped	0.781	15.4	0.742	21.4	_	_
RCD 1k $\Omega$	0.777	12.9	0.741	18.8	_	_
RCD 100 $\Omega$	0.756	10.3	0.698	14.5	0.621	20.9
RCD 47 $\Omega$	0.727	10.5	0.665	14.2	0.555	20.3
AC (always-on)	0.776	12.4	0.743	14.6	0.690	20.5
AC (10V offset)	0.778	12.5	0.743	14.5	0.691	20.5
AC (12V offset)	0.781	14.5	0.752	16.7	0.690	20.4
AC (15V offset)	0.781	15.3	0.752	18.2	0.690	20.4

In the experimental set-up, the performance of the active clamp — with several UVLO offsets, and in always-on mode

— is compared to the unclamped converter, and to several resistor values in an RCD clamp. Measurements of the converter efficiency and voltage stress on the rectifiers at different input voltages are included in Table I. The devices on the secondary side of the converter are only rated for a breakdown voltage of approximately 20 V, therefore no measurements could be obtained for the high input voltage in the unclamped and 1 k $\Omega$  RCD clamped converter. As an example, we can compare the proposed active clamp circuit in always-on mode with a 47  $\Omega$  RCD clamp. For the 10 V input voltage, the active clamping circuit shows a higher voltage stress than the RCD clamp. However, the voltage is still well within the limits, and efficiency is improved by 4.9 %. For the 14 V and 20 V input voltages, the voltage stress is comparable, and efficiency with the active clamp is improved by 7.8 % and 13.5 %, respectively. The expected increase in efficiency at lower input voltages by disabling the auxiliary converter at low clamp capacitor voltages is also apparent in the Table. The active clamp with a 15 V offset compared to the alwayson clamp achieves a 0.5 % efficiency improvement at 10 V input voltage, and a 0.9 % efficiency improvement at 14 V input voltage, while keeping the voltage stress within limits. For the 20 V input voltage, the efficiency and voltage stress for the always-on clamp and active clamps with different offsets are identical.

In Figure 2a, the voltages on the secondary side transformer connectors with respect to ground are plotted for the unclamped converter. In Figure 2b, the same voltages are plotted for the proposed active clamp in always-on mode. To achieve similar voltage stress on the devices, a 47  $\Omega$  RCD clamp is required, for which the voltages are plotted in Figure 2c.

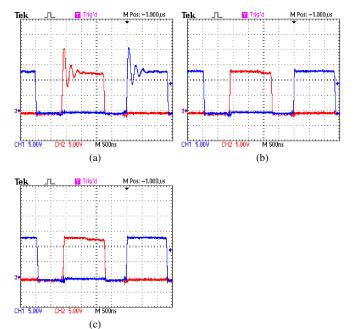


Fig. 2. Secondary side voltages for 14V input voltage without clamp (a), with always-on active clamp (b), and with 47 Ohm RCD clamp (c)

## IV. CONCLUSION

We propose the use of an asynchronous auxiliary converter to recover the secondary side ringing energy to the output. The asynchronous operation allows use of a physically small and inexpensive inductor compared to other non-dissipative clamping circuits. Using the auxiliary converter, the clamping voltage can be accurately controlled, thereby improving the converter efficiency at low input voltages. Measurements using a commercially available buck converter IC as the auxiliary converter on a prototype full bridge converter confirm the voltage clamping abilities of the circuit and show a considerable improvement in efficiency when compared with RCD clamping circuits.

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#### AUTHORS AFFILIATIONS

J. Windels and J. Doutreloigne: CMST, Department ELIS, Ghent University/IMEC, Technologiepark 914a, 9052 Ghent, Belgium

Email: jindrich.windels@elis.ugent.be

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