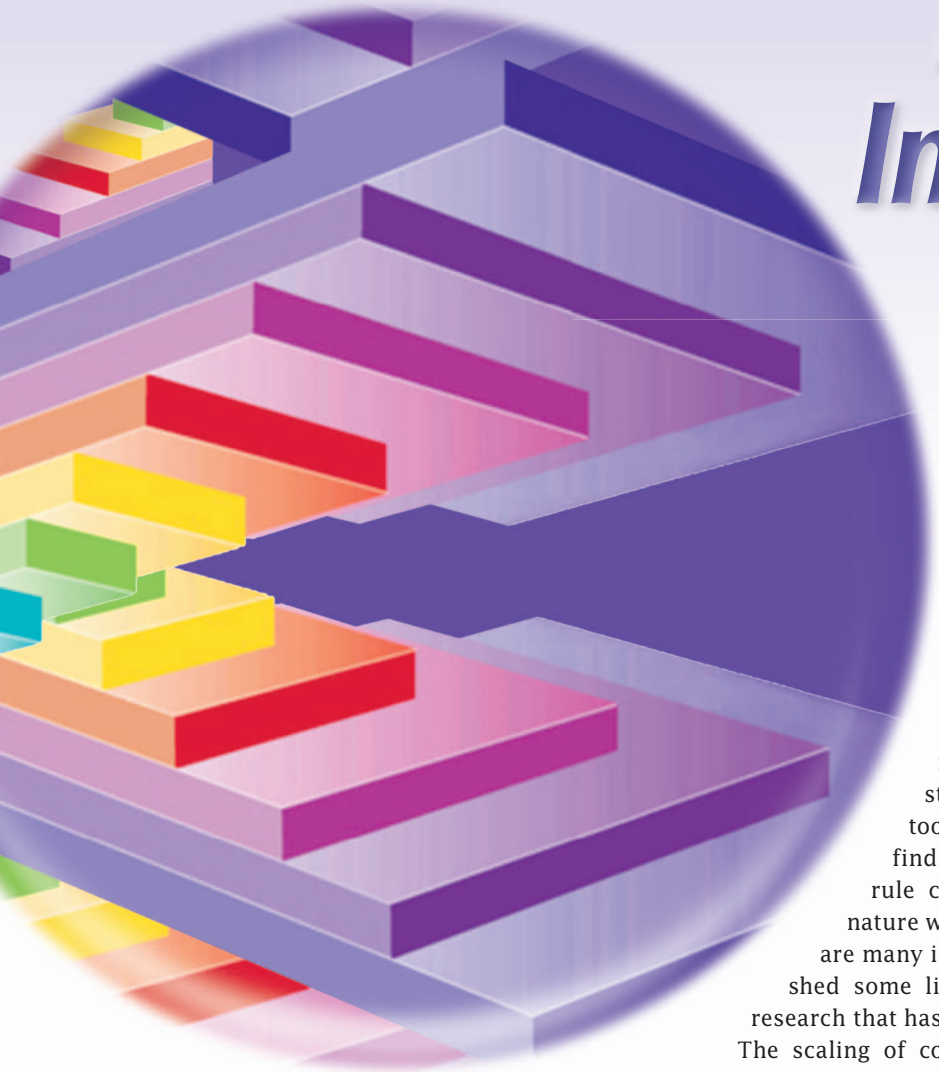
Dirk Stroobandt

Interconnect Research Influenced



How E.F. Rent's decades-old rule and its implications for chip wire lengths have guided the last ten years of interconnect research.

Although Rent's rule was formulated in the 1960s and published worldwide in 1971, it took until the end of the 1990s before its value became clearly apparent, leading to the creation of an entire research field on a priori wire length predictions. Even when the rule itself became quite popular, its inventor, E.F. Rent, stayed in the background: who the man actually was remained a mystery. It was as if Mr. Rent stayed in the prompter's box while others took the stage and spread the word on his findings. In this article, I will show that Rent's rule can be viewed as a fundamental law of nature with respect to electronic circuits. As there are many interpretations of the rule, this article will shed some light on the core of Rent's rule and the research that has been built on it.

The scaling of computer technology has been driven by Moore's law, which states that the number of transistors on a chip doubles with every technology generation. (In the 1970s, the number of transistors doubled every 18 months; later, this was every two years, and over the last decade it has been every three years.) In the 20th century, Moore's law also meant an increase in the clock frequency with every technology generation (Figure 1). This currently is no longer the case, however: clock frequencies are now staying almost the same with each new technology generation. Few people are aware of it, but the reason for this has its basis in Rent's rule.

Although there are many interpretations, Rent's rule basically states that, in a chip design, the number of wires emanating from a region containing B logic blocks (the basic computational elements on chips) grows faster than the perimeter length increase when B grows (Figure 2). Note that this is explicitly a scaling argument and, in principle, assumes an infinitely large circuit. With some calculations, one can deduce from this that the average length of an interconnection on chip must increase with a growing number of

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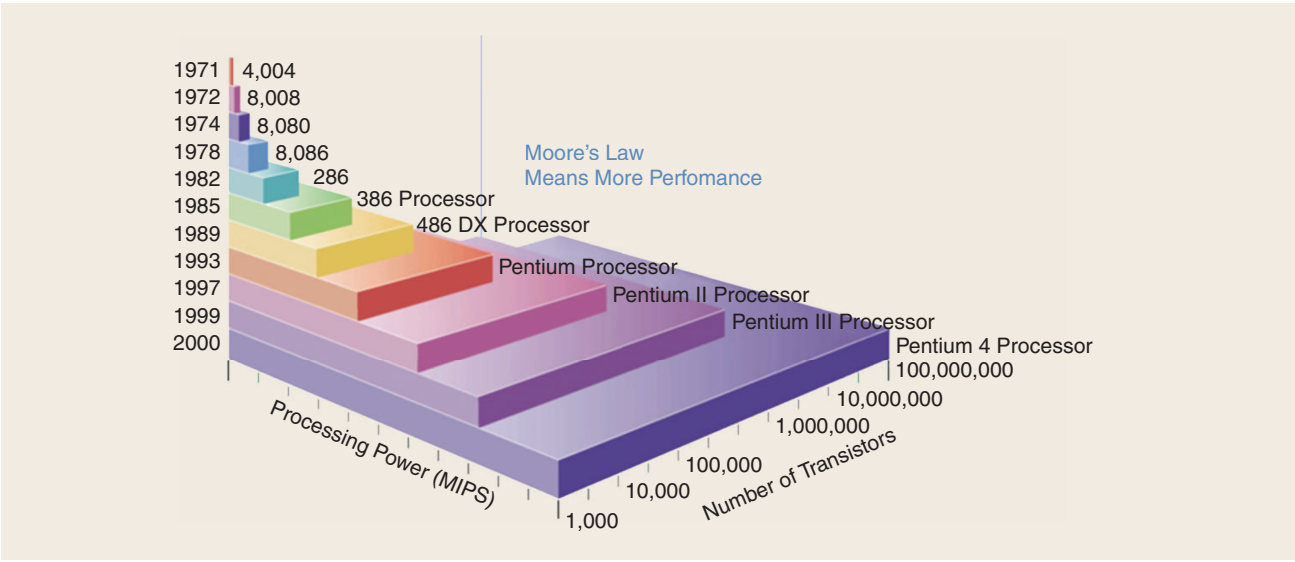

FIGURE 1: Moore's law expresses the exponential progress of technology scaling as an increase in the number of transistors. It has been valid for clock frequency as well.

gates [6]. Since the length of a wire has a large effect on the delay it induces on an electrical signal traveling the distance, the wire delay on chips has surpassed the transistor delay since the end of the 1990s. So while transistors keep on gaining in speed with every new technology generation, the wires in between them induce a relatively larger delay, and this has stopped the clock frequency from continuing to scale up.

Rent's rule, first formulated in the 1960s, is not nearly as well known as Moore's law but it is of a much more fundamental nature. Where Moore's law is a mere observation that has become a self-fulfilling prophecy (with major ASIC technology companies driving their road maps in accordance with it), Rent's rule was largely neglected for a long time. Yet there is no way to circumvent this fundamental rule, and so it had a detrimental effect on the clock speeds of new computer systems.

In this article, I will explain Rent's rule in detail, focus on the wire length estimations that result from it, and present an overview of the myriad of research activities that sprouted from the initial research work on a priori wire length estimates. The final section wraps up with a short look at the future of Rent's rule.

Rent's Rule

In the 1960s, IBM employee E.F. Rent wrote an internal memo that described what later became known as Rent's rule. It wasn't until two other IBM employees, Landman and Russo, wrote a landmark paper in 1971 that Rent's rule was made public [5]. It is actually surprising and a bit mysterious that E.F. Rent never published his findings outside of IBM himself, and it remains unknown (to me at least) why his name was not on the paper written by Landman and Russo—hence the title of this article.

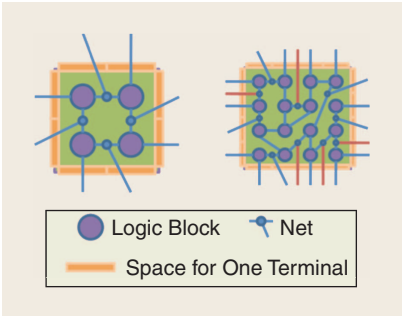

FIGURE 2: Rent's rule states that the number of terminals (wires emanating from a region) grows faster than the perimeter length increase when the number of blocks grows. If the space for one terminal on the boundary scales linearly with the block size, there is a shortage of space for all terminals (red lines lack space).

The Terminal-Gate Relationship of Rent's Rule

In their paper, Landman and Russo discuss ways of optimally partitioning a circuit into modules in such a way that as few interconnections as possible between the modules are cut during the partitioning. The rationale behind this is that connected gates in different modules will be placed further apart than the gates within each module, and therefore this partitioning strategy will keep the connections shorter. In such a strategy, Rent's rule relates the average number of terminals T of a part of any circuit (a module) to the average number of logic gates (basic logic blocks B) inside the module as $t = tB^p$. The parameter t is the average number of terminals per logic gate (if $B = 1$, Rent's rule reduces to $T = t$) and the exponent p is called the Rent exponent. Its value depends on the complexity of the interconnection topology (with higher values for more complex topologies) and on the quality of the placement (with higher values for less placement optimization). The maximal value of the Rent exponent p is one for a very complex topology or a random placement [1].

Rent's rule was found by experimental analysis of many circuit

partitions and proves to be valid for most designs. Figure 3 shows the result of a circuit partitioning in a log-log plot of number of terminals versus number of logic gates. The validity of Rent's rule follows from the fact that all points follow, on average, a straight line in the plot.

Note that there is a deviation from the straight line for high values of T and B that is known as Rent's region II and has been described in [1] and [5]. This deviation at the chip boundary is a direct result of the nature of Rent's rule itself. For circuits with an interconnection complexity p larger than 0.5, the number of pins (terminals at the outermost boundary) scales faster than the perimeter of the boundary (see Figure 2). In practice, the number of pins at the boundary of a chip is limited, and hence the number of signals going out is intentionally lowered by techniques such as serialization of the information stream or encoding of the information in fewer bits. Therefore, the actual number of pins on a chip is significantly lower in real circuits than Rent's rule predicts. It is one of the many misconceptions about Rent's rule (and one that lead to false conclusions in many papers) that Rent's rule fixes the relation between the number of pins of a circuit and its number of internal blocks. Rather, Rent's rule is based on a scaling argument and really captures only the internal interconnection complexity. Another deviation at the low end has also been observed in [8] but this is much less frequent.

Interpretations of Rent's Rule

In the previous section, we in fact already presented two different interpretations of Rent's rule: the one presented in Figure 2 (about the scaling of the number of terminals according to the number of internal blocks if this number grows) and the interpretation based on an "optimal" partitioning (resulting in Figure 3). In fact, Rent's rule has been explained as a fundamental scaling law [10] and it was shown in [1] that Rent's rule applies to any homogeneous design.

A less obvious interpretation, but the one that gives rise to all major uses of Rent's rule, is that it is a measure of interconnection complexity. The reasoning here is that a more complex structure of the wires between the logic blocks means that there are more wires that connect blocks that are less close (in terms of graph distances or, after placement, in terms of actual distances). Hence, it is harder to place such a circuit with short wire lengths. A circuit with simple interconnection complexity, then, is a circuit where all wires are between blocks that are close to each other (again in terms of graph distance). For example, planar graphs are simpler than nonplanar graphs because it is easier to place such circuits in two dimensions. It is clear that in this interpretation, a simpler circuit can be partitioned more easily, with fewer connections to be cut, than a more complex circuit. Therefore the average number of terminals in a partitioned complex circuit will be higher than for a simple circuit, and the Rent exponent will naturally be higher. Therefore, the Rent exponent is a measure of interconnection complexity.

The complexity interpretation also gives rise to a relation between the Rent exponent p and a fractal dimension D that describes the geometric dimension that would be the "ideal" fit for implementing the circuit [10]. One can deduce (through partitioning) that for any D-dimensional mesh the Rent exponent is given by

$$p = \frac{D-1}{d}.$$

Interconnect Length Predictions

The main claim of fame for Rent's rule has come from Wilm Donath's 1979 paper on wire length estimation [3] and a follow-up paper in 1981 [4]. In these papers, Wilm Donath, another IBM employee, used Rent's rule to predict the average wire length and wire length distribution in computer chips before the actual layout. The basic idea is simple and uses a partitioning scheme as the basis of the estimation. The three main models for the layout generation are (see Figure 4) i) a circuit graph model with Rent's rule as the model of its interconnection complexity, ii) a Manhattan grid architecture model where the circuit will be placed and routed, and iii) a model for the placement and routing of the circuit on the architecture.

Donath's Wire Length Prediction Model

Donath's model is basically a hierarchical partitioning of both the circuit and the

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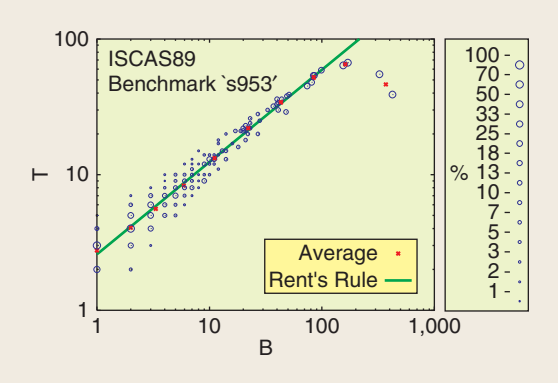

FIGURE 3: Rent's rule: number of terminals per module T versus number of gates per module B during the partitioning of a benchmark circuit (ISCAS89 benchmark `s953'). The size of the circles corresponds to the percentage of modules (on a total number of modules around an average number of gates, at equal distances in the log-log plot) that has B gates and T terminals.

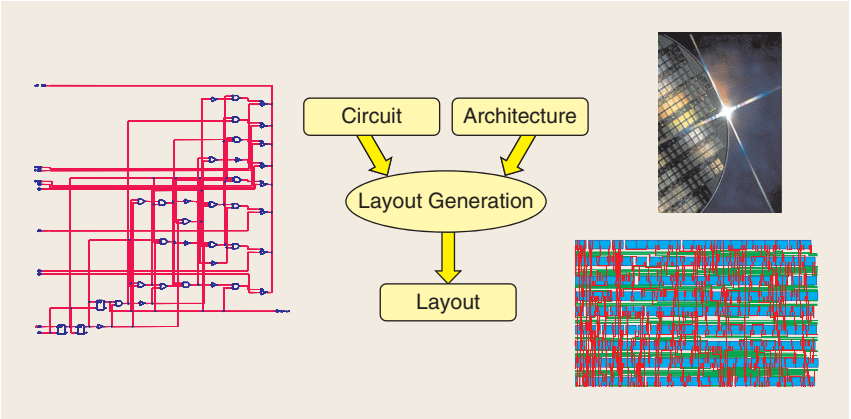

FIGURE 4: The three components of models for physical design: the circuit, the architecture and the layout generation. The combination of these models results in the (model for the) layout.

Manhattan grid architecture. The model starts with a partitioning of the circuit in four equal parts in such a way that the number of nets cut is minimized [Figure 5(a)]. At the same time, the Manhattan grid is partitioned in four equal subgrids that are the four quadrants [Figure 5(b)]. Then each of the subcircuits is mapped to a subgrid, and for each of the subcircuit/subgrid pairs the partitioning steps are repeated until each subcircuit only contains a single gate and each subgrid contains a single cell location.

This partitioning process ensures that the number of longer interconnections between large subblocks is minimized in favor of shorter interconnections between smaller blocks (inside the larger blocks). This is exactly the same partitioning as was assumed in Rent's rule. Hence we can use Rent's rule and the corresponding Rent exponent as an estimate of the complexity of the interconnection structure.

It wasn't until two other IBM employees, Landman and Russo, wrote a landmark paper in 1971 that Rent's rule was made public.

Without delving into the mathematical details (see [3] and [10] for this), it is clear to see that, in each partitioning step, Rent's rule can be used to estimate the number of terminals from the number of gates inside the subcircuit. As each terminal represents a wire going out of the module under investigation and given the fact that two terminals are needed to represent one wire that is cut (under the restriction of two-terminal nets only), one can easily deduce the number of wires crossing the module boundaries at a certain partitioning level. This number also contains the number of wires crossing the boundary from the previous partitioning in the hierarchy so one has to subtract that number to obtain the number of wires cut at each partitioning level.

The average length of a connection at a hierarchical level was assumed by Donath as the average of all possible connection lengths between each and every point from one subgrid to another one from the same partitioning level. The summation over all partitioning levels of these average lengths, weighted with the number of wires cut at that level, results in an estimate of the average wire length within the circuit. The detailed calculations can be found in [3] and [10].

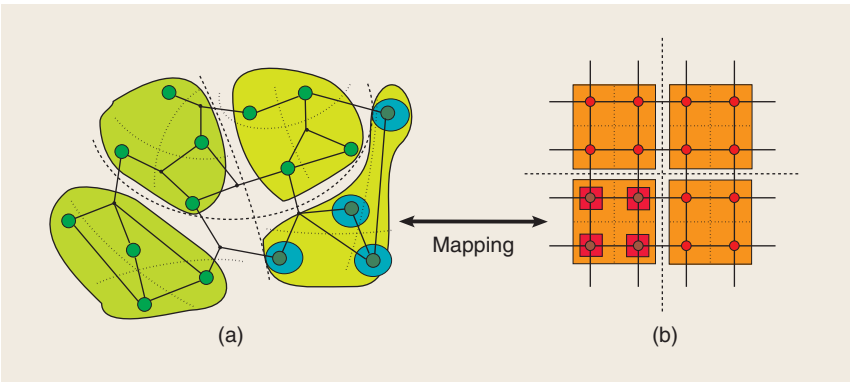

FIGURE 5: Donath's placement model: recursive partitioning of both (a) circuit and (b) Manhattan grid and mapping of circuit parts to grid parts.

Improved Wire Length Prediction Models

The placement and routing models used in Donath's prediction technique are very simple. The placement is modeled using the hierarchical partitioning model (which makes sense as partitioning is actually used in partitioning-based placers to induce optimality of the wire lengths). The routing model is very simple as well as every connection is assumed to be routed as the shortest wire between its two end points. This is a very common assumption and provides at least a lower bound on actual wire lengths. However, the simple partitioning-based placement model has its drawbacks. The main reason for this is the relatively large granularity of the partitioning steps. It is reasonable to assume wire lengths

will be longer when gates are in different partitions. However, this is not necessarily the case. Two gates placed in different modules but near their border (at both sides) can have a much shorter length than two connected gates within the same module. Donath's simple model does not take this into effect as it assumes all possible interconnections within one partitioning level as likely as any other one (see Figure 6). This leads to an overestimation of the average wire length in Donath's model by a factor of two approximately, as has been noted by several authors in the 1980s and 1990s (an evaluation can be found in [9] and [10]).

In my own Ph.D. research work [7], I found a way to remedy this discrepancy between the model and actual measurements by noting that an optimal placement (whether partitioning based or not) will prefer shorter wires over longer ones and will hence place gates in two modules of the same partitioning level preferably near the border of the modules. This has been represented in Figure 7 by a darker shade for more likely gate positions. We thus need a probability distribution for the placement of source and destination cells for all wires within a hierarchical level.

In [6] and [7], I deduced a probability distribution based on the overall wire length distribution found by Donath and statistical arguments that the local distributions should follow the same trends. It was very surprising to see that the exact same result was found around the same time by Jeff Davis at Georgia Tech [2] using a very different approach and another interpretation of Rent's rule. It took until 1999 before I actually found out through careful analysis [1] that our results were essentially the same. It was undoubtedly this improved understanding of Rent's rule and its effects on wire length estimations that reignited research on this fundamental rule of scaling, giving us a way of measuring the complexity of the interconnection structure of circuits.

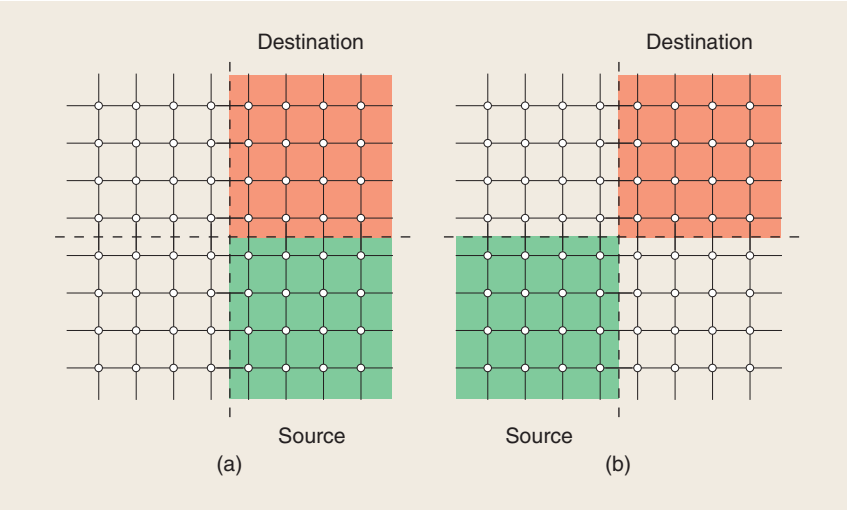

FIGURE 6: Donath's placement model: the average length on a hierarchical level is estimated by assuming that source and destination cells are uniformly distributed over the grid cells within the partition. We distinguish (a) adjacent combinations and (b) diagonal combinations.

Rent's rule, first formulated in the 1960s, is not nearly as well known as Moore's law but it is of a much more fundamental nature.

New System-Level Interconnection Research

Although Rent's rule had been known since the early 1970s, not much work (research at universities or development at companies) was based on it during the following 30 years—not even after Donath presented his very interesting application of Rent's rule in a priori wire length predictions. Of course, the rule was mentioned in a few papers and there were some individual

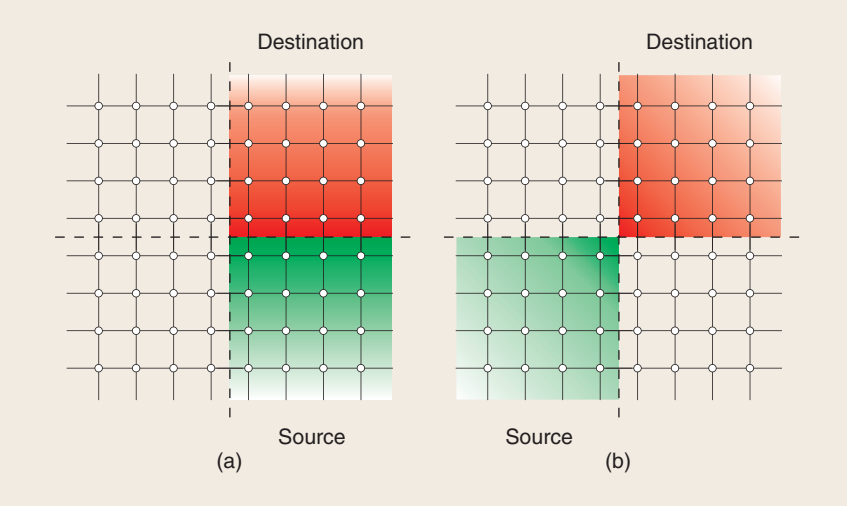

FIGURE 7: Placement of source and destination cells according to a probability distribution (darker regions have higher probability) for (a) adjacent and (b) diagonal combinations.

researchers who actually used it, but we can hardly speak of a widespread proliferation of the rule at that time. This changed, however, with the first System Level Interconnect Prediction Workshop (SLIP) in 1999 (http://www.SLIPonline.org). This workshop started with a clear focus on Rentian interconnection models (the first keynote speaker was Wilm Donath) and gradually became a breeding ground for research on the boundary between physical interconnect modeling and interconnect technology, the impact of interconnects on CAD, and architectural interconnect issues.

Historical Note

The idea of SLIP came out of frustration about the fact that my own research on Rent-based interconnection models always ended up at the strangest sessions at conferences: it was deemed interesting (and so was accepted) but was the only work of its kind. At the same time, there was a clear need for more interconnect-related research as the dominance of wire delays over gate delays began to show up in real designs. When I first presented the idea of a new workshop to Andrew Kahng (who was then a professor at UCLA), I meant it to be a workshop primarily on Rent's rule-based research. Kahng rightfully thought the scope should be broader than that and came up with the name SLIP. But Rent's rule has played a major role in the workshop ever since.

The presentation of Rent-related work and a tutorial on Rent's rule at SLIP in 1999 seem to have ignited new research programs at several universities worldwide. It is impossible to list all the recent applications of Rent's rule, but in "Recent Work Based on Rent's Rule" I briefly list some of the areas of study connected with it, with an indication of important contributors and the year they published their work at SLIP or in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (*VLSI*), where several special issues

RECENT WORK BASED ON RENT'S RULE

- The interpretation and derivation/measurement of Rent's rule: Stroobandt, University of Gent, SLIP 1999/SLIP 2001/SLIP 2003; Davis, Georgia Tech, *IEEE Transactions on Electron Devices,* 1998; Donath, IBM, SLIP 1999; Christie, University of Delaware, SLIP 1999
- Improvements/validation of interconnection length models: Christie, University of Delaware, SLIP 2000/SLIP 2002; Najm, Toronto, SLIP 2000/SLIP 2003; Stroobandt/Dambre, University of Gent, SLIP 1999/SLIP 2000/SLIP 2001/SLIP 2002; Davis, Georgia Tech, SLIP 2000/SLIP 2003/SLIP 2006; Sarrafzadeh, Northwestern University, SLIP 2001; Otten, TU Delft, SLIP 2001; Cheng, UCSD, SLIP 2001/SLIP 2003; Bennebroek, Philips Research, SLIP 2003; Bhatia, University of Texas, Dallas, SLIP 2003; Zarkesh-Ha, LSI Logic, SLIP 2004; Chrzanowska-Jeske, Portland State University, SLIP 2004; Lanzerotti, IBM, SLIP 2005/SLIP 2007; Amakawa, Tokyo Institute of Technology, SLIP 2007; Behjat, University of Calgary, SLIP 2009
- Generation of synthetic benchmark circuits: Stroobandt, University of Gent, *IEEE Transactions on Computer-Aided Design,* vol. 19, no. 9, 2000
- Wire length models for three-dimensional systems: Rahman, MIT, SLIP 1999/SLIP 2001; Saraswat, Stanford, SLIP 2000; Davis, Georgia Tech, SLIP 2000; Chandrakasan, MIT, SLIP 2005; Christie, University of Delaware, SLIP 2005
- Timing estimations: Christie, University of Delaware, SLIP 2002; Amakawa, Tokyo Institute of Technology, SLIP 2005; Brown, Altera Toronto, SLIP 2006; Luk, Imperial College London, SLIP 2008
- Routing/routability/congestion optimization: Chong, University of California, Berkeley, SLIP 1999; Stroobandt/Kahng, UCLA, SLIP 2000; Scheffer, Cadence, SLIP 2000; He, University of Wisconsin, SLIP 2001; Kahng/Stroobandt, UCLA, *IEEE Transactions on Computer-Aided Design,* vol. 20, no. 5, 2001; Sapatnekar, University of Minnesota, SLIP 2002; Teig, Simplex Solutions, SLIP 2002; Becer/Blaauw, Motorola/University of Michigan/University of Illinois, SLIP 2002; Christie, University of Delaware, SLIP 2002; Kravets/Kudva, IBM, SLIP 2003; Karypis University of Minnesota, SLIP 2003; Kahng, UCSD, SLIP 2003; Groeneveld, TU Eindhoven, SLIP 2005; Sarrafzadeh, UCLA, SLIP 2007
- Placement optimization: Cong, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 9, no 6, 2001; Christie, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 9, no. 6, 2001; Marek-Sadowska/Xilinx, UCSB, SLIP 2001/SLIP 2002/SLIP 2003
- Floorplanning: Sarrafzadeh, Northwestern University, SLIP 1999
- Manufacturability and yield: Christie, University of Delaware, SLIP 2001; Zarkesh-Ha, LSI Logic, SLIP 2003; Zarkesh-Ha, University of New Mexico, SLIP 2007
- Rent-based system/architectural analysis and technology extrapolations: Sylvester, University of California, Berkeley, SLIP 1999; Kahng, UCLA, DAC 2000; Rose, Rensselaer Polytechnic Institute, SLIP 2001; Hutton, Altera, SLIP 2001/SLIP 2003; DeHon, CalTech, SLIP 2001; Maex, IMEC, SLIP 2002/SLIP 2004; Cheng, UCSD, SLIP 2003; Bergamaschi, IBM, SLIP 2004; Kumar, Cornell University, SLIP 2004; Greene, Actel, SLIP 2006
- On-chip power distribution/optimization: Friedman, University of Rochester, SLIP 2002; Nassif, SLIP 2002; Kolodny, Intel, SLIP 2004; Saraswat, Stanford, SLIP 2004; Kahng/Sylvester, UCSD/University of Michigan, SLIP 2004; Schmit, CMU, SLIP 2004
- Networking and NoCs: Muddu, Sanera Systems, SLIP 2002; Verbauwhede, UCLA, SLIP 2002; Tenhunen, KTH Sweden, SLIP 2003; Davis, Georgia Tech, SLIP 2004; Burleson, University of Massachussetts, SLIP 2004; Kolodny, Technion-Israel Institute of Technology, SLIP 2007; De Micheli, Ecole Polytechnique Federale de Lausanne, SLIP 2007; Smit, University of Twente, SLIP 2008; Heirman/Dambre/Stroobandt, University of Gent, SLIP 2008; Reda, Brown University, SLIP 2009
- Optical systems: O'Connor, Ecole Centrale de Lyon, SLIP 2004; Heirman/Dambre/Stroobandt, University of Gent, SLIP 2005/SLIP 2006

Rent's rule has found its way mainly to a priori interconnect length estimation and related extrapolations.

on SLIP research have been published. Many more research papers addressing Rent's rule can be found on the Web.

Apart from the papers presented at SLIP, there have been a number of special issues of journals dedicated to this topic: *VLSI* published one in 2002 (vol. 10, no. 2), one in 2003 (vol. 11, no. 1), and one in 2007 (vol. 15, no. 8), and *Integration, the VLSI Journal* published a special SLIP issue in 2007 (vol. 40, issue 4).

As can be seen from "Recent Work Based on Rent's Rule," several companies have begun discussing and using Rent's rule—notably IBM but also Actel, Altera, Cadence, Intel, Sanera Systems, Simplex Solutions, and Xilinx.

Historical Note

Before SLIP, I had read a few papers by Phillip Christie (then at the University of Delaware), but I had never met him. He was, at the time, the one person in the world who had written a series of papers related to Rent's rule. He came to SLIP in 1999 and gave a presentation there, but what I remember most is our hours-long discussion on Rent's rule in the local Irish pub one Saturday evening. Our interpretations of Rent's rule were very different yet so alike. The next morning, Phillip asked me for 15 minutes of the workshop program time to explain to the audience the unifying interpretation he had come up with overnight. The workshop atmosphere allowed for such an intervention and laid the basis for the highly cited paper we wrote together afterwards [1].

Future Issues in Interconnect Research

As stated earlier, Rent's rule has found its way mainly to a priori interconnect length estimation and related extrapolations. As wire lengths increasingly dominate circuit delays as well as power and area usage, the importance of interconnects will surely endure. One can question whether Rent's rule will still be sufficient as a basis of the predictions, since the accuracy of Rentian predictions may not be high enough. If one needs accurate estimates, one needs to revert to simulation and actual (albeit fast) synthesis methods. Using actual synthesis as the basis for estimation may not be as problematic as it used to be, and so it will probably gain in importance with respect to Rent's rule. However, as hardware design moves up to higher hierarchy levels (e.g., with electronic system-level design), the early steps of architecture exploration before any synthesis has been done will again require very fast and simple estimates to weed out inferior solutions and keep only the promising ones. In this domain, a simple estimate based on Rent's rule, even if it is not very accurate, provides the only plausible way to obtain estimates quickly. It is difficult to predict what lies ahead, but I believe Rent's rule has a bright future as design moves to higher levels of abstraction. But even if we risk forgetting about its power, the rule fundamentally governs our designs. We will be forced to listen to the prompter and take it into account.

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About the Author

Dirk Stroobandt obtained the Ph.D. degree in electrotechnical engineering in 1998 from Ghent University, Belgium. Since 2002, he has been a professor at Ghent University, affiliated with the Department of Electronics and Information Systems (ELIS). He was the first recipient of the ACM/SIGDA Outstanding Doctoral Thesis Award in Design Automation (1999) and also received the Alcatel Bell Prize in 2002 for his work on structural and behavioral aspects of short optical interconnects in electronic systems. He was a visiting researcher at the laboratory of Fadi J. Kurdahi at the University of California at Irvine (1997) and postdoctoral researcher under Andrew B. Kahng at UCLA (1999–2000). Stroobandt has coorganized the International Workshop on System-Level Interconnect Prediction (SLIP) since 1999. He has been the guest editor for two special issues of *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* dedicated to system-level interconnect prediction and a special issue of *Integration, the VLSI Journal* on SLIP for integration.

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