# Calibration of DAC mismatch errors in $\Sigma\Delta$ ADC's based on a sine wave measurement.

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[1] M. De Bock, X. Xing, L. Weyten, G. Gielen, and P. Rombouts, "Calibration of DAC Mismatch Errors in Sigma Delta ADCs Based on a Sine-Wave Measurement," *IEEE Trans. Circuits Syst.-I: Regular Papers*, vol. 60, no. 9, pp. 567–571, Sep. 2013.

# Calibration of DAC mismatch errors in $\Sigma\Delta$ ADC's based on a sine wave measurement.

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***Abstract*—We present an off-line calibration procedure to correct the non-linearity due to DAC mismatch in multi-bit $\Sigma\Delta$-modulation A/D-converters. The calibration uses a single measurement on a sinusoidal input signal, from which the DAC-errors can be estimated. The main quality of the calibration method is that it can be implemented completely in the digital domain (or in software) and does not intervene in any way in the analog modulator circuit. This way, the technique is a powerful tool for verifying and debugging designs. Due to the simplicity of the method it may also be a viable approach for factory calibration.**

## I. Introduction

It is well known that the linearity of a multi-bit $\Sigma\Delta$ modulator is limited by the linearity of its feedback D/A-converter (DAC). This way, some kind of linearization scheme is needed if a linearity beyond the intrinsic device matching is required. For this purpose, dynamic element matching techniques, which achieve spectral shaping of the DAC errors, have been successfully exploited [1–9]. However, at low oversampling ratios, such dynamic element matching techniques become inefficient and calibration techniques come into the picture [10–14].

In this paper we present such a calibration technique. It is based on storing a digital estimation of the DAC errors in a look-up-table (LUT), which is used during the normal conversion to correct the DAC-errors. Obviously, the performance of such a LUT-based scheme depends on the accuracy of the digital estimation of the DAC-errors. Therefore, the actual calibration, i.e. the process of obtaining the calibration data is essential. Moreover, the technique should not increase the complexity of the rest of the A/D-converter circuitry. In this manuscript we present such a calibration scheme that minimally intervenes with the A/D-conversion. It uses a single calibration measurement on a spectrally pure sinusoidal input signal, which is performed in an off-line calibration cycle. From this measurement the calibration data are calculated which are stored in the LUT.

Alternative calibration techniques [10–14], (be it on-line or off-line) invariably add some circuitry in the modulator's feedback loop (typically additionally gates for multiplexing logic). This puts stress on the timing budget. Compared to those techniques, the presented approach has the main distinct feature that the calibration is completely outside the $\Sigma\Delta$ control loop and does not require any modification of the actual core A/D-converter circuit. As a result it has the advantage that it does not add to the timing budget of the overall feedback path, and hence is readily applicable to the highest speed converters. As will be shown, the algorithm is simple and may be implemented in production testing, without significantly adding to the testing time. This way, it is a potential candidate for factory-level calibration. But probably the most important application is in debuging prototypes and monitoring device matching.

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Maarten De Bock, Ludo Weyten and Pieter Rombouts are with the Department Electronics and information Systems, Ghent University, Ghent, Belgium. Xinpeng Xing and Georges Gielen are with MICAS-ESAT Kuleuven, Leuven, Belgium.



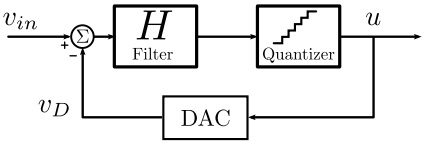


Figure 1. Block diagram of a typical $\Sigma\Delta$-modulation A/D-converter

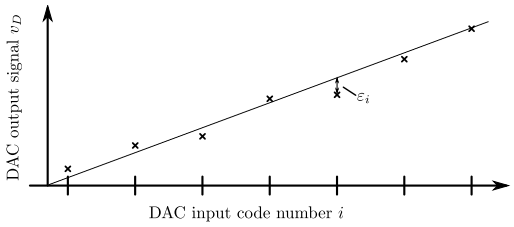


Figure 2. Typical feedback DAC input output relationship.

The rest of this paper is organized as follows: section II reviews DAC non-linearity in multibit $\Sigma\Delta$ modulators, section III covers look-up-table based digital calibration. In section IV we describe the algorithm to estimate the DAC errors from a sinusoidal measurement. Section V discusses application considerations. Section VI describes the application of the approach on an actual silicon ADC circuit and finally we present our conclusions in section VII.

## II. DAC-non-linearity in $\Sigma\Delta$-modulators

Fig. 1 shows a $\Sigma\Delta$-modulator with input signal $v_{in}$. It consists of a multi-bit quantizer embedded in a control loop with loopfilter $H$. The digital output signal $u$ of the quantizer is fed back by means of a digital-to-analog converter (DAC).

In most practical implementations the feedback DAC will not be perfectly linear and will have an input-output behavior as shown in Fig. 2. To quantify this, we introduce the DAC-level selection signals $x_i$, which are defined as[1]:

$$x_i(n) = \begin{cases} +1, & \text{if the } i\text{th code is selected} \\ 0, & \text{else} \end{cases}$$

This way, there are $N$ selection signals for an $N$-level DAC and there is always exactly 1 selection signal high at each time step. Then we can write the DAC-output signal sequence $v_D$ as:

$$v_D(n) = \sum_{i=1}^{N} x_i(n) \cdot D_i, \tag{1}$$

[1] In this work lowercase letters are used for time-domain representation of signals, whereas uppercase letters are used for more abstract transformed (Z-domain or frequency domain) representations.

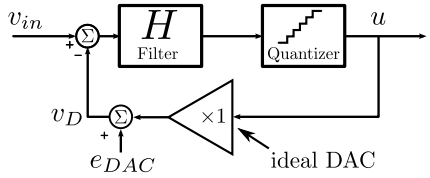


Figure 3. Equivalent diagram of a typical ΣΔ-modulation A/D-converter with a non-linear DAC.

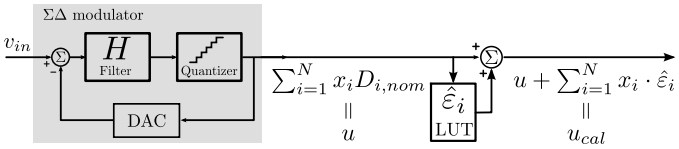


Figure 4. Normal operation of LUT-based calibration.

where the $D_i$ values correspond to the actual DAC-levels. The DAC-non-linearity manifests itself in the sense that the actual DAC-levels $D_i$ deviate from their nominal values $D_{i,nom}$ by a mismatch error $\varepsilon_i$ (see Fig. 2). As a result the DAC-output signal $v_D$ will exhibit an error $e_{DAC}$ and can be written as:

$$v_D(n) = \sum_{i=1}^{N} x_i(n) \cdot (D_{i,nom} + \varepsilon_i) = u(n) + \underbrace{\sum_{i=1}^{N} x_i(n) \cdot \varepsilon_i}_{\text{DAC error } e_{DAC}} \quad (2)$$

Here, we have defined the uncalibrated output signal $u(n)$ as:

$$u(n) = \sum_{i=1}^{N} x_i(n) \cdot D_{i,nom}$$

With this definition of the output signal $u(n)$, the DAC has unity gain (see Fig. 3). Now we can solve this system by inspection:

$$U = STF \cdot V_{in} + NTF \cdot Q - STF \cdot E_{DAC} \quad (3)$$

Here the signal transfer function (STF), the noise transfer function (NTF) and the quantization noise ($Q$) are defined as usually. Since the signal transfer should have a gain close to unity in the signal band, we find that the non-linearity error $E_{DAC}$ of the DAC is found directly in the output signal.

## III. LUT-based calibration

The non-linearity of the DAC can be counteracted by digital calibration. Here, a digital estimation $\hat{\varepsilon}_i$ of each of the $N$ mismatch errors $\hat{\varepsilon}_i$ is stored in the look-up-table. This look-up-table is quite small because the number of DAC-levels $N$ is relatively small in a ΣΔ modulator (typically of the order of 8 to 32). Then, during normal operation, the calibrated output signal $u_{cal}(n)$ is obtained by retrieving a correction term $\hat{e}_{DAC}$ from the LUT, as shown in Fig. 4:

$$u_{cal}(n) = u(n) + \underbrace{\sum_{i=1}^{N} x_i(n) \cdot \hat{\varepsilon}_i}_{\text{estimated DAC error } \hat{e}_{DAC}} \quad (4)$$

Here, the digital correction term $\hat{e}_{DAC}$ can be interpreted as a digital approximation of the actual DAC error $e_{DAC}$. An important advantage of this scheme is that the correction is completely outside the ΣΔ loop. There is one minor disadvantage: i.e. the digital representation of the overall calibrated output $u_{cal}$ now consists of significantly more bits. This way, the complexity of the decimation filter that follows, is increased. But in today's ultra deep submicron technologies, this is not a major concern.

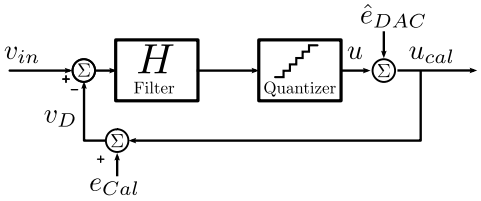


Figure 5. Equivalent diagram showing the error sources in a ΣΔ-modulation A/D-converter with a LUT-based digital calibration.

The effectiveness of the calibration will depend on how accurately the estimated DAC-error $\hat{e}_{DAC}$ corresponds to the actual DAC error $e_{DAC}$. To quantify this, we can obtain the equivalent system-level diagram of Fig. 5. Here, we have introduced the calibration error $e_{cal}$, which equals the difference between the actual DAC error $e_{DAC}$ and its digital estimation $\hat{e}_{DAC}$ :

$$e_{cal} = e_{DAC} - \hat{e}_{DAC} = \sum_{i=1}^{N} x_i(n) \cdot (\varepsilon_i - \hat{\varepsilon}_i)$$

This allows to obtain an exact (Z-domain) expression of the calibrated output signal:

$$U_{cal} = STF \cdot V_{in} + NTF \cdot (Q + \hat{E}_{DAC}) - STF \cdot E_{cal} \quad (5)$$

If the digital estimation matches the error well, the calibration error $e_{cal}$ will be negligible and the effect of the DAC-errors will be nearly zero, because it is filtered by the modulator's NTF. However if the calibration error is not negligible, it will directly affect the accuracy of the calibration scheme.

## IV. Estimating the mismatch errors

The estimation of the mismatch errors, occurs in an off-line procedure prior to the normal operation. Here, a spectrally pure sinusoidal input signal $s(t)$ is applied to the ΣΔ ADC. The frequency of the calibration sine wave should be low, because the sine's harmonics have to be within the ADC's signal band. The amplitude should be high enough to use all DAC levels.

Let us now consider the digital (decimation) low-pass filter that is needed to remove the modulator's quantization noise. This filter has a transfer function $L(z)$ and an impulse response $l(n)$. When we apply this low-pass filter $L(z)$ to the digital output signal $u$, we obtain the filtered output signal $u_{LP}(n)$:

$$u_{LP}(n) = l(n) \star u(n),$$

where the $\star$ operator stands for the convolution. The filtered output signal $u_{LP}$ then consists of the undistorted (low-pass filtered) calibration signal $s(n)$, the filtered DAC-error signal $e_{DAC,LP}(n)$ which is due to the DAC-errors and the noise signal $e_{noise,LP}(n)$. This noise signal corresponds to all the system noise that is not related to the DAC-signals, and contains the shaped quantization noise [the term $NTF \cdot Q$ in Eq. (3)], but also potential additive circuit noise:

$$u_{LP}(n) = s_{LP}(n) + e_{noise,LP}(n) + e_{DAC,LP}(n)$$

Applying the definition of the DAC-error in Eq. (2):

$$u_{LP}(n) = s_{LP}(n) + e_{noise,LP}(n) + \sum_{i=1}^{N} l(n) \star x_i(n) \cdot \varepsilon_i$$

Now, we introduce the filtered selection signals $x_{i,LP}(n) = l(n) \star x_i$ and the residue signal $r(n)$ which equals:

$$r(n) = u_{LP}(n) - s_{LP}(n)$$

To calculate this residue signal we need to know the filtered calibration signal $s_{LP}(n)$, which corresponds to the analog calibration signal. In principle this is not known, but we know that it is a sinusoidal signal. This way, this signal can be obtained by curve-fitting a sine wave to the uncalibrated filtered output signal $u_{LP}$. Very efficient algorithms for accurate sine-wave fitting such as IEEE-STD-1057 are well known [15, 16] and may already be deployed in the circuit evaluation setup. The residue signal $r(n)$ is then evaluated as the curve fit error and hence can be considered to be known. Then we can write:

$$r(n) = e_{noise,LP}(n) + \sum_{i=1}^{N} x_{i,LP}(n) \cdot \varepsilon_i$$

From this equation, we observe that we can obtain an estimation $\hat{\varepsilon}_i$ of the DAC-errors, by performing a least mean square (LMS) minimization of $r(n) - \sum_{i=1}^{N} x_{i,LP}(n) \cdot \hat{\varepsilon}_i$. Indeed:

$$E\left\{\left(r(n) - \sum_{i=1}^{N} x_{i,LP}(n) \cdot \hat{\varepsilon}_i\right)^2\right\} =$$

$$\underbrace{E\left\{e^2_{noise,LP}(n)\right\}}_{\text{noise variance}} + \underbrace{E\left\{\left(\sum_{i=1}^{N} x_{i,LP}(n) \cdot (\varepsilon_i - \hat{\varepsilon}_i)\right)^2\right\}}_{\text{calibration error variance}} \quad (6)$$

The calibration error variance cannot be negative. Moreover, it is observed that it becomes zero when the estimated DAC-errors $\hat{\varepsilon}_i$ are equal to the actual DAC-errors $\varepsilon_i$. This implies that the correct estimation $\hat{\varepsilon}_i$ of the DAC-errors corresponds to the LMS optimization. In practice, the expectation value of Eq. (6) must be approximated as the mean value over a finite data set of $L$ data points. This way, we obtain the estimated DAC errors $\hat{\varepsilon}_i$ by minimizing:

$$\sum_{n=1}^{L}\left(r(n) - \sum_{i=1}^{N} x_{i,LP}(n)\hat{\varepsilon}_i\right)^2$$

with regard to $\hat{\varepsilon}_i$. Or:

$$\frac{\partial}{\partial \hat{\varepsilon}_j}\sum_{n=1}^{L}\left(r(n) - \sum_{i=1}^{N} x_{i,LP}(n)\hat{\varepsilon}_i\right)^2 = 0, \forall j$$

This yields a system of $N$ equations ($j = 1..N$) for the $N$ unknown DAC-errors $\hat{\varepsilon}_i$:

$$\sum_{n=1}^{L} r(n)x_{j,LP}(n) = \sum_{n=1}^{L}\sum_{i=1}^{N} x_{j,LP}(n)x_{i,LP}(n)\hat{\varepsilon}_i, \ \forall j \quad (7)$$

All the coefficients in this system of equations can easily be evaluated, and solving this system is trivial. The corresponding setup for the calibration is shown in Fig. 6.

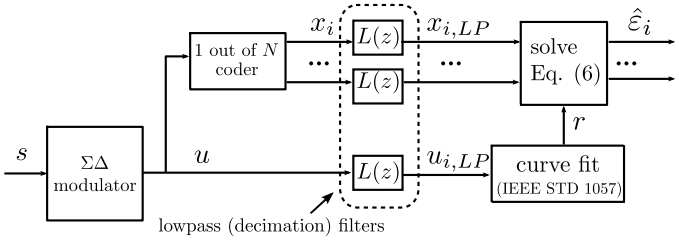


Figure 6. Calibration setup.

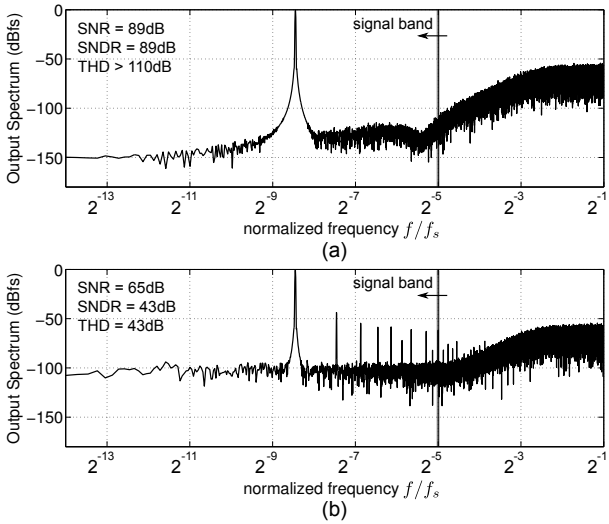


Figure 7. Simulated output spectrum of the uncalibrated modulator: (a) without and (b) with DAC-mismatch.

## V. Applications

### A. Prototype debug and evaluation

A first important application of the proposed technique is in the debugging and evaluation of prototype ΣΔ A/D converters. Indeed, sine wave tests are always an essential part of any prototype evaluation. Moreover, these tests are usually performed in a low-noise laboratory environment. This way, the proposed technique can be added to the arsenal of evaluation techniques. To illustrate how the technique behaves in such a situation, we have built a behavioral model of a 3rd order 5-bit ΣΔ ADC designed according to [17] with $h_\infty = 2.8$ for an $OSR = 16$. We modeled a unit-element DAC where the 31 unit-elements were assigned mismatch errors with a $\sigma$ of 3% (intentionally relatively large for the purpose of illustration).

Fig. 7 shows the simulated spectra of the test modulator for a sinusoidal input signal with an input amplitude of -1dBfs. This amplitude is chosen as large as possible, while still avoiding modulator overloading. 64K data points were used for the simulation, corresponding to $L = 4$K baseband data points. The figure shows the ideal case (without mismatch) and the real case (with mismatch). It is clear that the mismatch ruins the performance completely.

Fig. 8 shows the simulated spectra of the test modulator for the case with mismatch but with LUT-based calibration. Here the same simulation result as Fig. 7(b) was used, but now corrected with the LUT-based calibration described above. Two cases were considered. First the case where the simulated signal

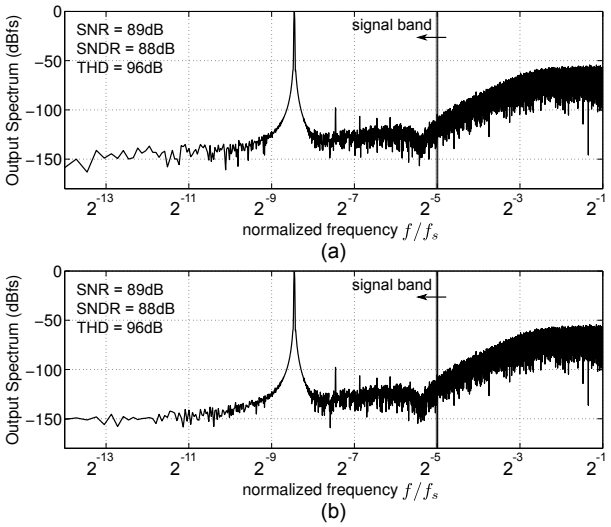


Figure 8. Simulated output spectrum of the modulator with mismatch and with calibration for the case where the look-up-table uses (a) the estimated mismatch errors $\hat{\varepsilon}_i$ and (b) the exact value $\varepsilon_i$ of the mismatch errors .

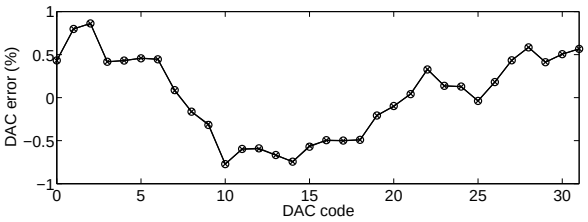


Figure 9. Mismatch errors (marked with ○) and estimated mismatch errors (marked with ×).

sequence was used to obtain the estimated DAC-errors $\hat{\varepsilon}_i$. This result is shown in Fig. 8(a). Here the SNDR is nearly identical to the case of the ideal modulator (88 dB vs. 89 dB), but some harmonic spurs are visible, corresponding to a THD of 96dB. However, this is not due to calibration errors. To illustrate this, Fig. 8(b) shows the result where the LUT uses the exact values $\varepsilon_i$ of the DAC-mismatch. Here the calibration error is strictly equal to 0, but this case also exhibits the spurs. Upon investigation it turns out that these spurs originate from the shaped mismatch error i.e. the term $NTF \cdot \hat{E}_{DAC}$ in Eq. (5). This term is greatly suppressed, and nearly has no effect on the SNDR, but it is visible in an FFT-result.

The calibration result is also illustrated in Fig. 9 which shows the actual mismatch errors $\varepsilon_i$ and the estimated DAC-errors $\hat{\varepsilon}_i$. Here we can see that the estimation matches the actual value nearly perfectly.

### *B. Factory level calibration*

The calibration flow may also be sufficiently efficient to be used for factory-level calibration. Indeed, most of the blocks that are needed, are anyway available in some form in the factory testing of ADC's (e.g. the sine wave stimulation test and curve fit set up). However, the situation of a factory-level calibration is different in the sense that the speed is important. This way, it is desirable that the number of samples $L$ that are needed to perform a calibration measurement is not too high. In addition to this, also the environment is more hostile than a typical laboratory environment and may exhibit higher interference and noise levels. To study this, we performed Monte Carlo simulations where we generated 100 sets of DAC-mismatch (with $\sigma$ of $3\%$). Then we obtained the error estimations $\hat{\varepsilon}_i$ from different calibration cycles where we intentionally added noise to the calibration sine wave, corresponding to a noisy environment during chip testing. In addition to the ideal case (with an SNR of 89dB), the cases of a baseband SNR during calibration of [40, 50, 60, 70, 80] were considered. Then these estimations, were used to calibrate a normally operating ADC (which should be able to reach an SNDR=88dB). The corresponding SNDR was evaluated and this experiment was repeated for increasing numbers of data points used in the calibration cycle. The results are summarized in Fig. 10, which shows the SNDR of the calibrated ADC vs. the number $L$ of baseband data points used in the calibration. The errorbars in the plot correspond to the 10% and 90% percentiles. The plot indicates that when the calibration is performed with a good SNR (of at least 80dB), about 1K of data-points is sufficient to obtain nearly perfect calibration results. However, when the noise during the calibration cycle is higher, more data-points are needed: e.g. 4K for a calibration SNR of 70dB and 64K for a calibration SNR of 60dB. With even lower SNR's the technique still works, but here the accuracy of the calibration improves only by roughly 3 dB for each doubling of $L$, which indicates a typical $1/\sqrt{L}$ averaging behavior. This way, it appears that when the calibration SNR is low, the amount of data points that are needed to obtain perfect calibration results, rapidly increases and becomes unpractical.

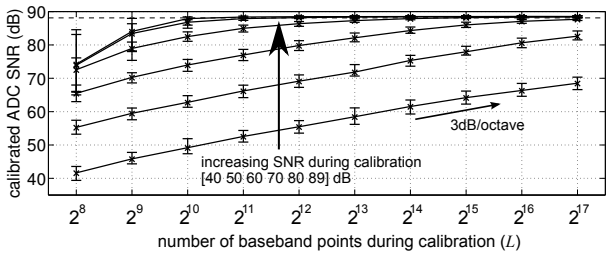


Figure 10. Effect of the SNR and the number of data-points during the calibration cycle on the obtainable SNDR after calibration.

## VI. Experimental results

In the previous section, the approach was applied to simulated $\Sigma\Delta$ ADCs, where static DAC-errors were the only error occuring in the ADC. In addition to this, the technique was also applied for calibration of actual prototype integrated circuits [18, 19]. Here, other parasitic effects (e.g. opamp slewing, dynamic DAC errors, ...) can occur as well. To illustrate the performance of the technique in such a real life situation, we consider the 960MSample/s continuous time $\Sigma\Delta$ ADC of [18]. Here the quantizer resolution was 5-bits and the OSR was 12, which corresponds to a 40 MHz bandwidth. This circuit was designed such that the circuit noise level would allow 12-bit performance. The full circuit details are discussed in [18]. The measured spectra for a low-frequency input signal are shown in Fig. 11, both for the case without as well as with calibration. In the uncalibrated case, the SNDR is limited by distortion

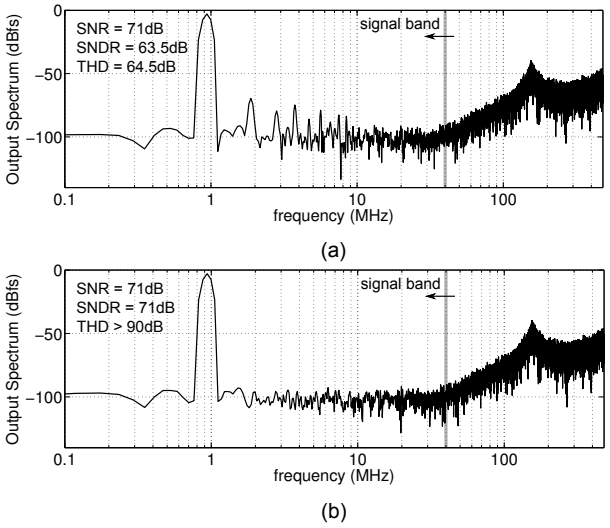


Figure 11. Measured output spectrum of a 960MSamples/s $\Sigma\Delta$ modulator with 40 MHz bandwidth for the case of a low input frequency (a) without calibration and (b) with calibration.

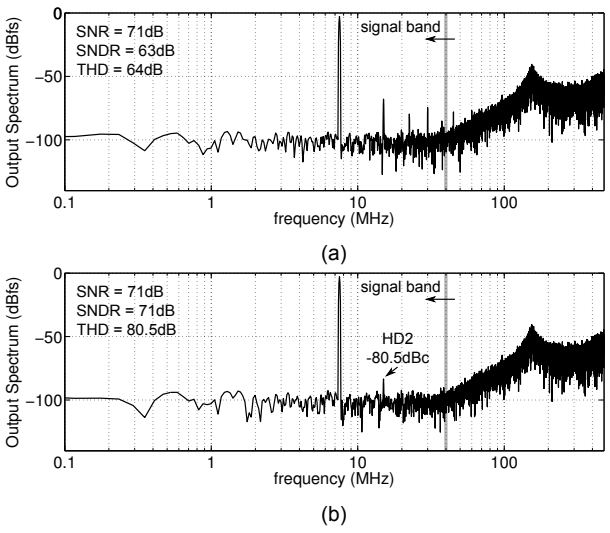


Figure 12. Measured output spectrum of a 960MSamples/s $\Sigma\Delta$ modulator with 40 MHz bandwidth for the case of a high input frequency (a) without calibration and (b) with calibration.

and is only 63 dB (about 10-bit performance). The same measurement was used to calculate the correction terms and then to calibrate the converter (according to the method described in sections III-IV). The corresponding results are also shown in the figure, where the distortion is entirely eliminated and a peak SNDR of 71 dB is observed now.

The case of a higher input frequency of 7.5 MHz (which still has its first 5 harmonics in the signal band), is shown in Fig. 12. Here the calibration coefficients that were obtained previously from the low-frequency measurement were used to calibrate the DAC. The figure shows that the calibration nearly eliminates the distortion for this case as well, although, in this case, a 2nd harmonic distortion component of -81dBc is visible. Since the DAC-calibration is not able to eliminate this distortion, this indicates that there is another source of distortion in this circuit. However, in this case, this distortion component does not limit the SNDR. Experiments on other prototypes with very different modulator designs e.g. [19] confirm that the calibration technique behaves well in typical real-life situations, and eliminates distortion due to static DAC-errors.

## VII. Conclusion

An off-line calibration method to correct static DAC-errors in $\Sigma\Delta$-modulation ADCs is presented. This technique uses a spectrally pure sinusoidal input signal and calculates the DAC errors from the resulting digital output signal. The straightforward implementation gives only little overhead to the digital post processing of the modulator output. This makes this method tailored for verifying and debugging designs and potentially also for factory calibration.

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