Athermal arrayed waveguide gratings in silicon-on-insulator by overlaying a polymer cladding on narrowed arrayed waveguides

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Athermal arrayed waveguide gratings (AWGs) in silicon-on-insulator (SOI) are experimentally demonstrated for the first time to our knowledge. By using narrowed arrayed waveguides, and then overlaying a polymer layer, the wavelength temperature dependence of the AWGs is successfully reduced to −1.5 pm/°C, which is more than 1 order of magnitude less than that of normal SOI AWGs. The athermal behavior of the AWGs is obtained with little degradation of their performance. For the central channel, the cross talk is less than −15 dB and the insertion loss is around 2.6 dB. Good characteristics can be maintained with temperatures up to 75 °C. The total size of the device is 350 μm × 250 μm.

1. Introduction

In recent years, silicon photonics is receiving more and more attention as it represents an ideal platform for realizing compact and multifunctional photonic integrated circuits. In combination with industrial waferscale complementary metal–oxide semiconductor (CMOS) fabrication technology, the silicon-on-insulator (SOI) photonic technology also has the potential for mass production, which would thus greatly reduce the device cost. As a key passive photonic component, arrayed waveguide gratings (AWGs) are of great use in all-optical networks as (de-)multiplexers and wavelength routers, and as part of more complex photonic switches, sources or receivers. Although AWGs have conventionally been fabricated in low-index-contrast glass technology like silica, the desire for high-density photonic integration has led to an increasing interest in ultrasmall AWGs based on the silicon photonic wire waveguides with high-index contrast [1–3].

However, the large thermo-optic (TO) coefficient of silicon ($dn/dT = 1.8 \times 10^{-4}$/°C) makes these SOI-based AWGs strongly temperature dependent, such that an external heater or cooler has to be employed to stabilize the chip temperature. These elements would not only take extra space but also consume higher power, counteracting the benefits brought by SOI technology. Athermal glass-based or InP-based AWGs have been demonstrated for several years, where the methods adopted for removing the temperature dependence include cutting silica AWGs at one of their slab waveguides into two pieces

and then connecting them by a metal plate [4], insertion of a resin-filled groove into the arrayed waveguides or one slab waveguide [5–7], and so on [8–9]. However, there has still not yet been an experimental demonstration of athermal SOI AWGs so far. The methods mentioned above cannot simply be applied to SOI AWGs, mainly due to their extremely small size and layout complication. Furthermore, the optical path length differences need to be strictly controlled between several tens of arrayed waveguides in order to obtain good characteristics for SOI AWGs. The arrayed waveguides suffer from a high sensitivity to phase noises resulting from the high-index contrast, which is even worse if modifications are to be made to them. That is the reason why the characteristics of SOI AWGs are still not comparable to those of their glass-based or InP-based counterparts. Other passive photonic components in SOI with relatively simpler structure, such as ring resonators or Mach–Zehnder interferometers, have been made athermal through a number of methods [10–14], but temperature independent AWGs have so far only been shown to be possible using simulations [15–16]. The slot waveguides proposed in [15–16] would also pose a challenge for fabrication.

In this paper we experimentally demonstrate 1 × 8 AWGs in SOI wire technology with a channel spacing of 400 GHz. By inserting narrowed waveguides into the straight arms of the arrayed waveguides, and then overlaying a polymer layer on top, the wavelength temperature dependence of the AWGs is successfully reduced to −1.5 pm/°C, which is more than 1 order of magnitude less than that of normal SOI AWGs. The proposed devices can still maintain good performances with temperature up to 75 °C. For the central channel, the cross talk is less than −15 dB and the insertion loss is around 2.6 dB, of which are the typical order for such compact SOI AWGs.

2. Concept, Design, and Fabrication

The fundamental phase relationship of an AWG can be described as

$$m\lambda_c = n_c \Delta L, \tag{1}$$

where λ_c is the central wavelength, n_c is the effective index of the arrayed waveguides, ΔL is length difference between two adjacent arrayed waveguides and m is phased array order [17]. By differentiating Eq. (1) with temperature T, the temperature dependence of the channels' wavelengths of the AWG can be obtained:

$$\frac{d\lambda_c}{dT} = \frac{\lambda_c}{n_g}\left(n_c\alpha + \frac{dn_c}{dT}\right). \tag{2}$$

Here $\alpha = (d\Delta L/dT)$ is the thermal expansion coefficient of the substrate, which is two orders of magnitude smaller than dn_c/dT value. As can be seen from the above equation, the wavelength shift of the AWGs' channels with temperature is mainly caused by the effective refractive index change of the arrayed waveguides. Thus if the arrayed waveguides can be made temperature independent, the temperature dependence of the AWGs' wavelengths can be removed.

It is well known that athermal SOI components could be made by compensating the large positive TO coefficient of silicon by using a cladding with negative TO coefficient, where polymer can be an ideal option. For the case of silicon wire waveguides, an additional problem is that for the usual waveguide dimensions and TE-like polarization, most of the light is confined to the silicon and only a fraction can penetrate into the cladding with opposite TO coefficient. To arrive at athermal components, it is therefore typically necessary to reduce the dimensions of the silicon wire to allow more light to penetrate into the polymer. Besides that, the polymer functioning as cladding for compensation should meet the requirements of high negative TO coefficient and high thermal stability. By using Eq. (2), the $d\lambda_c/dT$ behavior of the TE mode for different widths of the arrayed waveguides is calculated and the result is shown in Fig. 1(a). The effective index of the SOI waveguide is calculated using FIMMWAVE (Photon Design Ltd.). The height of 220 nm is in accordance with the value of the standard SOI wafer we use for fabrication in our group. The main parameters used are as follows: refractive index of Si, 3.4757; TO coefficient of Si, 1.8×10^{-4}/°C; refractive index of SiO_2, 1.444; TO coefficient of SiO_2, 1×10^{-5}/°C; α, 2.6×10^{-6}/°C [18]; refractive index of polymer, 1.515; TO coefficient of polymer, -2.4×10^{-4}/°C [19]. It is noted that practical SOI waveguides fabricated in a CMOS foundry exhibit a trapezoidal shape and therefore waveguides with an 80° sidewall angle have been simulated and compared to ideal rectangular waveguides [20]. The width value of the bottom edge of the trapezoidal SOI waveguides is adopted for the simulation and the following experiments. From the simulation, both kinds of SOI waveguides evolve from undercompensated to overcompensated with decreasing waveguide width. The ideal widths for these two kinds of arrayed SOI waveguides (and thus for AWGs) to be temperature independent lie around 305 nm and 340 nm for the rectangular and trapezoidal waveguides respectively. The optical modes at these two critical width values are shown in Figs. 1(b) and 1(c). Because the trapezoidal waveguide model is closer to the shape of the fabricated waveguide, it gives better agreement with experiments than the rectangular waveguide model (see Fig. 1).

On the other hand, reducing the dimensions of the silicon wire waveguides has a negative effect on the performance of the AWGs. Typically, the delay lines are broadened to reduce propagation loss and phase noise [3]. In our case, the phase noise in the waveguide arms would increase when they are narrowed, which would result in higher cross talk between channels. The insertion loss would also increase with the narrowing of these waveguides. However, from

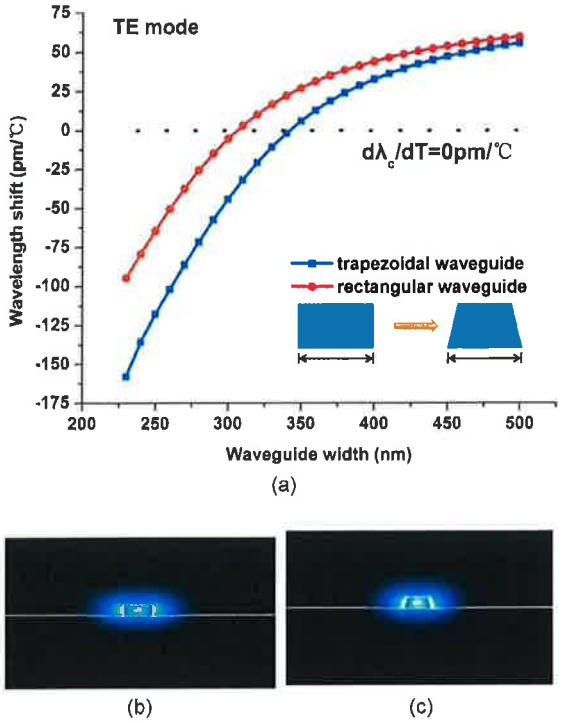

Fig. 1. (Color online) (a) Simulation of the temperature dependence of AWGs' central wavelength with waveguide widths for rectangular (red, circles) and trapezoidal (blue, squares) shape SOI waveguides (b) and (c). Optical modes at two critical width values for rectangular and trapezoidal shape SOI waveguides.

the experiment, we found that the combination of proper layout design and polymer overlay treatment can greatly eliminate the disadvantages brought by using narrowed arrayed waveguides.

Our design is based on the normal waveguide dimensions (450 nm × 220 nm) for the access waveguides to the star couplers and the bend waveguides in the AWGs. The narrowed waveguides are inserted for the straight waveguide arms only. The same rules for designing normal SOI AWGs are implemented on arranging these narrowed waveguides. The schematic picture is shown in Fig. 2. Compared with our early design [21], such layout with straight arrayed waveguides structures folded by two 90° broad bend waveguides is much more flexible. It makes sharp bends and close spacing of the arms possible [1], thus the footprint of devices is greatly reduced. In addition, compared with bent arrayed waveguides, the phase differences of the arrayed waveguides between each other in this layout are much more controllable, which helps reduce the cross talk.

The standard SOI wafer with a silicon layer of 220 nm and an oxide layer of 2 μm is used for this work. The SOI waveguides are fabricated by 193 nm deep UV lithography and inductively coupled plasma–reactive ion etching in a standard CMOS fabrication process [22]. The CMOS compatible fabrication processes offer the advantage of high resolution as well as high throughput. By varying the exposure dose over the whole SOI wafer for the

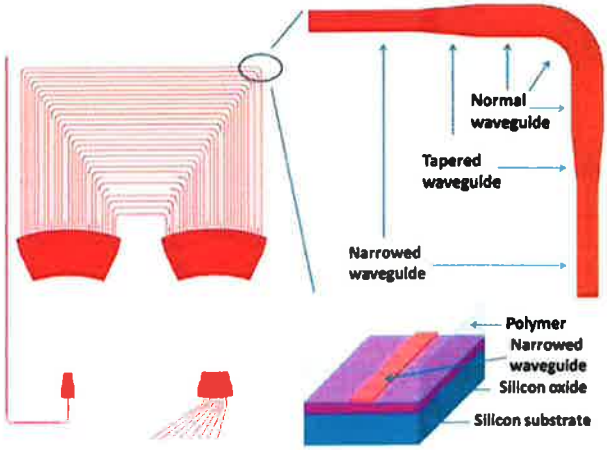

Fig. 2. (Color online) Schematic picture of the proposed AWGs inserted with narrowed arrayed waveguides.

patterning of the waveguides, narrowed waveguides with width values ranging from 330 nm to 390 nm were obtained. The double-etch technique was adopted for the star couplers' area to reduce reflections [3]. Surface grating couplers, which selectively pick up the TE mode from the optical fiber, are also fabricated at the end of the input and output waveguides [23]. The SEM pictures of the critical parts of the AWGs mentioned above are shown in Fig. 3. After cleaning, Polymer PSQ-LH with a large TO coefficient of -2.4×10^{-4} as well as low loss at 1550 nm and high thermal stability below 200 °C [19], is chosen as the cladding material and spin-coated on top of the fabricated SOI chips, with a layer thickness around 2 μm.

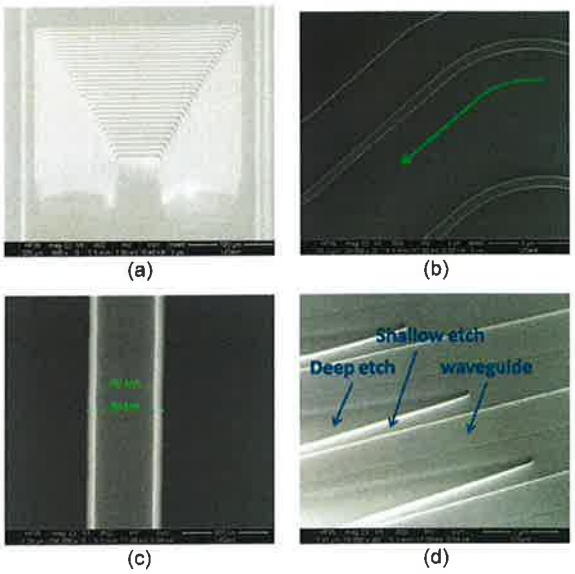

Fig. 3. (Color online) SEM pictures of the critical parts of the AWGs: (a) the whole image, (b) transition from broadband waveguide to narrowed arrayed waveguide through a linearly tapered waveguide, (c) trapezoidal waveguide fabricated by the CMOS technique, and (d) star couplers' area fabricated by the double-etch technique.

3. Measurement Results and Discussion

For measurements, a super luminescent light emitting diode is used as the light source. An optical spectrum analyzer (Agilent 86140B) is used to record the measurement data. In order to measure the AWG's spectra under different temperatures, the samples were mounted on a heating plate whose temperature could be controlled accurately. The temperature dependences of the peak wavelength for one of the central channels (channel 4) with different waveguide widths, before and after the polymer overlay, are shown in Fig. 4. In general, the SOI AWGs have an average wavelength temperature dependence above 65 pm/°C before the polymer overlay [Fig. 4(a)]. Although in theory these slope values of wavelength shift per degree should increase monotonically with waveguide widths due to the higher optical confinement, they are too high and too close to each other

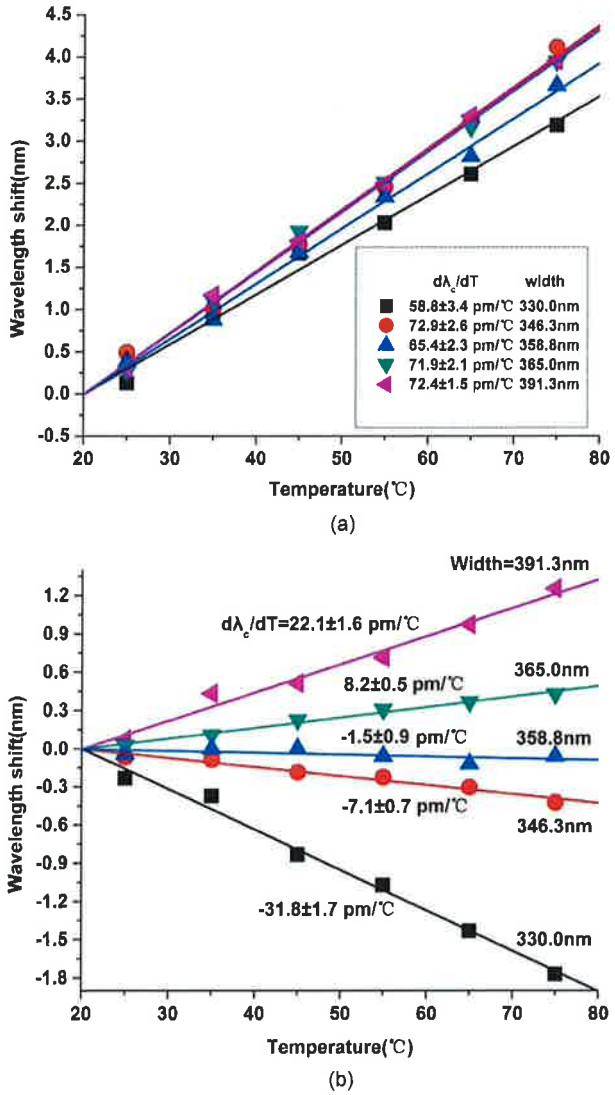

Fig. 4. (Color online) Temperature dependence of the peak wavelength of channel 4 (a) before polymer overlay and (b) after polymer overlay for different waveguide widths.

to be resolved by our current measurement system, which is affected by the measurement environmental stability, the temperature control accuracy of the heating plate, the resolution of the optical spectrum analyzer, the adopted fitting method and so on. However, the high-temperature dependence of the channel peak wavelength can be suppressed with polymer overlay. In Fig. 4(b), the AWGs with different narrowed arrayed waveguide widths exhibit obviously different temperature dependent behavior. The lowest temperature dependence was obtained for a waveguide width of 358.8 nm, where the temperature dependence of the filter peak wavelength was successfully reduced from above 65.4 pm/°C to −1.5 pm/°C, i.e., more than 1 order of magnitude lower than that of the normal SOI AWGs. This obtained width value also matches well with the previous simulation results based on a trapezoidal waveguide model in which the optimal value is 340 nm. It also explains the reason why there was a gap between the 350 nm experimental value and the 306 nm simulated value in our previous demonstration of athermal SOI ring resonators [13].

The comparison of the full spectrum of the proposed AWG at 25 °C and 75 °C with and without polymer cladding is shown in Fig. 5. It can be seen that normal SOI AWG (without polymer cladding) have around 3.3 nm total spectrum shift with 50 °C temperature change, a shift which already exceeds the designed channel spacing of 400 GHz. In contrast, the total spectrum shift of the proposed AWG with polymer overlay is greatly reduced to only around 0.2 nm in this large temperature range, while keeping the good filtering property at the same time.

It can also be seen from Fig. 5 that the AWGs' characteristics are also improved significantly after the polymer overlay. For the central channel 5, the insertion loss is reduced from 6.6 to 2.6 dB. The loss value of the AWG is extracted by normalizing the input to output port transmission of the AWG to that of a simple photonic wire. The reduced insertion loss can be explained by reduced scattering losses of the narrowed arrayed waveguides because the refractive index contrast is reduced by polymer deposition. The cross talk is reduced from −11 to less than −15 dB as a result of smaller phased errors. The variation of the effective index of the arrayed waveguides with their width plays the most significant role in inducing phased errors, which can be expressed as $\partial n_c/\partial w$, where n_c is the effective index and w is the waveguide width. This stochastic nanometer-scaled width variation is inevitable during fabrication and it becomes worse with the decreasing of waveguide width [24]. For 350 nm width, simulation of the waveguide mode shows that this value is reduced by around 45% with polymer cladding, thus resulting in lower cross talk. The junction loss between the arrayed waveguides and the two star couplers might also be lower. The nonuniformities between central and edge channels are around 0.7 dB.

Although athermalization of silicon AWGs with characteristics at an average level has been

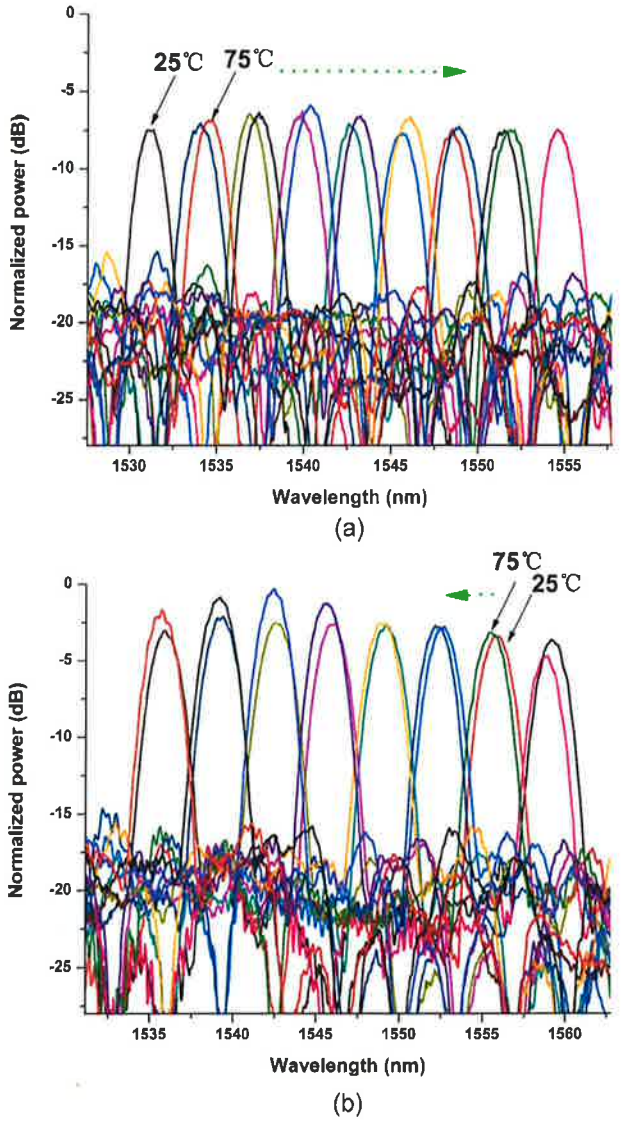

Fig. 5. (Color online) Full spectrum of the proposed AWGs at 25 °C and 75 °C (a) without and (b) with polymer cladding.

successfully realized in this paper, the characteristics of the AWGs are still below those of silica AWGs or of optimized silicon AWGs and further improvements are still required and expected. This requires more advanced fabrication techniques which can significantly reduce the phase errors.

Silicon AWGs working in the TM mode regime can also be a solution. The TM mode of a silicon wire waveguide is less confined than the TE mode, which means that the waveguide can be compensated more easily by overlaying a polymer. Thus broad arrayed waveguides can be used instead of narrowed ones. Moreover, there is no discontinuity of the electrical field at the vertical sidewalls, where the waveguide roughness and width variation are unavoidable due to the fabrication. This would reduce the propagation loss and phase noise dramatically. Based on these arguments, the characteristics of athermal silicon AWGs are expected to be improved. However, special attention must be paid during the design to prevent mode conversions between TM and TE modes and other challenges. So far, to our best knowledge, no working TM-mode AWG devices have been demonstrated. The other potential challenge is post-trimming of this athermal device. High intensity UV light trimming or electron beam induced compaction and strain trimming could be the possible solutions. [14,25]

4. Conclusion

In summary, a compact athermal SOI-based 1 × 8 AWG with 400 GHz channel spacing is demonstrated for the first time. The total size of the device is 350 μm × 250 μm. By insertion of the straight narrowed arrayed waveguides and overlay polymer layer, the wavelength temperature dependence of the AWG is successfully reduced to only −1.5pm/°C. Good characteristics of the AWG such as low insertion loss and cross talk are also obtained at the same time. The athermal AWG proposed in this paper is expected to be an important component in optical telecommunication networks or complicated hybrid integrated circuits.

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