Planar Concave Grating Demultiplexer Fabricated on a Nanophotonic Silicon-on-Insulator Platform

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***Abstract*—We show that a nanophotonic silicon-on-insulator (SOI) platform offers many advantages for the implementation of planar concave grating (PCG) demultiplexers, as compared with other material systems. We present for the first time the design and measurement results of a PCG demultiplexer fabricated on a nanophotonic SOI platform using standard wafer scale CMOS processes including deep-UV lithography. Our PCG device has four wavelength channels with a channel spacing of 20 nm and a record-small footprint of 280×150 μm. The on-chip loss is 7.5 dB, and the crosstalk is better than -30 dB.**

***Index Terms*—Demultiplexing, diffraction, gratings, nanophotonics, silicon-on-insulator (SOI).**

I. Introduction

THE TWO main techniques available today for implementing (de)multiplexer functionality based on planar spectrograph-type designs are arrayed waveguide gratings (AWGs) and etched planar concave gratings (PCGs). Both types of demultiplexers have been demonstrated in many material systems, including silica-on-silicon [1], [2], III–Vs [3], [4], and large-core silicon-on-insulator (SOI) platforms [5], [6]. AWGs have become increasingly popular due to their more simple and tolerant technology, as compared with PCGs. Silica-based AWGs are widely used in wavelength-division-multiplexing systems in the 1.5–1.6 μm wavelength range due to their low insertion loss and low crosstalk. Grating-based devices require deeply etched grating facets and the losses of these devices depend critically on grating profile imperfections, and particularly, the verticality of these deeply etched grating facets remains a critical issue.

To reduce the size and increase the integration density of these devices and photonic IC's in general, the nanophotonic SOI platform is an interesting candidate. It consists of a submicrometer Si core layer (refractive index $n = 3.45$) on top of a SiO_2 buried layer ($n = 1.45$), which is carried on a Si substrate. By etching through the Si top layer, a very high refractive index contrast is obtained in both vertical and horizontal directions. This allows the creation of so-called photonic wire waveguides with core sizes of only 0.1 μm^2 and bend radii as small as 1 μm [7], [8], which can be fabricated using wafer scale CMOS processing techniques [9]. This opens the way to low-cost integrated components that can be mass-fabricated and integrated with CMOS electronics on the same chip.

Ultracompact AWGs have already been demonstrated on a nanophotonic SOI platform [8], [10], [11]. However, these devices still have significant crosstalk arising from multiple sources. The high index contrast, submicrometer size waveguides are very sensitive to small waveguide width variations such as random roughness and longer scale variations or more systematic mask digitization errors. This can give rise to significant phase errors between the delay lines. In this paper, we present for the first time a PCG demultiplexer fabricated on a nanophotonic SOI platform using standard wafer scale CMOS processing techniques including deep-UV lithography. Measurements show that crosstalk is not a major issue in these devices. The nanophotonic SOI platform offers other major advantages, as compared with PCGs fabricated in other material systems. First, there is no need for dedicated deep etching techniques to define the grating facets. Also, the strict fabrication tolerances on facet nonverticality are relaxed, and finally, there is no deterioration of insertion loss and crosstalk caused by multimodal propagation in the slab region. This will be discussed further.

In this paper, we primarily focus on the proof op principle demonstration of a PCG demultiplexer on a nanophotonic SOI platform without considering advanced grating geometries and passband tailoring techniques to obtain flat-top-shaped passbands.

The remainder of this paper is organized as follows. In Section II, the operating principles and design method of the PCG are described. Section III discusses the simulation method and gives an overview of the simulation results, Section IV describes the fabrication. We discuss the measurement results in Section V and conclude in Section VI.

II. Design

A concave grating combines the function of a flat grating to spatially separate different wavelengths from the input waveguide and a focal lens to focus the light into a series of output waveguides. We consider the conventional Rowland geometry [12], [13]. The design principles of a PCG based

Manuscript received October 19, 2006; revised January 23, 2007. This work was supported in part by the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT-Vlaanderen) under the SBO epSOC project and in part by the European Union in the framework of the IST-ePIXnet network of Excellence and the Silicon Photonics Platform. The work of W. Bogaerts was supported by the Flemish Fund for Scientific Research (FWO-Vlaanderen) through a postdoctoral fellowship. The work of P. Dumon was supported by IWT-Vlaanderen through a scholarship.

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Digital Object Identifier 10.1109/JLT.2007.893025

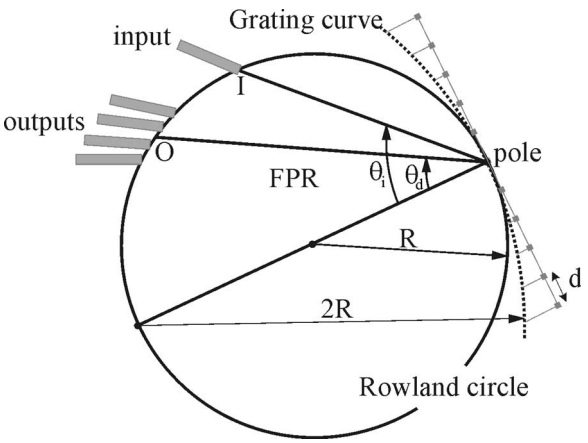

Fig. 1. PCG demultiplexer based on Rowland configuration.

on the Rowland configuration are well-known and widely described in literature [14]. The layout is shown in Fig. 1.

The input and output waveguides are positioned along a circle with a radius R, called the Rowland circle. The grating facets sit on a grating circle with a radius $2R$, and both circles touch at the middle of the grating, which is called the pole. The middle of the grating facets are positioned on the grating circle in such a way that when projected onto the tangent of the circles at the pole, they are spaced equidistantly at distance d, which is the grating period.

The input waveguide ends in an unetched slab region, the free propagation region (FPR), where the light beam expands into the direction of the grating. The concave grating both diffracts and focuses the reflected light back into a series of output waveguides on the Rowland circle. Using this configuration, any point on the Rowland circle is imaged on the same circle with a reflection angle determined by the grating equation:

$$d(\sin\theta_i + \sin\theta_d) = m\frac{\lambda}{n_{\text{eff}}} \tag{1}$$

where d is the grating period, and θ_i and θ_d are the angles between the Rowland circle diameter through the pole and the incident and diffracted beams, respectively. The whole number m is the order of diffraction, λ is the wavelength in vacuum, and n_{eff} is the effective index of the slab mode. Equation (1) states the condition for constructive interference for diffracted beams from adjacent grating facets. Out of this equation and the Rowland construction, other important parameters such as the linear dispersion (LD) [14] and the free spectral range (FSR) can be deduced

$$\text{LD} = \frac{2R}{\cos\theta_d}\frac{m}{d}\frac{n_{\text{g}}}{n_{\text{eff}}^2} = \frac{2R}{\lambda}\frac{(\sin\theta_i + \sin\theta_d)}{\cos\theta_d}\frac{n_{\text{g}}}{n_{\text{eff}}} \tag{2}$$

$$\text{FSR} = \frac{\lambda}{m}\left[1 - \frac{m+1}{m}\left(1 - \frac{n_{\text{g}}}{n_{\text{eff}}}\right)\right]^{-1} \tag{3}$$

where $n_{\text{g}} = n_{\text{eff}} - \lambda(dn_{\text{eff}}/d\lambda)$ is the group index of the slab mode.

In most publications, the term $dn_{\text{eff}}/d\lambda$ is not taken into account, and n_{g} is replaced by n_{eff} in (2) and (3). We will show later that for the nanophotonic SOI platform, the term $dn_{\text{eff}}/d\lambda$ is important and cannot be neglected. Equation (3) is deduced from the grating equation by setting the condition that the direction of a diffracted beam with wavelength λ in an order $(m+1)$ is the same as the direction of a beam with higher wavelength $(\lambda + \delta\lambda)$ diffracted in a lower order m.

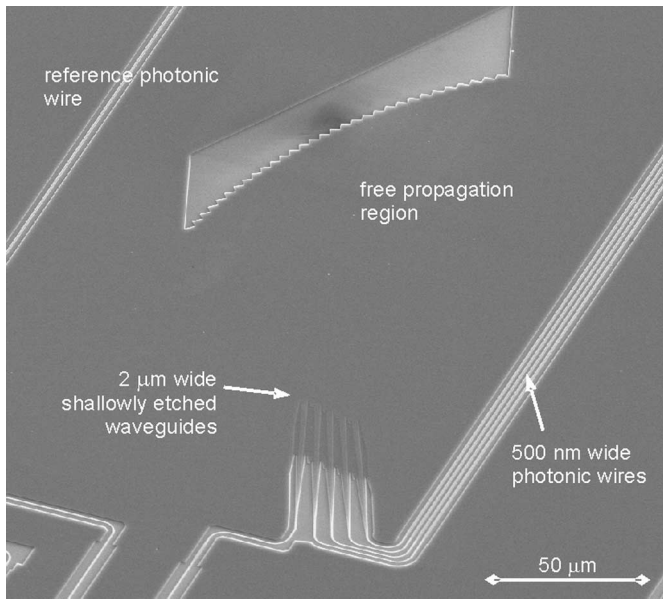

Fig. 2. SEM picture of 1 × 4 PCG demultiplexer.

We fabricated a 1 × 4 demultiplexer on a 200-mm SOI wafer with a silicon top layer of 220 nm and a buried oxide layer of 1 μm. A detailed micrograph of the device is shown in Fig. 2. The demultiplexer is designed around a central wavelength $\lambda = 1.55$ μm. The effective refractive index of the fundamental TE-polarized slab mode $n_{\text{eff}} = 2.83$. The change of this index as a function of wavelength $dn_{\text{eff}}/d\lambda = -0.57$ μm^{-1} and the group index $n_{\text{g}} = 3.7$ around the central wavelength. The four output channels are spaced by 20 nm, resulting in central channel wavelengths of 1.52, 1.54, 1.56, and 1.58 μm. For the definition of the grating facets and the photonic wire access waveguides, the 220-nm-thick Si layer is fully etched. However, the input and output waveguides on the Rowland circle are shallowly etched (70-nm deep), 2-μm wide, and spaced 5-μm apart on this circle. This shallow etching is done in order to reduce both the diffraction angle of the propagating incident beam in the FPR and the transition losses between the waveguides and the FPR.

The size of the PCG can be calculated by means of (2): The Rowland radius R scales linearly with the required LD of the design. The term $n_{\text{g}}/n_{\text{eff}}$ in the last part of this equation is determined by the central wavelength λ and properties of the fundamental TE-polarized slab mode: n_{eff} and $dn_{\text{eff}}/d\lambda$. The larger this term, the smaller the device size for a given LD and a given design. Table I gives a comparison between typical values of $n_{\text{g}}/n_{\text{eff}}$ for the nanophotonic SOI platform considered in this paper and an SOI platform with a 5-μm-high Si slab waveguide [6]. From the values stated in Table I, we can conclude that the demultiplexer with the same layout and specifications (LD, λ, m, θ_i, and θ_d) can be made roughly 21% smaller on the SOI

TABLE I
COMPARISON OF THE PROPERTIES OF THE FUNDAMENTAL TE SLAB MODE FOR TWO DIFFERENT SOI PLATFORMS

	Nanophotonic SOI platform Si slab height = 220nm	Large-core SOI platform Si slab height = 5μm [6]
λ	1.55 μm	1.55 μm
n_{eff}	2.83	3.47
$dn_{eff}/d\lambda$	-0.57 μm^{-1}	-0.08 μm^{-1}
$\left(1-\frac{\lambda}{n_{eff}}\frac{dn_{eff}}{d\lambda}\right)=\frac{n_g}{n_{eff}}$	1.31	1.04

platform considered in this paper as compared to a large-core SOI platform.

The relatively small width of the output waveguides and their high refractive index contrast have an even larger impact on device size. As this allows positioning of the output waveguides more densely along the Rowland circle, the LD and, hence, the size of the device for a given channel spacing $\Delta\lambda$ can be strongly reduced. The output waveguides are spaced only 5-μm apart on the Rowland circle, and this makes it possible to shrink the device by a factor 3, as compared with reported silica-on-silicon PCGs [2], and a factor 4, as compared with PCGs on a large-core SOI platform [6]. On top of that, 500-nm-wide photonic wires access waveguides with a bend radius of a few micrometers allow further decrease of the size of the device [8], [10], [11]. The 1×4 PCG demultiplexer discussed in this paper has, to the best of our knowledge, a record-small footprint of 280×150 μm, including photonic wire access waveguides.

The design process starts with determining the order of diffraction. Equation (3) gives the relation between the order of diffraction and the FSR. As the FSR has to be larger than the operational spectral range of the demultiplexer, the upper limit of the order of diffraction can be calculated. In this design, it is chosen to be $m = 10$. This results in an FSR of 115 nm. The incident and diffracted angles are chosen to be $\theta_i = 41^\circ$ and $\theta_d = 37^\circ$. From (1), we can calculate the grating period $d = 4.35$ μm. This parameter also determines the channel uniformity across the operational spectral range [14]. As the grating facets become smaller, the sinc-shaped diffraction envelope of a single grating facet will broaden, resulting in smaller loss variations over the used spectral range. A smaller grating period can be obtained by decreasing m as can be seen from (1), but then, smaller grating facets are more sensitive to profile imperfections due to fabrication.

The 2-μm-wide shallowly etched output waveguides are spaced 5-μm apart on the Rowland circle. This results in a required LD of 0.25 μm/nm. The Rowland circle radius R and hence the size of the device can than be calculated from (2), which in this design results in $R = 94$ μm.

The 31 grating facets are individually blazed to maximize their reflection at the blaze point *O* (Fig. 1). This point is chosen to be in the middle of the four output waveguides in order to obtain a symmetrical response across the output channels.

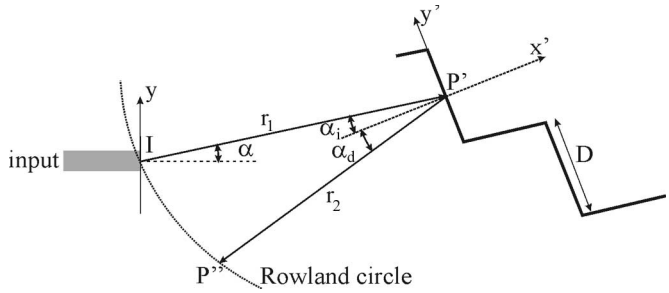

Fig. 3. Schematic view of grating and coordinate system.

III. SIMULATIONS

To verify the design, we performed simulations based on scalar diffraction theory. A schematic view of the grating and the coordinate system used is shown in Fig. 3.

According to the Kirchhoff–Huygens diffraction formula, the incident electric field $E_{\rm inc}$ at the center points of the grating facets (P') at a distance r_1 and at an angle α can be calculated as

$$E_{\rm inc}(P') = \frac{1}{2}\sqrt{\frac{n_{\rm eff}}{\lambda}} \int\limits_{\rm input} E_{\rm wg}(y)\frac{e^{-jkr_1}}{\sqrt{r_1}}(1+\cos\alpha)dy \quad (4)$$

where $k = 2\pi n_{\rm eff}/\lambda$ is the wavenumber within the slab waveguide, and $E_{\rm wg}$ is the electric field profile of the TE-polarized fundamental mode of the input waveguide. Similarly, the diffracted field $E_{\rm out}$ on the Rowland circle is calculated as

$$E_{\rm out}(P'') = \eta\sqrt{\frac{n_{\rm eff}}{\lambda}} \sum_{\rm Grating} \int\limits_{-D/2}^{+D/2} E_{\rm inc}(y')\frac{e^{-jkr_2}}{\sqrt{r_2}}\frac{(\cos\alpha_i+\cos\alpha_d)}{2}dy' \quad (5)$$

where α_i and α_d are the incident and diffracted angles with respect to the normal of each grating facet, and η is the reflection coefficient of the grating. This formula simplifies a lot if we assume that the magnitude of the incident field $|E_{\rm inc}|$ is constant over each facet and the phase of this field changes linearly along the length of the facet

$$E_{\rm inc}(y') = E_{\rm inc}(y'=0)e^{+jky'\sin\alpha_i}. \quad (6)$$

This approximation is valid if the size of the facets is small compared with the distance to the input and if the angle of incidence α_i is small. This is the case if the blaze point (O) is positioned near the input waveguide (I).

Finally, the spectral response of each channel can be obtained by calculating the overlap integral between the diffracted field $E_{\rm out}$ and the field profile of the fundamental mode of the output waveguides. The 2-μm-wide output waveguides support higher order modes, but these modes are filtered out as the waveguides are adiabatically tapered to 500-nm-wide, single-mode photonic wires. Fig. 4 shows the simulated response of

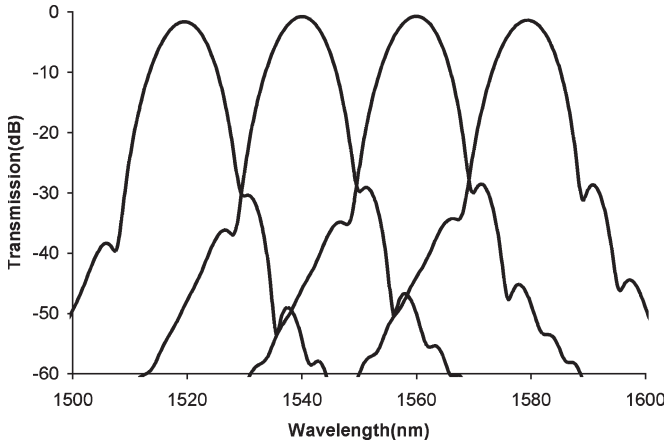

Fig. 4. Simulated transmission spectrum.

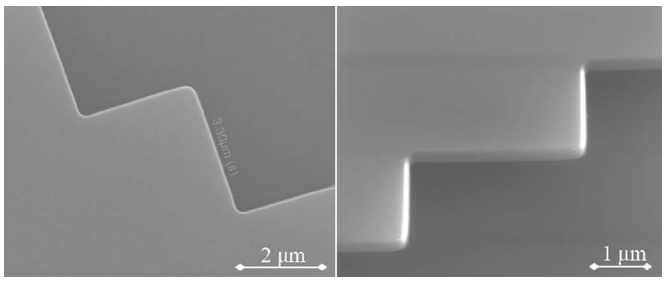

Fig. 5. SEM pictures of grating facets.

the device. For these simulations, the reflection coefficient of the grating η is set to 1.

The nonuniformity across the channels is 0.9 dB, and the insertion loss for the two central channels is 0.7 dB.

IV. Fabrication

For the fabrication, we use CMOS-compatible fabrication techniques on industrial tools. Structures were defined with 248-nm deep-UV lithography and transferred into the silicon using inductively coupled plasma reactive ion etching (ICP-RIE) etching. The fabrication process is described in detail in [9] and [15].

For the definition of the grating and the photonic wires, we etched completely through the 220-nm-thick Si layer. A more shallow etch (70 nm) was used for the definition of the 2-μm-wide entrance and exit waveguides [8], [10]. The deeply and shallowly etched structures are defined in separate lithography and etch steps. Alignment accuracy between both layers is of the order of 50 nm. The transition between deep and shallow waveguides is done using a short but adiabatic transition structure [8]. In the shallow etch step, we also defined grating fiber couplers which allow for easy characterization [15], [16]. Fig. 5 is a detailed photograph of the demultiplexer grating facets.

V. Measurement and Discussion

In order to characterize the demultiplexer, light is coupled from a standard single-mode fiber into a broad ridge waveguide and vice versa using shallowly etched fiber couplers [15], [16]. These waveguides are then tapered down to narrow wires using adiabatic linear tapers. All waveguide structures, including the fiber couplers, are designed for TE-polarized light. If needed, a polarization diversity configuration can be implemented to obtain polarization—insensitive photonic integrated circuits [17].

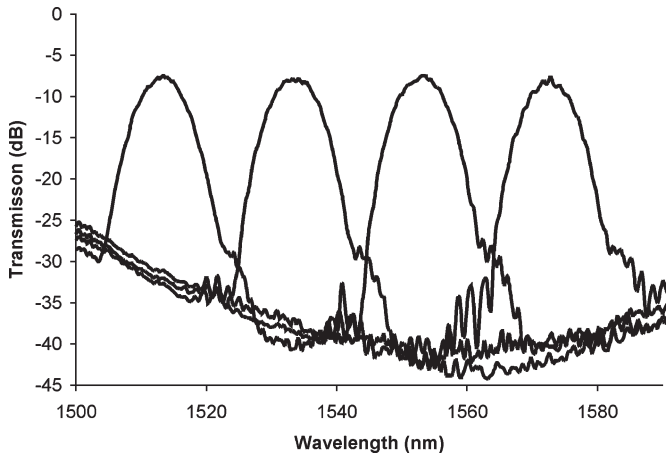

Fig. 6. Measured transmission spectrum (TE polarization) normalized to a reference photonic wire waveguide.

The measured transmission spectrum (TE polarization) of the 1×4 demultiplexer is shown in Fig. 6. This transmission spectrum is normalized to a reference photonic wire waveguide (Fig. 2). The on-chip loss for the central channels is 7.5 dB with a crosstalk better than -30 dB. The loss variation over the channels is 0.6 dB. Measurement results are slightly disturbed by the high noise floor of the measurement setup: The high noise floor at the edges of the operational range is due to the limited bandwidth of the fiber couplers, resulting in low absolute transmission at these wavelengths. As compared with simulation results (Fig. 4), there is a shift in the transmission spectrum of 6 nm toward shorter wavelengths, which can be attributed to a slightly smaller n_{eff}, as compared with the value used in the simulations.

The on-chip loss of 7.5-dB results from several factors. The largest contribution (4.6 dB) is caused by Fresnel reflection loss at the grating since no measures were taken to enhance the reflectivity of the grating facets.

A second contribution is due to the nonverticality of the grating facets. This causes coupling loss between the incident fundamental slab mode and the reflected fundamental slab mode. As mentioned in Section IV, standard deep-UV lithography in combination with ICP-RIE dry etching is used for the definition of the structures, including the grating facets. This fabrication process is not optimized to create perfect vertical sidewalls and results in a rather large nonverticality of 10.5°. However, this only gives rise to an additional loss of 0.3 dB. This brings the total modal reflection loss, including Fresnel loss at 4.9 dB. These reflection losses were calculated by means of CAvity Modelling FRamework (CAMFR) [18], which is a 2-D fully vectorial tool based on eigenmode expansion. A staircase approximation was used for the simulation of the reflection loss at the angled facet. It is important to note that PCGs reported in literature, including PCGs on SOI, have a

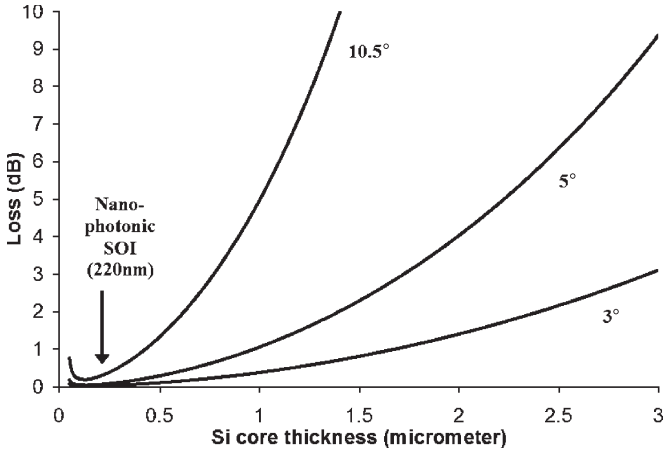

Fig. 7. Coupling loss between incident and reflected fundamental TE slab mode ($\lambda = 1550$ nm) as a function of Si core thickness. Parameter is the deviation from verticality (degrees).

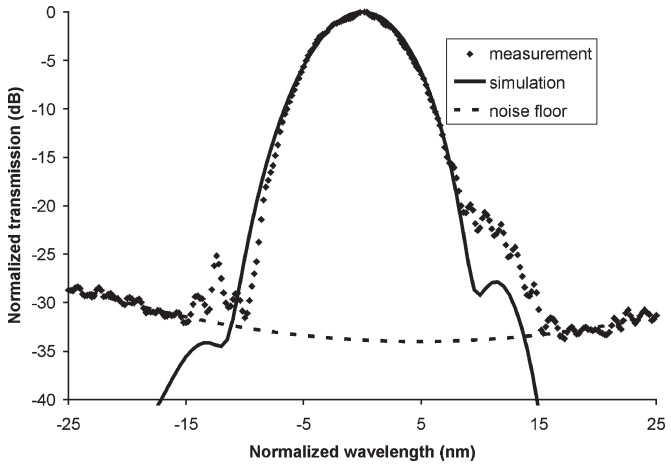

Fig. 8. Comparison between measurement and simulation for channel 3 ($\lambda_0 = 1560$ nm).

several-micrometer-thick FPR with deeply etched grating facets [5], [19]. In these devices, a similar sidewall nonverticality would completely destroy the transmission characteristics, as can be seen in Fig. 7.

In this figure, we plotted the modal reflection loss as a function of silicon core thickness for different values of grating nonverticalities. This was done by calculating the overlap integral between the fundamental modes of two tilted slab waveguides. An even thinner Si core layer ($<$ 220 nm) could be envisioned, further decreasing the reflection loss at the angled facets. However, when the core layer becomes too thin ($<$ 130 nm), mode size will increase again resulting in a higher modal reflection loss as can be seen in Fig. 7.

A third contribution, which is inherent to the design, is the diffraction loss of 0.7 dB for the central channels. This means that 1.9 dB of loss is caused by other effects, mainly grating profile imperfections like facet corner rounding and surface roughness. This low value, as compared to previous reported SOI PCGs [20], is partially due to the fact that the grating only needs to be etched 220-nm deep, making it possible to obtain a high-quality grating profile making use of standard dry etching techniques, as can be seen in Fig. 5. If precautions are taken to reduce the reflection loss at facets like metal coating or total internal reflection (TIR)-type facets [21], we believe that on-chip losses close to 2.9 dB can be achieved.

To prove the validity of the simulation method based on scalar diffraction theory, we compared the measured and simulated transmission of the third channel, as can be seen in Fig. 8. The two spectra are normalized and the measured spectrum is shifted over 6 nm so that the transmission maxima coincide. The spectral shapes around the central channel wavelength overlap almost perfectly. As explained before, comparison of the sidelobes is harder because of the high noise floor of the measurement setup. However, we clearly see two sidelobe structures at -12 and $+12$ nm both in the measured and simulated transmission. The measured sidelobe level is 10 dB higher as compared to simulations. We believe this discrepancy originates mainly from small grating profile imperfections such as facet roughness and corner rounding. Sidelobe structures like these limit the crosstalk value of the device, which is still better than -30 dB.

Notwithstanding the difficulty to compare two totally different demultiplexer designs, this crosstalk value is far better as compared with AWGs fabricated on the same platform and with the same SOI nanophotonic technologies [8], [10]. It is obvious that the grating facets and the FPR of a PCG, which replace the arrayed waveguides in an AWG, introduce fewer phase faults.

Another important advantage of the nanophotonic SOI platform for the fabrication of PCGs is that the 220-nm-high FPR only supports one guided TE-mode. It is known that multimodal propagation in the FPR deteriorates insertion loss and channel crosstalk as different modes have different values of n_{eff} and multiple images are formed along the Rowland circle, each corresponding to an FPR mode [22]. As the FPR only supports one guided TE mode, there is no deterioration of PCG performance caused by excitation of higher order modes.

VI. Conclusion

We show for the first time that the fabrication—making use of standard CMOS wafer scale processing techniques including deep-UV lithography—of PCGs on a nanophotonic SOI platform can lead to very compact devices with high performances. This is a consequence of the fact that grating facets only need to be etched through the 220-nm-thick silicon core.

First of all, this reduces the strict fabrication tolerances of grating verticality as mentioned earlier. Second, a more perfect grating profile can be fabricated (corner rounding, roughness) without the need of dedicated deep etching techniques, and third, since the FPR only supports one guided TE-mode, there is no deterioration of insertion loss and channel crosstalk caused by excitation of higher order modes in the FPR.

We believe that by metal coating the backside of the grating or by adopting TIR-type facets, the on-chip loss can be further reduced to values close to 2.9 dB. On top of that, the nanophotonic SOI platform has numerous advantages, as compared with other material systems [23]. It makes it possible to reduce the

size of these devices, and CMOS fabrication techniques open the way for the realization of low-cost components that can be mass fabricated.

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