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Calculation Of The Packet Loss In Optical Packet Switches: An Analytic Technique

Joris Walraevens, Sabine Wittevrongel, Herwig Bruneel

Abstract **In this paper, we investigate the performance of optical packet switches. Optical packet switches are operated entirely in the optical domain (except for the header extraction). The optical buffering is realised by using fiber delay lines (FDL's). We analyse, using generating functions, an optical buffering structure, consisting of FDL's with increasing lengths. We use this analysis to investigate the packet loss rate (PLR) in two types of switches with output buffering.**

Keywords **optical packet switch, queueing analysis**

1. Introduction

Optical packet switching seems a promising technique to cope with the explosive growth of the Internet traffic [1]. Optical packet switching can offer more bandwidth and more processing capacity than the traditional electronic packet switching networks. A conceptual model of an optical packet switch is shown in Fig. 1. Packets arrive to the switch via a number of incoming fibers and each fiber carries a number of wavelengths. The headers of the packets are extracted and processed electronically. From this information, each packet is switched independently from the other packets to its requested output, where it leaves the switch via an outgoing fiber once the header is rewritten. Since the switching has to be done entirely in the optical domain however (except for the header processing), a means for optical buffering is needed, to deal with packet contentions. One way of buffering optically is the use of fiber delay lines (FDL's) [2, 3]. In case of contention, the packets which cannot be transmitted directly, are delayed in these fibers, thus using the optical fibers as a temporary buffer. The delay caused by putting a packet in such an FDL obviously depends on the length of that particular delay line.

There are a number of different types of optical packet switches proposed in literature. They can be categorised into two main classes (see also [4]): (i) optical packet switches with recirculation buffering and (ii) optical packet switches with output buffering. In a recirculation buffering switch, if more than one packet is scheduled for the same output at the same time, all packets but one are recirculated to the input of the switch via FDL's. These packets are then, together with the newly arrived packets again switched to the desired outputs. Different types of FDL structures are proposed (consisting of FDL's with identical lengths, of FDL's with increasing lengths, ...). Switches of this type are analysed e.g. in [5, 6]. In the output buffering technique on the other hand, FDL's of different lengths are situated at the output side of the switch. When contentions occur, the not directly transmitted packets are put into the delay lines, giving them an extra delay, instead of discarding them immediately. By providing delay lines with different lengths, buffered packets that entered the delay lines at the same time, will leave them at different time instants thus resolving the contention between those particular packets.

In this paper, we first analyse the delay line contents of an FDL-structure with increasing lengths using a generating-functions approach. As shown in Fig. 2, the packets can be buffered in N delay lines with increasing lengths (ranging from 1 times the packet length to N times the packet length). From the obtained generating functions, we then calculate the packet loss rate (PLR) in optical packet switches with dedicated or shared output buffering.

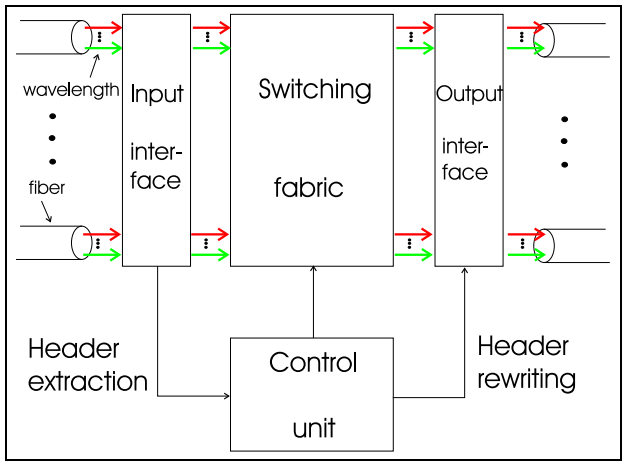

Fig. 1. Conceptual model of an optical packet switch.

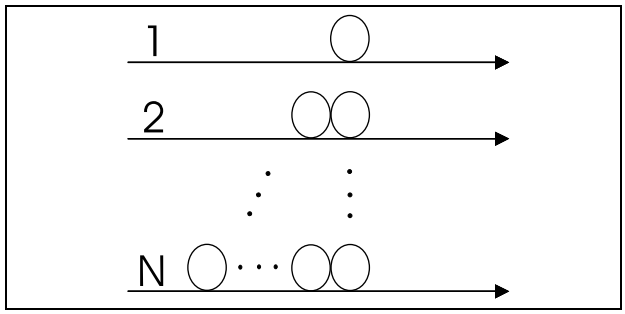

Fig. 2. FDL-structure under consideration.

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The remainder of this paper is structured as follows. In the following Section, we present the mathematical model of the FDL-structure under consideration. In Section 3, we will then analyse the steady-state delay line contents using generating functions. In Section 4, we will use our results to calculate the PLR in switches with output buffering and show some numerical examples. Finally, some conclusions are formulated in Section 5.

2. The Mathematical Model

We consider an FDL-structure consisting of N delay lines with increasing lengths (see Fig. 2). We assume that the number of packet arrivals to the FDL-structure on different wavelengths (if more than one) are uncorrelated, so that it suffices to analyse the delay line contents of one wavelength. We assume that the optical packets have deterministic lengths and the i-th delay line ($i = 1, .., N$) has a length of i times the packet length. Time is assumed to be slotted, where one slot corresponds to the time needed to transmit a packet. We also assume that the arrivals of packets at the input of the FDL-structure are synchonized with respect to the slot boundaries; specifically, packets can only arrive at the end of a slot. We denote the number of arrivals at the end of slot k by a_k. The number of packet arrivals are assumed to be independent and identically distributed (i.i.d.) from slot-to-slot and are characterized by the probability mass function (pmf)

$$a(m) = \text{Prob}[a_k = m],\ m \geq 0.$$

Finally, we assume that the scheduling discipline is *smallest FDL first*. In this scheduling discipline, if i packets arrive at the same time, they are put in the i delay lines with the smallest lengths if $i \leq N$. If $i > N$, N packets are put in the N delay lines and the other $i - N$ packets are lost. A packet put in the i-th delay line, needs exactly i slots to exit this delay line. So, once put in a specific delay line, a delayed packet cannot be transmitted before it reaches the end of this delay line, even if the output becomes available in the meantime. This is an important difference with the (traditional) electronical buffers, where a buffered packet can be retrieved from the memory at any time.

3. Delay Line Contents

In this section, we analyse the delay line contents of the FDL-structure under consideration. We define the random variable $r_{j,k}$ as the (total) number of packets present in the delay lines at the beginning of slot k, that need another $N-j+1$ slots to leave the delay line they are in. This definition is illustrated in Fig. 3. So, e.g. $r_{N,k}$ is the number of packets in the delay lines that will leave the FDL-system at the end of slot k, while $r_{1,k}$ is the number of packets that entered the last delay line (of length N times the packet length) at the end of slot $k-1$, and thus needs another N slots to leave this delay line. Note that $r_{j,k} \leq j$.

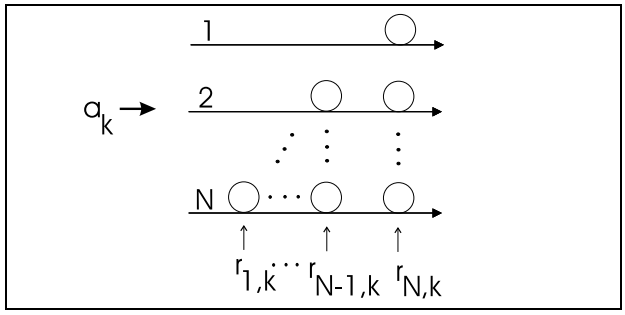

Fig. 3. FDL-structure with the relevant stochastic variables.

The following system equations can then be established:

$$r_{j,k+1} = r_{j-1,k} + t_{j,k}, \tag{1}$$

for $j = 1, .., N$, with $r_{0,k} = 0$ and

$$t_{j,k} = \begin{cases} 0 & \text{if } a_k \leq N - j \\ 1 & \text{if } a_k > N - j. \end{cases} \tag{2}$$

In other words, $t_{j,k}$ equals 1 if and only if a newly arriving packet is put in the $(N - j + 1)$-th delay line at the end of slot k. These system equations can be understood as follows: the packets in the delay lines at the beginning of slot k are one slot closer to their departure instant at the beginning of the next slot (or the packets move one column to the right in Fig. 3 during one slot). The $r_{N,k}$ packets who needed still one slot before departure (at the beginning of slot k) leave the system at the end of slot k. Furthermore, a_k new packets arrive at the end of slot k and these are put (on the left side) in the smallest delay lines first (the a_k top delay lines in Fig. 3).

Let us now denote the joint probability generating function (pgf) of the $r_{j,k}$ ($j = 1, .., N$) as

$$P_k(z_1, .., z_N) = E\left[\prod_{j=1}^{N} z_j^{r_{j,k}}\right].$$

Using the system equations (1), we then find:

$$P_{k+1}(z_1, .., z_N) = T(z_1, .., z_N) P_k(z_2, .., z_N, 1), \tag{3}$$

with $T(z_1, .., z_N)$ the joint pgf of the $t_{j,k}$ ($j = 1, .., N$), i.e., $T(z_1, .., z_N) = E\left[\prod_{j=1}^{N} z_j^{t_{j,k}}\right]$. It is clear that the pgf's $P_k(z_1, .., z_N)$ and $P_{k+1}(z_1, .., z_N)$ converge both to a common steady-state value:

$$P(z_1, .., z_N) = \lim_{k \to \infty} P_k(z_1, .., z_N).$$

By taking the $k \to \infty$ limit of equation (3), we obtain:

$$\begin{aligned} P(z_1, .., z_N) &= T(z_1, .., z_N) P(z_2, .., z_N, 1) \\ &= \prod_{i=1}^{N} T(z_i, .., z_N, 1, .., 1). \end{aligned} \tag{4}$$

It now remains for us to determine the pgf $T(z_1, .., z_N)$. This can be done by means of equations (2). It follows that

$$T(z_1, .., z_N) = \sum_{j=0}^{N-1} \left(a(j) \prod_{l=N-j+1}^{N} z_l \right) + \left(1 - \sum_{j=0}^{N-1} a(j) \right) \prod_{l=1}^{N} z_l. \quad (5)$$

Using equation (5) in equation (4), we finally find the following explicit expression for $P(z_1, .., z_N)$:

$$P(z_1, .., z_N) = \prod_{i=1}^{N} \left[\sum_{j=0}^{i-1} a(j) + \sum_{j=i}^{N-1} \left(a(j) \prod_{l=N-j+i}^{N} z_l \right) + \left(1 - \sum_{j=0}^{N-1} a(j) \right) \prod_{l=i}^{N} z_l \right]. \quad (6)$$

From the above expression some interesting marginal pgf's can be calculated. For instance $U(z)$, the pgf of the total delay line contents at the beginning of a slot, is given by

$$\begin{aligned} U(z) &= P(z, .., z) \\ &= \prod_{i=1}^{N} \left[\sum_{j=0}^{i-1} a(j) + \sum_{j=i}^{N-1} a(j) z^{j-i+1} + \left(1 - \sum_{j=0}^{N-1} a(j) \right) z^{N-i+1} \right]. \end{aligned}$$

A more interesting pgf is the generating function of the number of packets that leave the delay lines at the end of a slot, since this is closely related to the packet loss at the output of the FDL-system. This pgf is obtained as

$$\begin{aligned} R_N(z) &= \lim_{k \to \infty} E\left[z^{r_{N,k}} \right] = P(1, .., 1, z) \\ &= \prod_{i=1}^{N} \left[z + (1 - z) \sum_{j=0}^{i-1} a(j) \right]. \end{aligned} \quad (7)$$

From the above generating functions, we can derive several performance measures, such as the moments and the distributions of the respective stochastic variables. We will demonstrate their use by calculating the PLR in output queueing optical packet switches in the following section.

4. Numerical Examples

In this Section, we use the results of the previous analysis to study the performance of output queueing optical packet switches. Specifically, we investigate the packet loss in two types of optical packet switches with output queueing, i.e., switches with dedicated FDL's per outlet and switches with a shared FDL-structure over all outlets respectively.

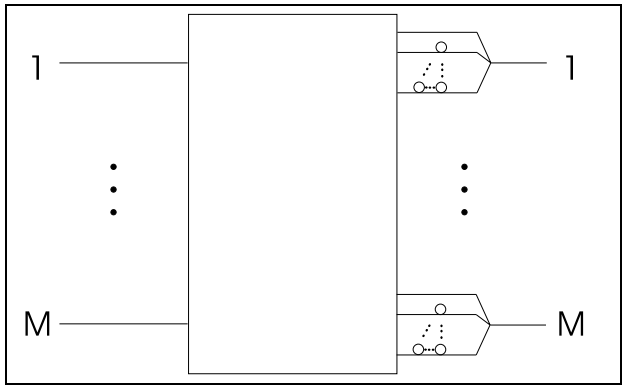

Fig. 4. Optical packet switch with dedicated FDL's per output.

4.1 Dedicated Buffering

The first type is an MxM optical packet switch with dedicated FDL's per output, as shown in Fig. 4. Packets enter the switch via the inputs of the switch and are then routed to one of the outputs according to their destination. In order to resolve possible contention, every output has an FDL-structure consisting of N delay lines with increasing lengths. As a result, when i packets are switched to the same output at the same time, one of these packets will be transmitted directly, a $\min(i-1, N)$ number of them will be put in the output FDL-structure and thus will be delayed for j slots ($j = 1, .., \min(i-1, N)$) respectively, and – in case more than $N+1$ packets are switched to the same output at the same time – the remaining packets will be lost.

We assume an independent and uniform switching process, i.e., every packet is randomly switched to one of the outputs and independently of the other packets. Since all outputs are then statistically identical, we choose one of the outputs and analyse the PLR at the selected ("tagged") output. We denote the pmf of the number of packet arrivals at the end of a slot at the entrance of the tagged output's FDL-structure by $b(n)$, $n \geq 0$.

At the outputs there are two locations where packet loss can occur. First, if more than $N+1$ packets are switched to the same output at the same time, packets get lost at the entrance of the FDL-structure. Secondly, at the output side of the FDL-structure only one of the packets that leave the FDL's at a specific time instant can be transmitted (provided that no new packets are switched to the output at that time) and as a result the other packets are lost. Since the PLR can be calculated as the mean total number of packets that are switched to the tagged output and get lost at the end of a slot, divided by the mean total number of packets that are switched to this output at the end of a slot, we find the following expression:

$$PLR = \left[b(0) \sum_{n=1}^{N} (n-1) r_N(n) + \sum_{m=1}^{\infty} b(m) \sum_{n=0}^{N} ((m - (N+1))^+ + n) r_N(n) \right] / \bar{b}, \quad (8)$$

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with $\bar{b}$ the mean number of packets switched to the tagged output and with $r_N(n)$ the probability that the number of packets that leave the FDL-structure at the end of a random slot equals n and $(.)^+ = max(0, .)$. Formula (8) can be understood as follows: the denominator equals the mean number of packets that are switched to the tagged output at the end of a random slot. The numerator expresses the mean number of packets that get lost at that output at the end of a slot. The first term of the numerator corresponds to the number of packets that get lost when no new packets are switched to the tagged output. In this case, which occurs with probability $b(0)$, 1 of the n packets that leave the FDL-structure at the end of the slot, is transmitted and the others get lost. If at least one new packet is switched to the tagged output, one of those new packets is transmitted directly and the packets that leave the FDL-structure at the same moment are all lost (only one packet per output can be transmitted during a slot). If no more than $N+1$ packets are switched to the designated output, no loss occurs at the entrance of the FDL-structure (and $(m-(N+1))^+ = 0$ in equation (8)). On the other hand, if more than $N+1$ packets are switched to the tagged output, $m-(N+1)$ packets get lost at the entrance. These have to be added to the number of packets lost at the exit of the FDL-structure, to account for the total packet loss in this case.

After some mathematical manipulations, expression (8) can be transformed into the following formula:

$$PLR = \left[\bar{b} + \bar{r}_N + \sum_{m=0}^{N+1} ((N+1-m)b(m)) - (N+1) - b(0)(1-r_N(0)) \right] / \bar{b}, \quad (9)$$

with $\bar{r}_N$ the mean number of packets that exit the output's FDL-structure at the end of a random slot. So, in order to be able to calculate the PLR, we need $\bar{r}_N$ and $r_N(0)$, and these can be calculated from the analysis in Section 3.

For the following figures, we assume a Bernoulli arrival process at the inlets of the switch, i.e., at every inlet a packet arrives with probability λ and no packets arrive with probability $1-\lambda$ at slot boundaries. In Fig. 5, we have shown the PLR as a function of the arrival rate λ, when $M = 6$ and $N = 0, \ldots, 3$ respectively. Without delay lines in the switch ($N = 0$), the PLR is less than 0.4. When $N = 1$, the PLR is reduced significantly. Adding at every output one more delay line ($N = 2$), lowers the PLR even more, but adding more delay lines, does not have a significant effect.

In Fig. 6, the PLR is shown when N varies, $M = 6$ and $\lambda = 0.1$, 0.5, 0.75, 0.9 and 1 respectively. As expected the PLR is strongly related to the arrival rate λ, i.e., to the load that is offered to the switch. This figure also shows that making the number of delay lines larger than 2 does not give much advantage.

From Figs. 5 and 6, we can conclude that just adding more delay lines does not reduce the PLR significantly. The reason for this is that although adding more delay lines at an output line reduces the number of packets lost *before* the delay lines, the problem is only shifted, because

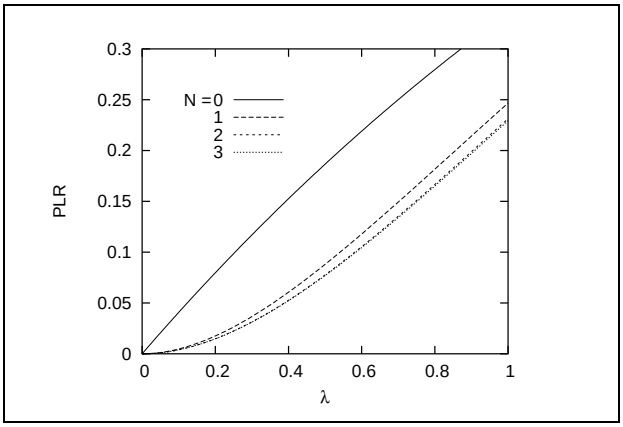

Fig. 5. PLR versus the arrival rate when the number of inlets M is 6.

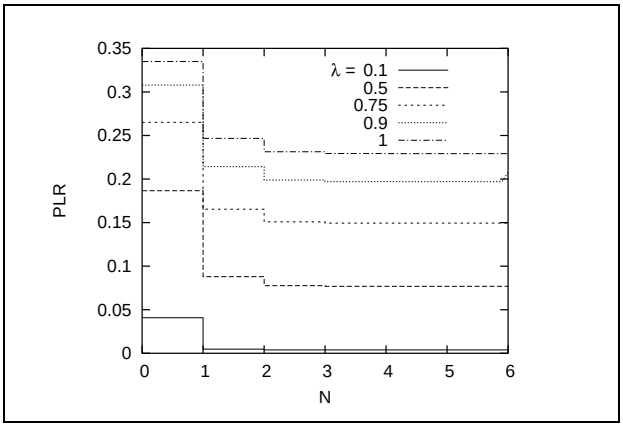

Fig. 6. PLR versus the number of delay lines per output when the number of inlets M is 6.

the delayed packets have a higher probability of still being lost when they exit the delay lines (because of a higher probability of more than one packet exitting the delay lines at the same output at the same time). This can also be concluded from Fig. 7. This figure shows the same as Fig. 5, but the results of the smallest delay line first scheduling (upper curves in the figure) are compared with the results for a traditional queue with a queuelength of N (lower curves) for $N = 0, \ldots, 3$. The latter series of curves represent the smallest PLR that can be obtained with N FDL's and can thus be seen as a lower bound for the PLR in the analysed switch (for a specified N).

4.2 Shared Buffering

In this subsection, we analyse the PLR in an MxM optical packet switch with shared output buffering. This type of switch is shown in Fig. 8. Again, packets enter the switch via the inputs of the switch and are then routed to one of the outputs according to their destination. In order to resolve possible contention, there is now a shared FDL-structure consisting of N delay lines with increasing lengths. As a result, when i arriving packets cannot be

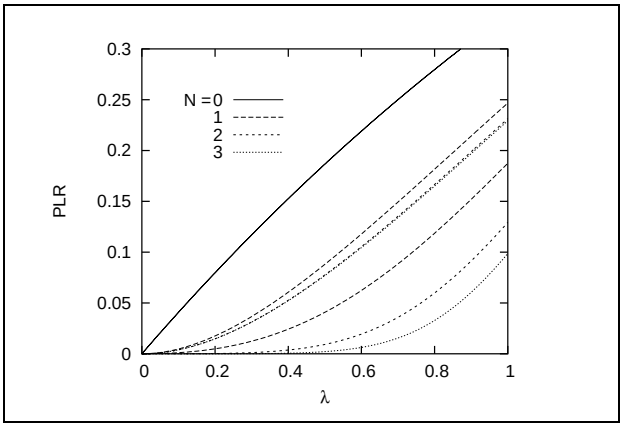

Fig. 7. PLR versus the arrival rate when the number of inlets M is 6 compared with the lower bounds.

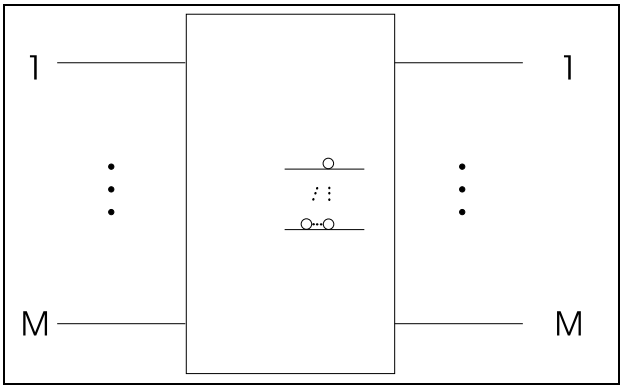

Fig. 8. Optical packet switch with shared output queueing.

transmitted due to contention with other arriving packets (contention occurs when more than one packet is switched to the same outlet), a $\min(i, N)$ number of them will be put in the shared FDL-structure and thus will be delayed for j slots ($j = 1, .., \min(i, N)$) respectively, and – in case more than N arriving packets cannot be transmitted directly – the remaining packets will be lost. A packet departing the FDL-structure is transmitted if its outlet is not already occupied (by a newly arriving packet or another packet leaving the FDL lines); otherwise, the packet is lost.

We assume again an independent and uniform switching process, i.e., every packet is randomly switched to one of the outputs and independently of the other packets. We denote the total number of packet arrivals to the switch at the end of a slot by c and its pmf by $c(n)$, $n \geq 0$.

Again two locations can be specified where loss can occur. First, if more than N arriving packets have to be delayed/buffered, packets get lost at the entrance of the FDL-structure. Secondly, at the output side of the FDL-structure, if a packet departing from an FDL has to be transmitted via an already occupied outlet, the packet is lost. Since the PLR can be calculated as the mean total number of packets that get lost in the switch at the end of a slot, divided by the mean total number of packets that arrive at the end of a slot, we find the following expression:

$$PLR = \left[\sum_{n=0}^{N} r_N(n) \sum_{m=1}^{\infty} c(m) \sum_{l_1=0}^{m} \sum_{l_2=0}^{n} ((l_1 - N)^+ + l_2) \hat{a}_M(m - l_1|m) \hat{a}_{M-m+l_1}(n - l_2|n) \right] / \bar{c}, \qquad (10)$$

with $\bar{c}$ the mean number of packet arrivals to the switch at the end of a random slot and $r_N(n)$ the probability that the number of packets that leave the FDL-structure at the end of a random slot equals n and $\hat{a}_m(n|j)$ =Prob[n of a total of j packets can effectively be transmitted over m specified outlets at the end of a slot]. Formula (10) can be understood as follows: the denominator equals the mean number of packets that arrive to the switch at the end of a random slot. The numerator expresses the mean number of packets that get lost in the switch at the end of a slot. When m new packets arrive in the switch (with probability $c(m)$), and $m - l_1$ of them can be transmitted directly (with probability $\hat{a}_M(m - l_1|m)$), l_1 packets have to be delayed. If $l_1 \leq N$ they can all be buffered, otherwise $l_1 - N$ of them get lost. When in the same slot n packets leave the FDL-structure (with probability $r_N(n)$), and $n - l_2$ of them can be transmitted (with probability $\hat{a}_{M-m+l_1}(n - l_2|n)$, since there are $M - m + l_1$ not yet occupied outlets), l_2 of the n packets leaving the FDL-structure cannot be transmitted and are thus lost. This leads to expression (10).

For the following figures, we assume again a Bernoulli arrival process at the inlets of the switch, i.e., at every inlet a packet arrives with probability λ and no packets arrive with probability $1 - \lambda$ at slot boundaries. In Fig. 9, we have shown the PLR as a function of the arrival rate λ, when $M = 6$ and $N = 0, \ldots, 3$ respectively. Without delay lines in the switch ($N = 0$), the PLR is the same as in Fig. 5 (no delay lines). When $N = 1$, the PLR is reduced significantly (but less than in the switch with dedicated FDL's). Adding at every output one more delay line ($N = 2$), lowers the PLR even more, but adding more delay lines, does not have a significant effect (as for the switch with dedicated FDL's). Comparing Figs. 5 and 9, we see that the PLR is a bit lower for the switch with dedicated delay lines, but not significantly. Furthermore, the higher N the closer the PLR's for both cases. You need however $M = 6$ times more FDL's for the switch with dedicated FDL's. So, if the number of FDL's is the crucial design factor, the switch with shared FDL's is the best choice.

In Fig. 10, the PLR is shown when N varies, $M = 6$ and $\lambda = 0.1, 0.5, 0.75, 0.9$ and 1 respectively. As expected the PLR is again strongly related to the arrival rate λ, i.e., to the load that is offered to the switch. This figure also shows that making the number of delay lines larger than 3 does not give much advantage.

5. Conclusions

We have analysed an FDL-structure with N delay lines of increasing lengths. Such an FDL-structure is promising for being used in future optical packet switches. We used a

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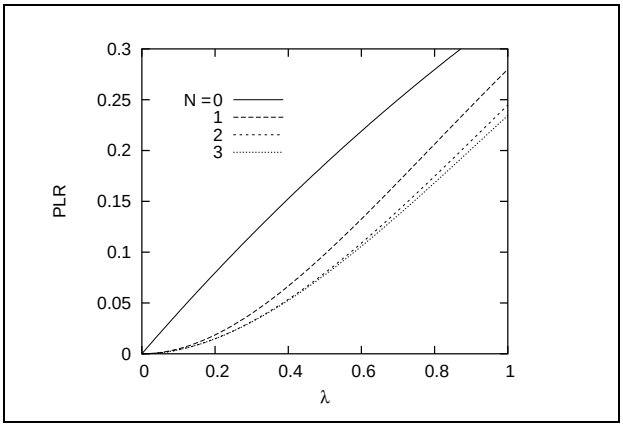

Fig. 9. PLR versus the arrival rate when the number of inlets M is 6.

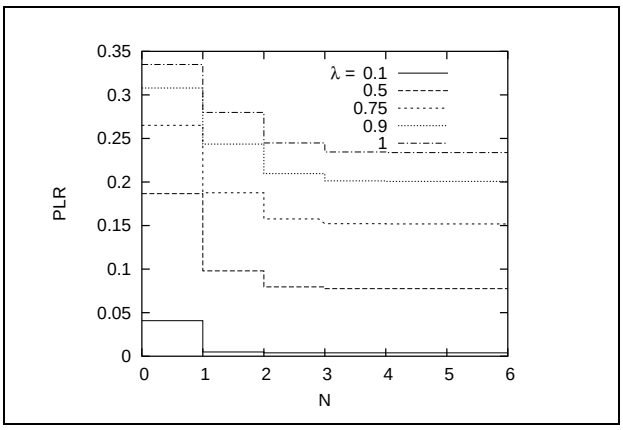

Fig. 10. PLR versus the number of delay lines when the number of inlets M is 6.

generating-functions approach in order to assess some important performance measures of such an FDL-structure. We have furthermore used the obtained results to calculate the packet loss rate in two types of optical packet switches, i.e., switches with dedicated or shared output queueing respectively. The results showed that more intelligent scheduling techniques than smallest FDL-first are needed to adequately use the FDL's. On the other hand, smallest delay line first is the easiest implementable scheduling discipline. Furthermore, we have shown that in a switch with a shared FDL-structure approximately the same PLR can be obtained as in a switch with dedicated FDL's, but with considerably less FDL's.

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