

Quadrature Mismatch Shaping Techniques for Fully Differential Circuits

Stijn Reekmans, Pieter Rombouts and Ludo Weyten

Ghent University (UGent), Dept. ELIS
Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium
Email: Stijn.Reekmans@ELIS.UGent.be

Abstract—Quadrature $\Sigma\Delta$ ADCs require a feedback path for both the I and the Q part of the complex feedback signal. A complex DAC could give this feedback with near-perfect I/Q balance. Still, the mismatch between the unit elements of the complex DAC introduces mismatch noise that should be shaped out of the signal band with dynamic element-matching (DEM) techniques. In literature, only quadrature DEM techniques for 3-state (I, Q, 0) unit elements are considered. However, in fully differential circuit, also 5-state unit elements are available. In this case, each unit element can be selected $\pm I$, $\pm Q$ or 0. When using these 5-state unit elements, the amount of hardware and power consumption can be reduced significantly. In this paper it is shown how the tree structure, the data directed swapper and the vector quantizer structure can be adapted for the use in fully differential circuits with such 5-state unit elements.

I. INTRODUCTION

In low-IF receivers, quadrature bandpass (QBP) $\Sigma\Delta$ modulators provide interesting advantages over a pair of real bandpass $\Sigma\Delta$ modulators [1]. Such a QBP $\Sigma\Delta$ modulator takes in a complex analog input and produces a complex digital output which represents the complex input within a narrow bandwidth. As such, it performs complex analog-to-digital conversion. Complex signals are a convenient representation of a pair of real signals. One signal is interpreted as the real part and the other signal as the imaginary part of the combined complex signal.

Whereas traditional $\Sigma\Delta$ modulators employed 1-bit quantization, multibit $\Sigma\Delta$ ADCs achieve a higher resolution and alleviate stability problems [2], [3]. However, multibit DACs are not inherently linear since they suffer from mismatch between the DAC elements. Furthermore, most of the QBP $\Sigma\Delta$ modulators are using two separate feedback DACs, one real DAC for the feedback of the in-phase (I) path, another one for the quadrature (Q) path. In this situation, the mismatch results in a non-linear error, called DAC mismatch noise, and in path mismatch between the I- and Q-path. This path mismatch causes both the input signal and the quantization noise in the image band to fold into the desired signal band. For QBP modulators this is highly unwanted since quantization noise is not attenuated in the image band [4]–[6].

An interesting approach, to solve the problem related to path mismatch, is to merge the two real DACs into one complex multibit DAC structure [5]–[7]. The block diagram of such a complex DAC looks very similar to its real counterpart and

is shown in Fig. 1. It consists of an element selection logic (ESL) which addresses the N unit elements. The task of the ESL is to map each complex input sample $x[n]$ to complex selection signals $x_i[n]$ such that the sum of the N selection signals equals $x[n]$.

Until now, these complex DACs were derived for the case of single-ended circuits. Here each unit element can be selected in three different ways, therefore it is called a 3-state unit element. If the selection signal $x_i=1$, the unit element is selected 'I' and gives a feedback signal to the I-path. When $x_i=j$, the unit element is selected 'Q' and gives a feedback signal to the Q-path and when $x_i=0$, the unit element is unselected and generates no feedback signal.

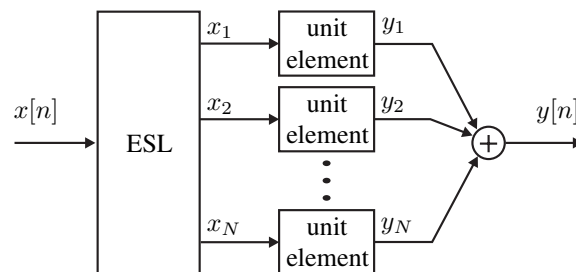


Fig. 1. A complex multibit DAC with ESL.

Next, we will introduce the concept of 5-state unit elements and show why this has a lot of advantages when used in fully differential circuits. The remaining problem of DAC mismatch noise should be reduced by using quadrature mismatch shaping techniques like [5]–[7]. In section III, the tree structured ESL and the data-directed swapper ESL will be adapted for 5-state unit elements. In section IV, we discuss how the vector quantizer structure needs to be altered to be adapted for 5-state unit elements. Finally, the effectiveness of the proposed techniques is confirmed by simulations.

II. FULLY DIFFERENTIAL CIRCUITS

Today most high-performance circuit implementations are fully differential [3]. Here, a straightforward complex unit element has 5 states. This is understood because each unit element can now be selected $\pm I$ or $\pm Q$ or not selected at all. The selection signals $x_i[n]$ would then be ± 1 , $\pm j$ or 0. An implementation of such a 5-state unit element, together

with the input stage of a complex $\Sigma\Delta$ modulator, could look as in Fig. 2(a). Here, the unit element consists of the combined blue (pmos) and the yellow (nmos) current source. For a DAC with four 5-state unit elements, the differential feedback DAC current I_D can be equal to $I_D^I + jI_D^Q$ with $I_D^I, I_D^Q \in [4, 2, 0, -2, -4]I_d$. The total current consumption in this situation is $4 \times 2I_d = 8I_d$.

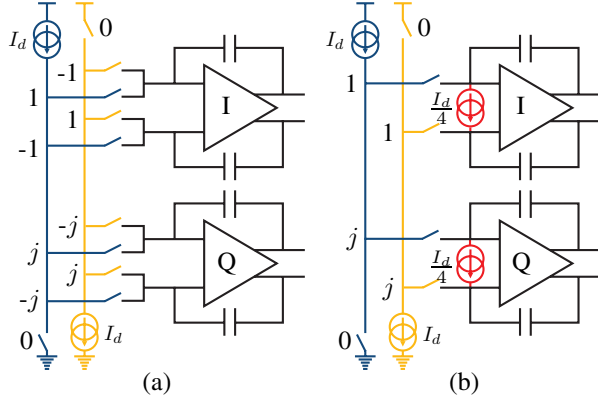


Fig. 2. Implementation of (a) a 5-state and (b) a 3-state unit element, together with the input stage of the $\Sigma\Delta$ modulator.

To be able to give the same feedback currents as with four 5-state unit elements, eight 3-state unit elements are necessary. The three states $[1, j, 0]$ need to be mapped to a differential feedback DAC current so that the DC-component is zero. If the DAC needs to return a zero differential current, two unit elements will be selected 'I', two 'Q' and four elements remain unselected. The following differential feedback DAC currents will result in such a zero DC-component:

$$\begin{aligned} 1 &\rightarrow (+1.5 - 0.5j) I_d \\ j &\rightarrow (-0.5 + 1.5j) I_d \\ 0 &\rightarrow (-0.5 - 0.5j) I_d \end{aligned} \quad (1)$$

A 3-state unit element, together with the input stage of the $\Sigma\Delta$ modulator, could look as in Fig. 2(b). The constant (non switched) current sources (red) are needed to set the required DC-level. As can be concluded from the figure, each unit element consumes $2I_d$ resulting in a total current consumption of $8 \times 2I_d = 16I_d$. Comparing this with the situation for 5-state elements (see above), we conclude that the power consumption of the DAC itself is doubled when using 3-state elements.

So, if 5-state unit elements were used instead of 3-state unit elements, only half the amount of unit elements would be required. This results in a simplified layout of the analog part which can be routed more efficiently. Furthermore, as will be shown in the following sections, the use of the 5-state unit element also results in a reduced complexity of the ESL. However, until now all complex DEM techniques consider only 3-state unit elements. In this paper, we will introduce complex DEM techniques for 5-state unit elements.

III. TREE STRUCTURE AND DATA-DIRECTED SWAPPER

A. Structure

In Fig. 3, the tree structured DAC [2] and in Fig. 4 the data-directed swapper DAC [8] are shown for a DAC with four unit elements. Both techniques can easily be generalized to any number $N=2^b$ of unit elements. The ESL consists of b (2 in Fig. 3 and Fig. 4) layers of cells $S_{k,r}$, where k and r denote the layer number and the position within the layer, respectively. The number of cells is equal to $N-1$ for the tree structure and $N/2 \log_2(N)$ for the swapper [3]. As will become clear next, the complexity of a cell is similar for the case of 3-state and 5-state unit elements. This means that the digital hardware is roughly halved in the case of 5-state compared to 3-state unit elements since the amount of elements is halved.

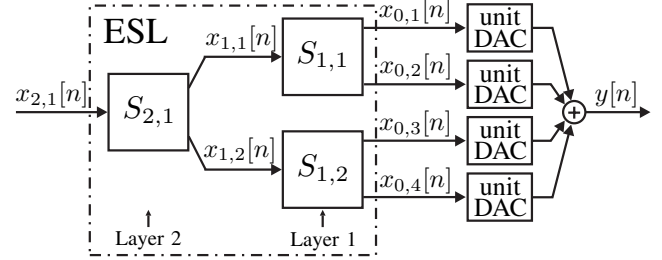


Fig. 3. Tree structure of a complex, mismatch shaping DAC

For a tree structured DAC, these cells are called switching blocks. Each switching block $S_{k,r}$ has a single input $x_{k,r}[n]$, a top output $x_{k-1,2r-1}[n]$ and a bottom output $x_{k-1,2r}[n]$. The input/output relationship of the switching block $S_{k,r}$ is given by:

$$\begin{aligned} x_{k-1,2r-1}[n] &= \frac{1}{2}(x_{k,r}[n] + s_{k,r}[n]) \\ x_{k-1,2r}[n] &= \frac{1}{2}(x_{k,r}[n] - s_{k,r}[n]) \end{aligned} \quad (2)$$

where $s_{k,r}[n]$ is the switching sequence. Note that the sum of the two outputs equals the input.

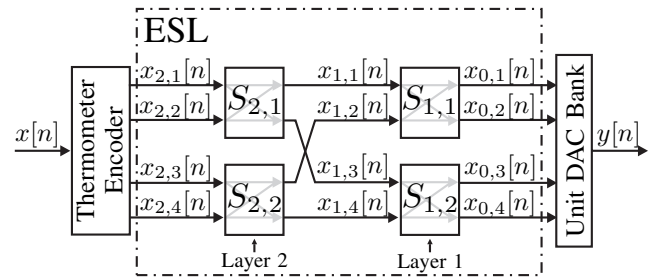


Fig. 4. Data-directed swapper structure of a complex, mismatch shaping DAC.

For a data-directed swapper DAC, the cells are called swapper cells. The behavior of the swapper cell is based on the swapper sequence $s_{k,r}[n]$. This sequence is defined as the difference between the two outputs. To illustrate this, the input/output relationship of swapper cell $S_{1,1}$ is given by:

$$\begin{aligned} x_{0,1}[n] &= \frac{1}{2}(x_{1,1}[n] + x_{1,2}[n] + s_{1,1}[n]) \\ x_{0,2}[n] &= \frac{1}{2}(x_{1,1}[n] + x_{1,2}[n] - s_{1,1}[n]) \end{aligned} \quad (3)$$

As shown in [2], the DAC mismatch error is a linear combination of the switching (swapper) sequences $s_{k,r}[n]$. So, if each switching (swapper) sequence is calculated as a K^{th} order shaped sequence that is uncorrelated with the sequences of the other switching blocks (swapper cells), then the DAC error will be a K^{th} order shaped sequence as well.

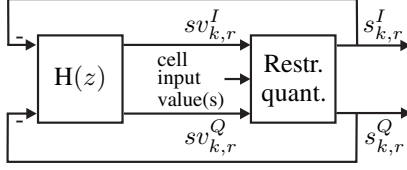


Fig. 5. QBP shaper with restricted quantizer.

The QBP shaped switching (swapper) sequences are obtained from a QBP shaper, shown in Fig. 5. Essentially, it consists of a digital domain QBP $\Sigma\Delta$ modulator with no input signal, where the two quantizers are replaced by one restricted quantizer. The restricted quantizer tries to track its inputs ($sv_{k,r}^I[n], sv_{k,r}^Q[n]$) while forcing its outputs ($s_{k,r}^I[n], s_{k,r}^Q[n]$) to fulfill certain constraints. These constraints are required to result in a correct functioning and will be discussed next. The complex loopfilter $H(z)$ ensures that this additive error is shaped.

B. Constraints for the tree structured DAC

In [5], [6] a set of constraints for $s_{k,r}[n]$ were presented in case of a complex DAC with 3-state unit elements. In this section the required constraints in case of 5-state unit elements are derived.

To ensure that the outputs of the switching blocks are integer numbers after the division by two in eq. (2), the following two constraints need to be fulfilled:

$$s_{k,r}^I[n] = \begin{cases} \text{even} & \text{if } x_{k,r}^I[n] \text{ is even} \\ \text{odd} & \text{if } x_{k,r}^I[n] \text{ is odd} \end{cases} \quad (4)$$

$$s_{k,r}^Q[n] = \begin{cases} \text{even} & \text{if } x_{k,r}^Q[n] \text{ is even} \\ \text{odd} & \text{if } x_{k,r}^Q[n] \text{ is odd} \end{cases} \quad (5)$$

These constraints are the same for a DAC with 3-state or with 5-state unit elements.

For DACs with 3-state unit elements, the number conservation rule stated that both the real and imaginary part as well as the sum of real and imaginary part of the two outputs of each switching block must be in the range of $\{0, 1, \dots, 2^{k-1}\}$. For DACs with 5-state unit elements it should be in the range of $\{-2^{k-1}, \dots, -1, 0, 1, \dots, 2^{k-1}\}$. As a result, the constraints arising from the number conservation rule will be different for DACs with 5-state unit elements from those for DACs with 3-state unit elements:

$$\begin{aligned} |s_{k,r}^I[n]| &\leq 2^k - |x_{k,r}^I[n]| \\ |s_{k,r}^Q[n]| &\leq 2^k - |x_{k,r}^Q[n]| \end{aligned} \quad (6)$$

as the substitution for eq. (15) in [6] and

$$|s_{k,r}^I[n] \pm s_{k,r}^Q[n]| + |x_{k,r}^Q[n] \pm s_{k,r}^Q[n]| \leq 2^k \quad (7)$$

for eq. (16) in [6]. Note that eq. (7) implies eq. (6).

For layer-1 switching blocks, the switching sequence constraints could be summarized as followed:

$$s_{1,r}[n] = \begin{cases} 0 & \text{if } x_{1,r}[n] \text{ is } 0, \pm 2 \text{ or } \pm 2j \\ \pm 1 & \text{if } x_{1,r}[n] \text{ is } \pm 1 \\ \pm j & \text{if } x_{1,r}[n] \text{ is } \pm j \\ \pm(1-j) & \text{if } x_{1,r}[n] \text{ is } \pm(1+j) \\ \pm(1+j) & \text{if } x_{1,r}[n] \text{ is } \pm(1-j) \end{cases} \quad (8)$$

For all other layers, the implementation of the combined constraints, in their most general form, is rather hardware expensive. Therefore, the following simplified constraints may be used:

$$\begin{aligned} s_{k,r}^I[n] &= \begin{cases} 0 & \text{if } x_{k,r}^I[n] \text{ is even} \\ \pm 1 & \text{if } x_{k,r}^I[n] \text{ is odd} \end{cases} \\ s_{k,r}^Q[n] &= \begin{cases} 0 & \text{if } x_{k,r}^Q[n] \text{ is even} \\ \pm 1 & \text{if } x_{k,r}^Q[n] \text{ is odd} \end{cases} \end{aligned} \quad (9)$$

These constraints are more restrictive than necessary but they simplify the hardware of the switching block significantly.

C. Constraints for the data-directed swapper DAC

If we merge the two inputs of the swapper cell into one new input which is equal to the sum of its original inputs, then the swapper cell has the same functionality as a layer-1 switching block. As a result, the constraints for the data-directed swapper DAC could be directly derived from the ones for the tree structured DAC. If we set $x_{1,r}[n]$ of (8) equal to $x_{k,2r-1}[n] + x_{k,2r}[n]$, then the constraints for the data-directed swapper DAC are obtained.

IV. VECTOR QUANTIZER STRUCTURE

Another way to implement an ESL with QBP shaping is the vector quantizer structure of [7]. Just as in [6], this structure was presented for single-ended complex unit elements (3-state). Next, we will adopt it toward 5-state elements.

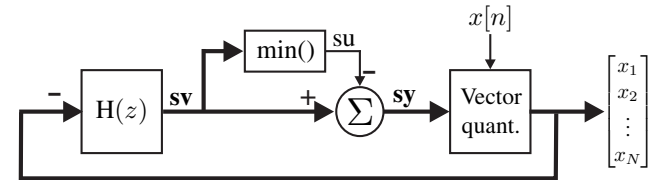


Fig. 6. Vector quantizer based element selection logic.

The block diagram of the vector quantizer structure is shown in Fig. 6. Here, a vector notation $[x_1, x_2, \dots, x_N]$ is used for the selection signals. The nonlinear block 'vector quant.' ensures that the sum of the N selection signals $x_i[n]$ equals $x[n]$. The vector control loop, together with the complex loopfilter $H(z)$, ensures that the error, introduced by the vector quantizer, is shaped. Finally, the $\min()$ -block, which generates $su = \min(sv^I) + j\min(sv^Q)$, is added to keep the input of the vector quantizer \mathbf{sy} bounded [7].

The 5-state vector quantizer is implemented by sorting the elements of \mathbf{sy} . When $x^I[n]$ ($x^Q[n]$) is positive, the highest

selection priority should be given to the elements with the largest sy_i^I (sy_i^Q). The $x^I[n]$ ($x^Q[n]$) selected unit elements will return +1 (+j). When $x^I[n]$ ($x^Q[n]$) is negative, it should be given to the ones with the smallest sy_i^I (sy_i^Q). In this case, the $|x^I[n]|$ ($|x^Q[n]|$) selected unit elements will return -1 (-j). If not selected they will return 0. Of course, it should be ensured that no element is selected for the I-path as well for the Q-path. Therefore, we suggest to alternate between the following strategies:

- 1) Start with the selection of an element for the I-path, then one for the Q-path, then again one for the I-path,.... until no more unit elements need to be selected.
- 2) Start with the selection of an element for the Q-path, then one for the I-path, then again one for the Q-path,.... until no more unit elements need to be selected.

In this case, we toggle between the preferential treatment of the two paths so that, on average, neither the I- or the Q-path is preferred. As a result, the I and Q signals are treated in exactly the same way and will not suffer from path mismatch.

Since the amount of hardware for the sorting operation in the vector quantizer is proportional to $N \log_2 N$, the complexity is even more than halved when using a DAC with 5-state unit elements [3].

V. SIMULATIONS

To illustrate the effectiveness of the proposed approach, simulations for the case of first order $f_s/4$ mismatch shaping were performed. The first order $f_s/4$ QBP shaper of [5], [6] can be used to obtain the switching (swapper) sequences. For this structure, it can be proven that, also in the 5-state case, it is possible to have the state variables ($sv_{k,r}^I[n]$, $sv_{k,r}^Q[n]$) bounded to $\{-2, -1, 0, 1, 2\}$ for swapper cells and layer-1 switching blocks and to $\{-1, 0, 1\}$ for the other layers in the tree structure.

A complex DAC bank with 8 unit elements was used as a test structure. The 8 unit elements were assigned a zero-mean random mismatch with a standard deviation σ of 1%. The same set of mismatches was used as in [6].

Fig. 7 shows a typical selection pattern which results from such a complex ESL with 5-state unit elements. It shows which of the 8 unit elements are selected ‘ $\pm I$ ’, ‘ $\pm Q$ ’ or remain unselected: e.g. element 2 is respectively selected ‘+I’, unselected, ‘-Q’, ‘+Q’ and ‘-I’ in the first five time steps. Fig. 8 shows the DAC noise spectrum in case of a tree structured ESL for 5-state unit elements. The other ESLs give similar results and are therefore omitted.

VI. CONCLUSION

This paper presents quadrature bandpass mismatch shaping techniques for a DAC with 5-state unit elements. This is important because these 5-state unit elements are readily available in fully differential circuits. It was shown that the use of 5-state instead of 3-state unit elements, reduces the power consumption with a factor 2. Also, the required number of unit elements is halved. As a result the complexity of the digital element selection logic is roughly halved. Next,

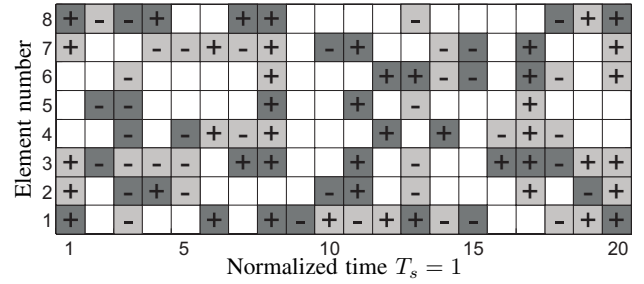


Fig. 7. Element selection pattern, light gray = selected ‘I’, dark gray = selected ‘Q’ and white = unselected.

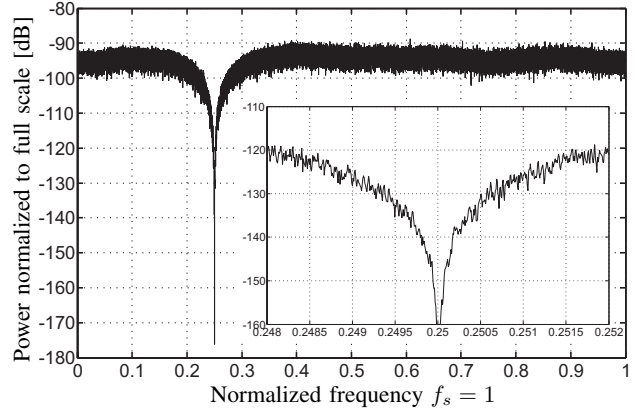


Fig. 8. DAC error spectrum (12 times averaged 128K FFT) (overview and detail)

it has been shown how quadrature dynamic element-matching techniques for 3-state elements, such as the tree structure, the data directed swapper and the vector quantizer structure, could be adapted for the use in fully differential circuits with 5-state unit elements.

ACKNOWLEDGMENT

S. Reekmans is supported by the Special Research Fund of Ghent University.

REFERENCES

- [1] S. Jantzi, K. Martin, and A. Sedra, “Quadrature Bandpass $\Delta\Sigma$ Modulation for Digital Radio,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, 1997.
- [2] I. Galton, “Spectral Shaping of Circuit Errors in Digital-to-Analog Converters,” *IEEE Trans. Circuits Syst. II*, vol. 44, no. 10, pp. 808–817, 1997.
- [3] P. Rombouts and L. Weyten, “A Study of Dynamic Element-Matching Techniques for 3-Level Unit Elements,” *IEEE Trans. Circuits Syst. II*, vol. 47, no. 11, pp. 1177–1187, 2000.
- [4] R. Maurino and C. Papavassiliou, “Multibit Quadrature Sigma-Delta Modulator with DEM Scheme,” in *IEEE International Symposium on Circuits and Systems, ISCAS*, 2004.
- [5] S. Reekmans, J. De Maeyer, P. Rombouts, and L. Weyten, “Quadrature Mismatch Shaping with a Complex, Tree Structured DAC,” in *IEEE International Symposium on Circuits and Systems, ISCAS*, 2006.
- [6] —, “Quadrature Mismatch Shaping for Digital-to-Analog Converters,” *IEEE Trans. Circuit Syst. I*, vol. 53, no. 12, pp. 2529–2538, 2006.
- [7] R. Schreier, “Quadrature Mismatch-Shaping,” in *IEEE International Symposium on Circuits and Systems, ISCAS*, 2002.
- [8] T. Kwan, R. Adams, and R. Libert, “A Stereo Multibit $\Sigma\Delta$ DAC with Asynchronous Master-Clock Interface,” *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1881–1887, 1996.