Fully Equipped Half Bridge Building Block for Fast Prototyping of Switching Power Converters

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***Abstract*— With the advent of high performance digital controllers, the time and effort to implement new control algorithms for the control of power electronic converters have decreased drastically. Nevertheless, the design and the practical implementation of power electronic converters, intended for testing new control algorithms, are still complicated and time consuming activities. Therefore, a fully equipped half bridge test platform was designed ready to use as a fundamental building block for various converter types. The test platform incorporates fault protection, measurements of well-selected voltages and currents, and is directly interfacable with most digital and analog controllers. Due to these features and the flexibility of the board, this half bridge converter can be used for research as well as for educational purposes in applications ranging from a simple 100 W buck converter up to 10 kW inverters for motor control. The platform is demonstrated in this paper by means of some basic converter topologies, the half bridge boost converter and the full bridge buck converter.**

I. Introduction

With the advent of high performance digital controllers, the time and effort to implement new control algorithms for the control of power electronic converters have decreased drastically. This is demonstrated by the large amount of papers concerning digital control of power electronic converters in a wide range of applications, inverters and motor control applications [1], [2], [11], active filters [3], [4], and power factor correction converters [5]–[7]. Nevertheless, the design and the practical implementation of power electronic converters, intended for testing new control algorithms, are still complicated and time consuming activities.

Therefore, a fully equipped half bridge test platform was designed ready to use as a fundamental building block for various converter types. It offers great flexibility to implement several topologies, one-phase or three-phase rectifiers, inverters, a large number of basic DC-DC converters, by building one or more of these modules together with some passive components and a controller. The platform provides the measurement of some well-selected voltages and currents, and offers an easy interface with analog or digital controllers. Moreover, it incorporates a complete fault protection system, including overvoltage, overcurrent and high temperature detection and allows interaction between the fault protection system of all connected modules and the controller. Due to these features and the flexibility of the board, this half bridge converter is very suitable to be used in laboratory environments as well as for educational purposes in applications ranging from a simple 100 W buck converter up to 10 kW inverters for motor control.

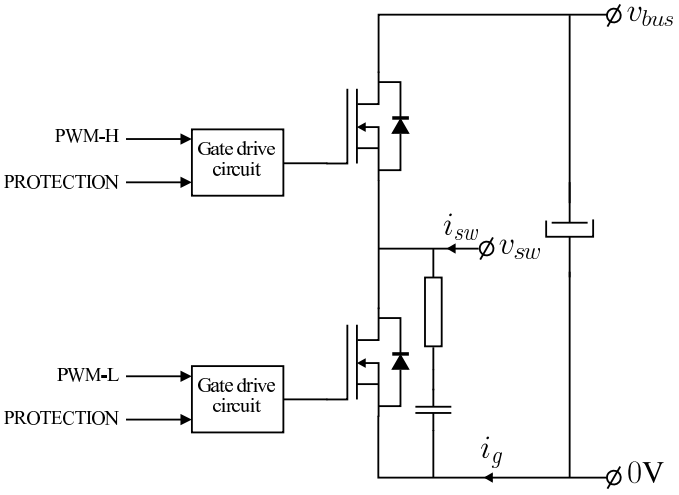

Fig. 1. Power stage of the half bridge test platform

This paper offers a detailed description of the entire board, including the power stage, the measurement equipment, the fault protection system and the interface with other modules and with the controller. In order to demonstrate the use of this platform in a practical realization, two experimental setups using this building block are demonstrated: a half bridge boost converter, based upon one platform, and a full bridge buck converter using two interconnected platforms.

II. Description of the Power Stage

The power stage consists of a half bridge topology containing two switches, as depicted in Fig. 1. It can be connected with other modules or passive components through three connectors which will be referred to as v_{bus} for the bus voltage, v_{sw} for the interconnection pin of the two switches, and 0V for the ground connection. The platform provides a bus capacitor between v_{bus} and 0V, while a snubber between v_{sw} and 0V terminals is used to prevent high frequent oscillations which may appear on the switch voltage [8].

The maximum bus voltage is limited by the design to 1

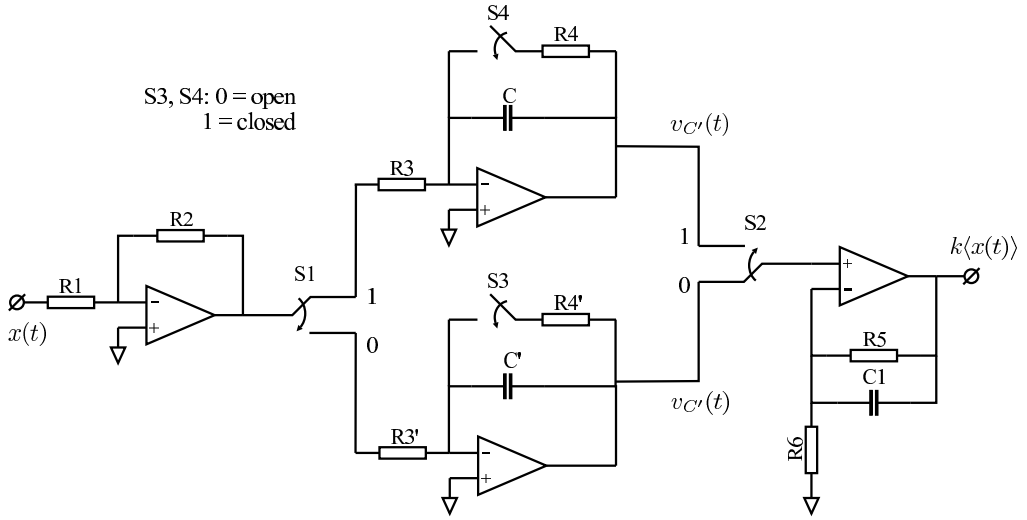

Fig. 2. Integrating circuit, used for measurement of the switch voltage v_{sw}

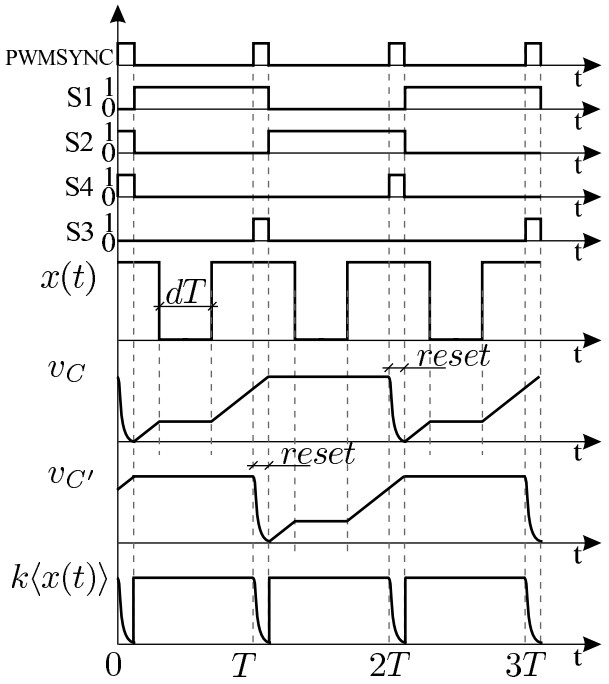

Fig. 3. Key waveforms of the integrating circuit for typical switch voltage waveform input

kV, but is in most cases determined by the choice of the switches and the bus capacitor. Depending on the requirements of switching frequency f_s and current rating, most discrete-packaged MOSFETs, IGBTs or even diodes may be employed for the switches. This makes the platform suitable for a broad range of applications.

III. Measurement Equipment

A. Averaging circuit for the switch voltage

For applications such as Inductor Voltage Control (IVC) for active rectifiers [9], or control of the output voltage for inverters and motor drives [10]–[12], it is useful to sense the average switch voltage $\langle v_{sw}\rangle$. This can be accomplished by integrating the switch voltage v_{sw} during one PWM cycle. Therefore, the integrating circuit of Fig. 2 is applied. This circuit consists of two parallel integrator circuits, connected alternately to the input and the output amplifier of the entire averaging circuit. When an integrator is connected to the input amplifier, it will integrate the signal $-\frac{R_2}{R_1}x(t)$, supplied at its input, yielding

$$v_C(T) = \frac{R_2}{R_1}\frac{T}{R_3C}\langle x(t)\rangle \tag{1}$$

at the end of a switching period T. During the next switching cycle, the output voltage of this integrator remains constant as no signal is connected to its input. This allows to provide a constant signal, proportional to the average of the switch voltage, at the output of the averaging circuit. At the end of this second switching cycle, the integrator is reset by closing switch $S3$ (or switch $S4$). Since the capacitor voltage will decrease exponentially

$$v_C(t) = v_C(0)exp(-\frac{t}{R_4C}), \tag{2}$$

the resetting switch should be closed during a time

$$T_{res} \geq 4R_4C \tag{3}$$

in order to allow the capacitor voltage to fall below 2% of its value. This time can be programmed by changing the length of the pulses applied on the PWMSYNC-input of the platform. Since this reset takes place during the interval where the corresponding integrator is connected to the output amplifier, the reset of the signal will be visible in the output of the averaging circuit. However, since the averaging interval lasts exactly one switching cycle, the averaged value is not affected by the reset.

The switching signals for all switches $S1$ to $S4$ are all derived from the PWMSYNC-signal by on-board logic. In order to yield correct averaging of the switch voltage, the PWMSYNC-signal must be synchronized with the switching of the power module, while the length of the pulses must meet (3). Most digital signal processors provide a signal that can be used for this purpose.

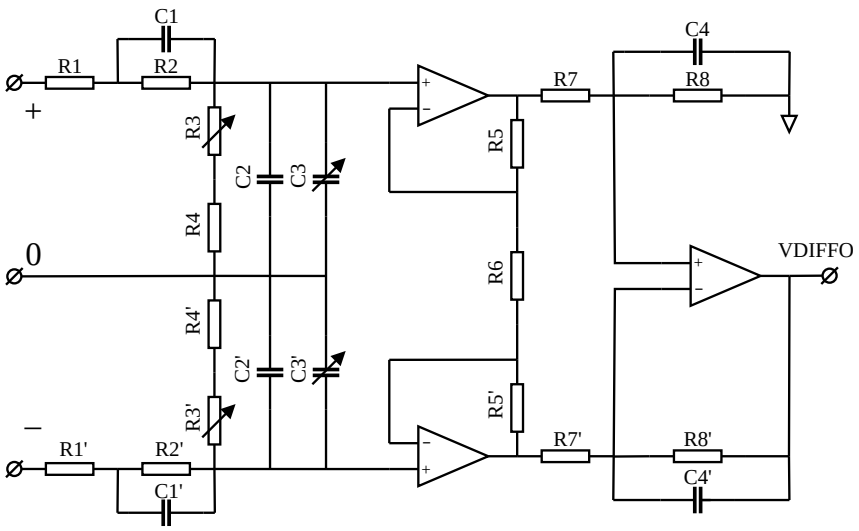

Fig. 4. Circuit of the differential voltage measurement

B. Switch current and bus voltage measurement

The electronic circuit required for the measurement and the amplification of the bus voltage v_{bus} and the current i_{sw} both use standard opamp circuits. The bus voltage is sensed by a high voltage, high ohmic voltage divider, using a very high voltage cermet plate resistor of 10 MΩ. this voltage divider is followed by two inverting opamp-based amplifiers. Additionally, some circuitry is provided to quickly change the gain and the offset of these amplifiers, so that an accurate measurement in a narrow band around an adjustable setpoint can be achieved.

For the sensing of the current i_{sw}, a LEM LTS-15NP current transducer is employed. The output of this current transducer contains a 2.5 V offset, which is compensated in a first opamp circuit, after which a second amplifier provides the required voltage range for the output signal.

C. Differential amplifier

Since the control of converters may require sensing of voltages outside the test platform, this platform is equipped with a differential amplifier. This amplifier, presented in [13], is capable of sensing high-frequency, high-voltage signals, with a high bandwidth (2 MHz) and very good common-mode rejection (-60 dB at 1000 V/μs). The circuit is displayed in Fig. 4. The inputs ($+$ for the non-inverting input, and $-$ for the inverting input) are first scaled down by a resistive-capacitive voltage divider. Both the input resistor network and the input capacitor network are trimmable, in order to allow fine tuning of the low-frequency and high-frequency gain. A high bandwidth of the amplifier with a constant gain up to high frequencies is only achieved when the time constants of the resistor-capacitor networks match

$$R2 \cdot C1 = (R3 + R4) \cdot (C2 + C3)\,. \tag{4}$$

In that case the pole and the zero of the input voltage divider are cancelled, and the bandwidth of the amplifier is limited by the time constant of $R1$ with $C1$.

In order to obtain a high common mode rejection, both networks $\{R1 - R4/C1 - C3\}$ and $\{R1' - R4'/C1' - C3'\}$ must have the same characteristics, which can be achieved by adjusting the trimmable resistor $R3'$ and the trimmable capacitor $C3'$.

After the first division of the inverting and the non-inverting input, the differential signal is send towards an output amplifier, which determinates the gain of the total amplifier by the choice of the ratio $\frac{R7}{R8} = \frac{R7'}{R8'}$.

IV. Fault Protection Circuit

As the platform is intended to be used for educational purposes or for experimental verification of new control strategies in research environments, some important overloads or short circuits can be expected to occur during the use of this platform. These errors could be caused by unintentional short circuits, errors in the implemented control algorithm, or wrong connections in the setup of the converter. Therefore, to guarantee safe operation of the platform under these conditions, a full fault protection system was elaborated. This system will shut down the converter when one of the protected quantities, the current i_{sw} through the v_{sw}-connector, the current i_g through the 0V-connector, the bus voltage v_{bus}, and the temperature of the switches, exceeds its threshold. Except for the switch temperature, all thresholds are programmable. The excess of one threshold will clear the protection signal EXTPROT (the output of a flip-flop), thus inhibiting further switching of the converter, see Fig. 5. When all quantities have returned into their safe operation ranges, the platform can be restarted by means of a push button or remotely by an external trigger signal (EXTRESET).

For applications where several modules are interconnected, the platform offers the option to connect the protection signal (EXTPROT) to the protection system of other modules. Hence, each block will stop switching when an error occurs in one of the interconnected blocks. Nevertheless, in order to allow startup of the entire system, the external protection system cannot trigger the protection signal of the block.

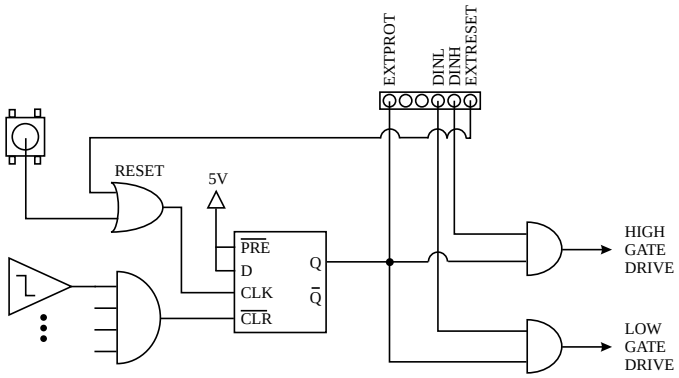

Fig. 5. Schematic representation of the fault protection circuit of the test platform

V. Supply of the Peripheral Equipment

For the sensing, amplification and protection systems, and for the supply of the gate drive circuits, the platform requires a dual ± 15 V supply voltage. From this main supply voltage, several voltage levels are derived on-board:

- ± 15 V: is used for the supply of all operational amplifiers on the platform and for the comparators used for the fault protection
- 15 V: is decoupled from the first 15 V to supply the low side gate drive.
- 12 V: is required to supply the high side gate drive with an isolated NME1215 DC-DC converter.
- 5 V: is required for the supply of the current transducer.
- ± 5 V: (or ± 3.3 V): supplies all logic components required for the fault protection circuit, and for the control signals of the analog switches of the integrating circuit.

The choice between ± 5 V and ± 3.3 V depends on the operating voltages of the controller. Since a lot of new digital signal processors (DSPs), such as ADSP2199X of Analog Devices or TMS320C2XX of Texas Instruments, use a 3.3 V interface, instead of 5 V for older DSPs such as the ADMC401 of Analog Devices, all logic components interfacing with the DSP should be supplied either with 3.3 V or with 5 V. Therefore, an on-board, adjustable voltage regulator is provided, allowing to choose the voltages according to the requirements of the controller.

VI. Experimental Results

A. Example topology: boost converter based upon one platform

The platform was tested using a boost topology, see Fig. 6, with following parameters

$$\begin{cases} \text{inductance} & L = 1\text{mH}, & \text{input voltage} & V_{in} = 200\text{V}, \\ \text{capacitance} & C = 470\mu\text{F}, & \text{load} & R = 720\Omega, \\ \text{switching frequency} & f_s = 50\text{kHz}, & \text{duty-ratio} & D = 0.5. \end{cases} \tag{5}$$

The key converter waveforms are shown in Fig. 7. The upper trace shows the switch voltage measured by the differential amplifier provided on the platform, while the lower trace depicts the inductor current, sensed by the current transducer of the platform.

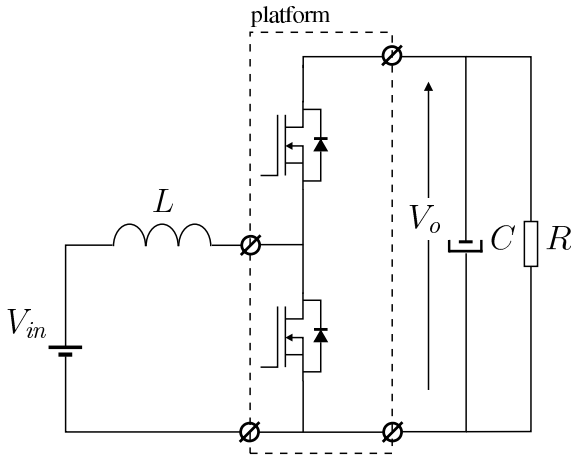

Fig. 6. Topology of a boost converter based upon the test platform

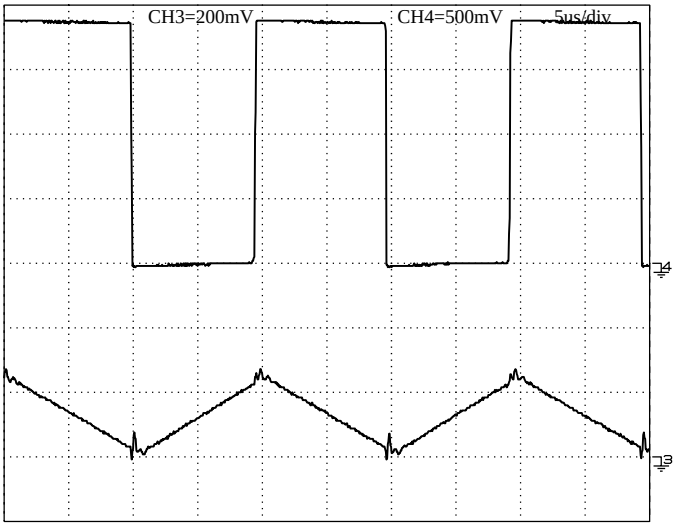

Fig. 7. Waveforms of the test platform employed as boost converter, upper trace: switch voltage sensed by the differential amplifier, lower trace: inductor current measurement

B. Testing of the peripheral equipment

In Fig. 7, some experimental waveforms of the measurement equipment, the differential amplifier and the switch current measurement, were already shown. The operation of the differential amplifier and the integration of the switch voltage are demonstrated in Fig. 8. The two upper curves show the response of the differential amplifier to a typical switching waveform of a converter, a square wave with an amplitude of 390 V and a switching frequency of 50 kHz. The choices for the passive components (Fig. 4) are

$$\begin{cases} R1 = 2.7\ k\Omega & R2 = 10\ M\Omega & R3 + R4 = 50\ k\Omega \\ C1 = 5\ pF & R5 = 1\ k\Omega & C2 + C3 = 1\ nF \\ R7 = 2\ k\Omega & R8 = 1\ k\Omega & C4 = 10\ pF \end{cases} \tag{6}$$

thus leading to a total attenuation by a factor 200, which can be observed on the upper trace of Fig. 8, where the

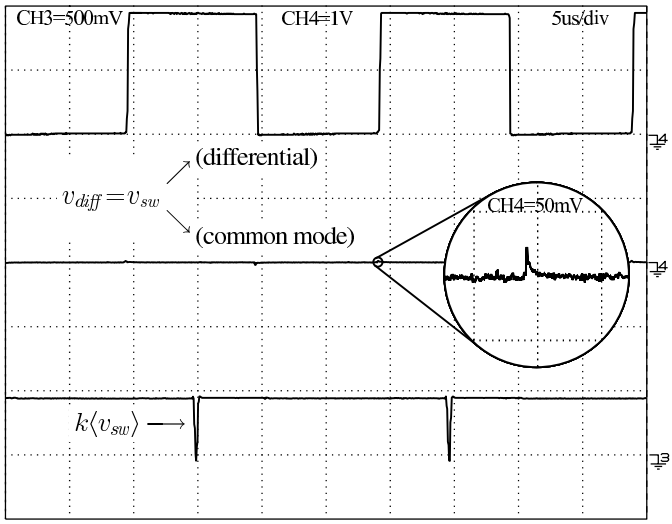

Fig. 8. black traces: output of the differential amplifier with a differential and with a common mode input voltage, gray trace: output of the integrating circuit

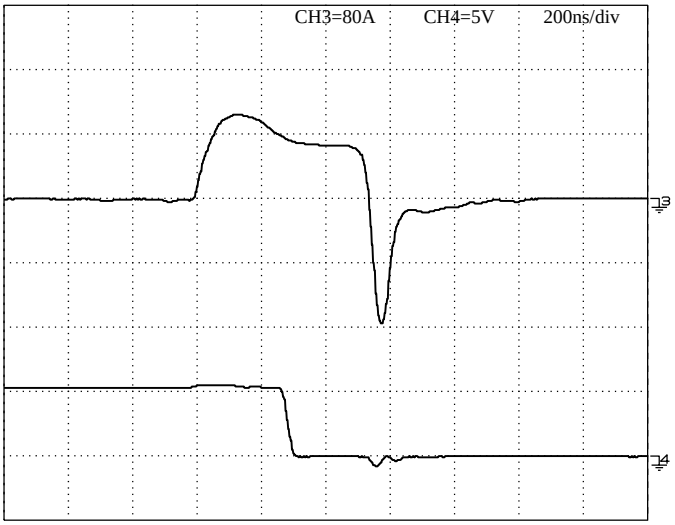

Fig. 10. Test of the fault protection circuit. Upper trace: short circuit current, Lower trace: reaction of the EXTPROT-signal

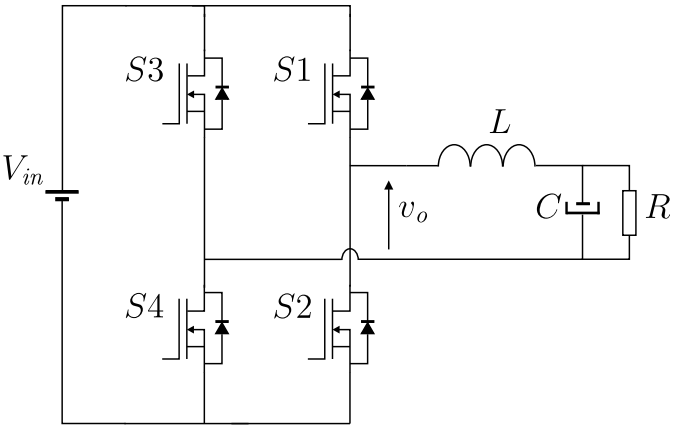

Fig. 9. Topology of the full-bridge buck converter, based upon two platforms

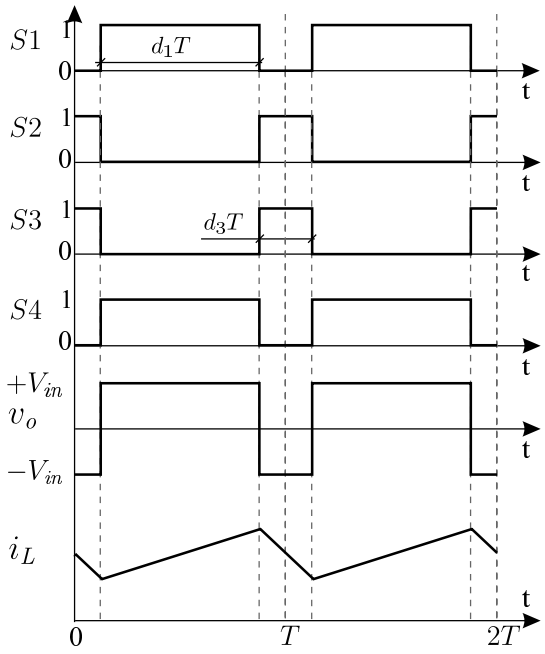

Fig. 11. The switching commands for the four switches and the theoretical waveforms of the full-bridge buck converter

switching voltage was applied as a differential voltage between the inverting and the non-inverting input of the amplifier. In order to obtain the center trace, the same square wave was applied as a common mode voltage to both inputs, yielding an output signal which can hardly be distinguished from zero, as a result of the good common mode rejection. The inset of Fig. 8 shows the same curve, zoomed in to 50 mV/div. The common mode rejection ratio (CMRR) achieved can be estimated from these curves, yielding -40 dB for a slope of the applied voltage steps about 4000 V/μs.

The lower curve of Fig. 8 displays the output of the integrating amplifier for the same input voltage: 390 V and 50 kHz switching. It reveals a good correspondence with the theoretical waveforms of Fig. 3: a constant output voltage, corresponding with the averaged value of the switch voltage. At the end of each switching period, a sharp peak in this voltage is observed, which is due to the reset of one of the capacitors of the integrating circuit.

In order to test the fault protection system of the platform under the worst fault conditions, the platform is supplied by a DC-voltage of 450 V at its bus capacitor. During the test both switches are commanded to close simultaneously, thus causing a short circuit of the bus capacitor and the power supply. In Fig. 10 the resulting current through the switches is shown in the upper trace. The current increases rapidly to reach 110 A in 100 ns, after which a constant saturation current of 70 A is obtained. The reaction of the EXTPROT-signal is displayed in the lower curve of Fig. 10. This signal is cleared after a propagation delay of 250 ns, causing the switches to interrupt the short circuit current another 300 ns later. As a result, the short circuit condition will exist for only 600 ns. Under some conditions the slew rate of the measuring opamps may cause an extra delay in the fault protection path, and the total short circuit time may be prolonged to 1 μs. Since most commercially available switches, MOSFETs or

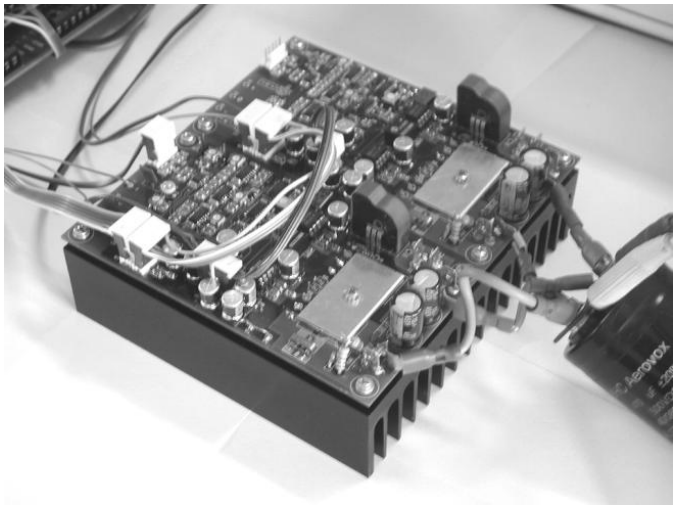

Fig. 12. Photograph of the full-bridge converter, based upon two platforms

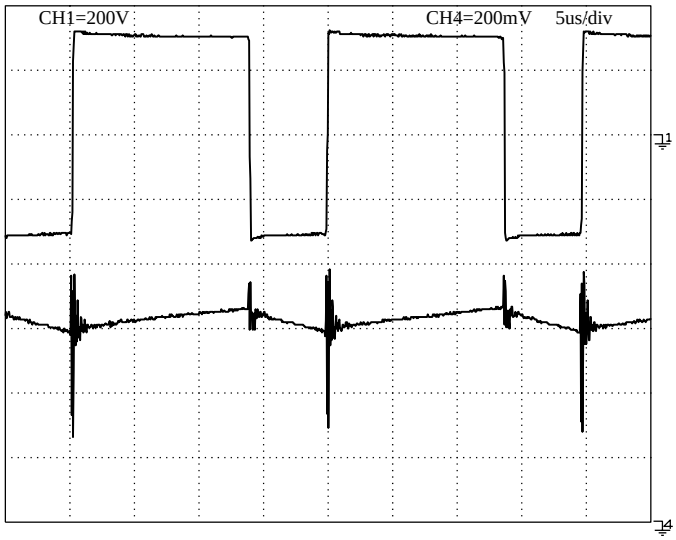

Fig. 13. Experimental waveforms of the full-bridge buck converter. Upper trace: output voltage. Lower trace: output current measurement

IGBTs, withstand a short circuit duration of 10 μs, the switches are protected in time and the platform will not be damaged. Similar experiments have been performed to test the other fault protections, all leading to safe operation of the platform under fault conditions.

C. Example topology: full-bridge buck converter

As second example topology, two platforms were build together to implement a full-bridge buck converter. The topology is depicted in Fig. 9, while a photograph of the setup is shown in Fig. 12. The switching commands for the four switches of the converter are displayed in Fig. 11 together with the theoretical waveforms of the converter, the voltage between the two switching terminals of the platforms and the inductor current of the converter.

The parameters of this experimental converter are

$$\begin{cases} \text{inductance} & L = 11\text{mH}, & \text{input voltage} & V_{in} = 300\text{V}, \\ \text{capacitance} & C = 470\mu\text{F}, & \text{load} & R = 32\Omega, \\ \text{switching frequency} & f_s = 50\text{kHz}, & \text{duty-ratio} & \begin{matrix} D_1 = 0.7 \\ D_3 = 0.3 \end{matrix} \end{cases} \quad (7)$$

The experimental waveforms are depicted in Fig. 13. The upper trace shows the output voltage of the buck converter, which is the voltage between the v_{sw}-terminals of both platforms. The switching patterns of Fig. 11 causes the output voltage to switch between ± 300 V. The resulting output current, measured by the current transducer of one platform, is represented by the lower trace of Fig. 13. The average output current is 3.75 A, corresponding to 640 mV at the output of the amplifiers.

VII. Conclusion

With the advent of high performance digital controllers, the time and effort to implement new control algorithms for the control of power electronic converters have decreased drastically. Nevertheless, the design and the practical implementation of power electronic converters, intended for testing new control algorithms, are still complicated and time consuming activities. Therefore, a fully equipped half bridge test platform was designed ready to use as a fundamental building block for various converter types. The test platform incorporates fault protection, measurements of well-selected voltages and currents, and is directly interfacable with most digital and analog controllers. Due to these features and the flexibility of the board, this half bridge converter can be used for research as well as for educational purposes in applications ranging from a simple 100 W buck converter up to 10 kW inverters for motor control.

After a detailed description of the several peripheral equipment which is integrated in the platform, this platform is demonstrated in this paper by means of some basic converter topologies, the half bridge boost converter and the full bridge buck converter.

References

[1] O. Kukrer, "Discrete-time current control of voltage-fed three-phase PWM inverters," *IEEE Trans. Power Electr.*, Vol. 11, No. 2, March 1996, pp. 260–269.

[2] B.-H. Bae, and S.-K. Sul, "A compensation method for time delay of full digital synchronous frame current regulator of PWM ac drives," *IEEE Ind. Appl. Conf.*, IAS 2001, Sept. 30–Oct. 4, 2001, Chicago, USA, pp. 1708–1714.

[3] P. Jintakosonwit and H. Fujita, and H. Akagi, "Control and performance of a fully-digital-controlled shunt active filter for installation on a power distribution system," *IEEE Trans. Power Electr.*, Vol. 17, No. 1, Jan. 2002, pp. 132–140.

[4] M. Sedighy and S.B. Dewan, and F.P. Dawson, "A robust digital current control method for active power filters," *Trans. Ind. Applic.*, Vol. 36, No. 4, July/Aug. 2000, pp. 1158–1164.

[5] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electr.*, Vol. 13, No. 5, Sept. 1998, pp. 814–823.

[6] A.H. Mitwalli, S.B. Leeb, G.C. Verghese, and V.J. Thottuvelil, "An adaptive digital controller for a unity power factor converter," *IEEE Trans. Power Electr.*, Vol. 11, No. 2, March 1996, pp. 374–382.

[7] D.M. Van de Sype, K. De Gussemé, A.P. Van den Bossche, and J.A.A. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," *IEEE Trans. Power Electr.*, in press.

[8] K. De Gussemé, D.M. Van de Sype, A.P. Van den Bossche, and J.A. Melkebeek, "Input current distortion of ccm boost pfc converters operated in dcm," *Proc. of the IEEE Power Electr. Spec. Conf.*, PESC 2003, June 15–19, 2003, Acapulco, Mexico, pp. 1685–1690.

[9] J. Ghijselen, A. Van den Bossche, and J. Melkebeek, "Improved immunity of current sensorless AC-DC converters for mains voltage disturbances," *Proc. Power Electr. Spec. Conf.*, PESC 2001, June 17–21, 2001, Vancouver, Canada, pp. 748–753.

[10] N. Klaes, "Parameter identification of an induction machine with regard to dependencies on saturation," *IEEE Trans. Ind. Applic.*, Vol. 29, No. 6, Nov./Dec. 1993, pp. 1135–1140.

[11] J. Maes, and J. Melkebeek, "Discrete time direct torque control of induction motors using back-EMF measurement," *Proc. of the IEEE Ind. Applic. Conf.*, IAS 1998, Oct. 12–15, 1998, St-Louis, USA, pp. 407–414.

[12] K. Masoud, and G. Ledwich, "Sampling averaging for inverter control," *Proc. Power Electr. Spec. Conf.*, PESC 2002, June 23–27, 2002, Cairns, Australia, pp.1699–1704.

[13] M. De Wulf, "Sonde differentielle a haute tension," *Electronique*, No. 85, Oct. 1998, p.106.