The ePIXnet silicon photonics platform

Pieter Dumon[1], Jean-Marc Fédéli[2], Wim Bogaerts[1]

[1] IMEC – Ghent University, Department of Information Technology
Sint-Pietersnieuwstraat 41, 9000 Gent
tel. +32 9 264 3448, e-mail: pieter.dumon@intec.ugent.be

[2] CEA-LETI, Minatec, 17 rue des Martyrs, 308054 Grenoble

Abstract – *The ePIXnet silicon photonics platform offers open access to CMOS fabrication facilities for research and prototyping of silicon photonic integrated circuits. Through cost sharing, the cost can be made affordable. Based on the technology in this platform, important achievements in silicon photonics have been reached.*

FACILITY ACCESS PROGRAMME

The silicon photonics platform offers access to the CMOS pilot lines of IMEC (Belgium) and CEA-LETI (France) for fabrication of silicon photonic circuits. Fabrication is done using stable and known wafer-scale processes, including deep UV lithography. Through cost sharing, a large reduction in the cost per user can be obtained, reaching a level that affordable for research labs and start-up companies. The platform is ideally suited for research and prototyping of a lot of different structures or large scale photonic integrated circuits. As the user gets a full wafer of chips, a lot of material is available for post-processing. Also, an automatic feature size variation can be obtained over the wafer if desired, through variation of the exposure dose during lithography.

Mask cost, processing cost, the cost of mask checking and integration and post-processing such as thinning and dicing, are all shared by the users signing in to a fabrication run. In this way, a large cost reduction is obtained. This is only possible through the use of a electronic IC fabrication environment. The cost per user is reduced by a factor of 5 to 10 compared to a single-user run. The more users join a fabrication run, the lower the cost for each user. The platform offers a limited but still diverse set of processes, and to a certain extent standardizes on mask design, allow for further cost reduction. The cost paid by the user reflects the actual cost, including mask, mask checking and integration, processing and postprocessing. A cost model is elaborated on the website. As the cost of coordination of the silicon photonics platform is covered by the EU ePIXnet Network of Excellence, users that are not an ePIXnet partner pay an overhead cost.

The platform issues calls for participation 2 to 3 times a year, to which users can sign in. The users deliver their mask designs and the platform returns the users one or a few wafers each. The facility access programme is basically open to research labs and commercial users, from Europe and worldwide. The facility access programme currently runs on a best effort basis. More details can be found on the website.

Both IMEC and CEA-LETI open up their CMOS pilot line through the silicon photonics platform. All technology is wafer-scale on 200mm SOI wafers. Only processes that are stable and known are offered. Process development is not a part of the platform. The platform offers passive waveguides and photonic crystals in SOI at both IMEC [1] and CEA-LETI [2]. IMEC focusses on a Si film thickness of 220nm and maximizes cost sharing in this way, while LETI offers a more flexible film thickness between 50nm and 400nm. At both locations, 193nm and 248nm deep UV lithography is used. Figure 1 illustrates the typical kind of structures based on this technology. Beyond the processing of simple waveguide structures and photonic crystals, IMEC offers a standard grating coupler module for interfacing to fibre, again maximizing cost sharing. These grating couplers have great alignment tolerances and therefore allow for much easier and faster alignment than with end-fire coupling, saving precious time in characterisation. A guideline for creating a measurement setup is available on the website. The shallow etch used for this fibre couplers is also available to create double-etch structures, as illustrated in figure 2, and more advanced fibre couplers. The alignment tolerance between both lithography steps is about 50nm with the right alignment markers. The platform takes care of integrating the right alignment markers on the mask designs. Like IMEC, CEA-LETI can etch shallow or completely through the Silicon film. The etch depth can be chosen flexibly. CEA-LETI also offers epitaxy of Si, SiGe and Ge films onto SOI. These processes can be used as a basis for advanced devices such as detectors and for complex structures with a varying Silicon film thickness. Additionaly, waveguides can be defined in amorphous Silicon-on-insulator in addition to the standard crystalline SOI [2]. To obtain planar surfaces, CMP (chemical

mechanical polishing) steps can be included. After fabrication, wafers can be diced if desired. At IMEC, wafers can be thinned to allow for an easy cleaving of facets. On the other hand, polished facets for end-fire coupling to (high NA or lensed) fibre can be obtained through the ePIXnet network packaging platform.

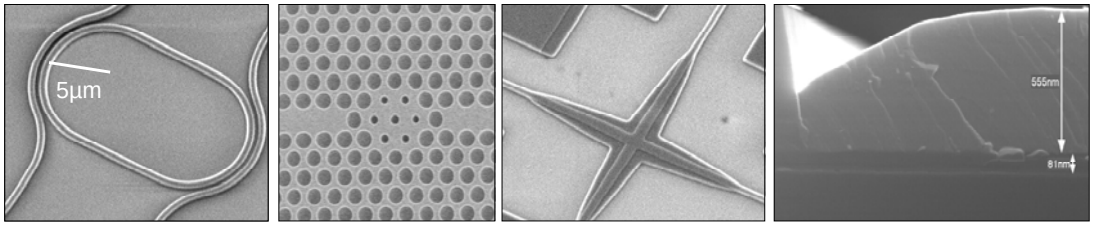

Figure 1: The fabrication processes support a variety of structures (from left to right): ring resonator, photonic crystal cavity, waveguide crossing in double-etch scheme and Ge epi in a Si waveguide

ABOUT THE PLATFORM

The silicon photonics platform is created by the EU FP6 ePIXnet network of excellence. The platform wants to help build a future for silicon photonics in Europe through the development of a fabless model for the fabrication of silicon photonic circuits. The rationale is to re-use as much as possible the processes, tools and methods of CMOS labs and foundries, and focus on the problems to be tackled for fabricating general silicon photonic circuits in a CMOS environment. While research and development is not a task of the platform, the platform wants to foster and help set out routes for the development of missing links in the design and fabrication toolchain and the definition of the various interfaces in this chain.

USAGE EXAMPLES

Several achievements were demonstrated using the platform's technologies. Passive wavelength filters were shown [1], as well as various basic structures such as low-loss waveguides, bends and waveguide crossings [3]. The double etch scheme allows for easy-to-use, tolerant fibre couplers [4] and low-loss crossings, AWG devices and others by locally using a lower index contrast. Low-loss amorphous silicon can be used for a number of passive devices [2]. High-speed all-silicon optical modulators were demonstrated [5]. Through Si and Ge epitaxial growth, ultra-high-speed infrared photodetectors are within reach [6]. Through die-to-wafer bonding of III-V material on top of passive silicon photonic circuits, ultra-compact disk laser sources were demonstrated [7]. This technology is not offered through the platform, but demonstrates the possibilities for post-processing and the huge potential for silicon as a generic integration platform when combined with other materials.

REFERENCES

[1] W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. V. Campenhout, P. Bienstman, and D. V. Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with cmos technology," *Journal of Lightwave Technology*, vol. 23, no. 1, pp. 401–412, 2005.

[2] B. Han, R. Orobtchouck, T. Benyattou, Binetti, Jeannot, J. M. Fedeli, and X. J. M. Leijtens, "Comparison of optical passive integrated devices based on three material for optical clock distribution," in *ECIO 2007, Copenhagen, Denmark*, 2007.

[3] W. Bogaerts, P. Dumon, D. Van Thourhout, R. Baets, Compact, Low-Loss Waveguide Crossings for High-Index-Contrast SOI Photonic Wires ,*Optical Fiber Communications (OFC)*, United States, p.OTuM1, 2007

[4] F. Van Laere, W. Bogaerts, D. Taillaert, P. Dumon, D. Van Thourhout, R. Baets, Compact Focusing Grating Couplers Between Optical Fibers and Silicon-on-Insulator Photonic Wire Waveguides, *Optical Fiber Communications*, United States, p.OWG1 (2007)

[5] D. Marris-Morini, X. Le Roux, D. Pascal, L. Vivien, E. Cassan, JM. Fedeli, JF. Damlencourt, D. Bouville, J. Palomo, S. Laval, High speed all-silicon optical modulator, *Journal of Luminescence*, pp. 387 – 390, 2006

[6] M. Rouviere, L. Vivien, X. Le Roux, J. Mangeney, P. Crozat, C. Hoarau, E. Cassan, D. Pascal, S. Laval, JM Fedeli, JF Damlencourt, JM Hartmann, S Kolev, Ultrahigh speed germanium-on-silicon-on-insulator photodetectors for 1.31 and 1.55 mu m operation, *Applied Physics Letters*, 87(23) , December 2005

[7] J. Van Campenhout, P. Rojo-Romeo, P Regreny, C Seassal, D. Van Thourhout, S. Verstuyft, L. Di Cioccio, JM Fedeli, C. Lagahe, R. Baets, Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit, *Optics Express*, May 28, 2007

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