Heterogeneously integrated III-V/Si single mode lasers based on a MMI-ring configuration and triplet-ring reflectors

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ABSTRACT

In this paper we show that using a DVS-BCB adhesive bonding process compact heterogeneously integrated III-V/silicon single mode lasers can be realized. Two new designs were implemented: in a first design a multimode interferometer coupler (MMI) – ring resonator combination is used to provide a comb-like reflection spectrum, while in a second design a triplet-ring reflector design is used to obtain the same. A broadband silicon Bragg grating reflector is implemented on the other side of the cavity. The III-V optical amplifier is heterogeneously integrated on the 400nm thick silicon waveguide layer, which is compatible with high-performance modulator designs and allows for efficient coupling to a standard 220nm high index contrast silicon waveguide layer. In order to make the optical coupling efficient, both the III-V waveguide and the silicon waveguide are tapered, with a tip width of the III-V waveguide of around 500nm. The III-V thin film optical amplifier is implemented as a 3µm wide mesa etched through to the n-type InP contact layer. In this particular device implementation the amplifier section was 500µm long. mW-level waveguide coupled output power at 20°C and a side mode suppression ratio of more than 40dB is obtained.

Keywords: silicon photonics; heterogeneous integration; single wavelength lasers

1. INTRODUCTION

Silicon-On-Insulator (SOI) waveguide circuits are widely studied because of the large refractive index contrast that is available on this platform, which allows realizing ultra-compact devices. The interest in this technology stems also from the expectation that the maturity and low-cost of CMOS-technology can be applied for advanced photonic products [1]. Since silicon lacks efficient light emission and amplification, the integration of III-V semiconductors on top of silicon waveguide circuits is required to achieve complex integrated circuits. Several approaches can be followed to realize this integration. Heterogeneous integration through die-to-wafer bonding and direct hetero-epitaxy allow for dense and wafer-scale integration of the III-V opto-electronic components on the silicon photonic platform. Since the quality of hetero-epitaxially grown layers is inferior to III-V epitaxy grown on its native substrate, the heterogeneous integration of III-V semiconductors on silicon using a wafer bonding technique is currently the most relevant solution for the waveguide circuits, mainly molecular wafer bonding and DVS-BCB adhesive bonding techniques are used and are actively reported in state-of-the-art hybrid amplifiers [2-3] and lasers [4-11].

In these approaches, unstructured InP-based dies are bonded, epitaxial layers down, on an SOI waveguide circuit wafer, after which the InP growth substrate is removed and the III–V epitaxial film is processed. In this paper we show that

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using a DVS-BCB adhesive bonding process compact heterogeneously integrated III-V/silicon single wavelength lasers can be realized, which are key optical components in communication and sensing systems.

2. DIE-TO-WAFER BONDING TECHNOLOGY

The bonding process was developed for multiple III-V die-to-silicon wafer bonding, as well as single die bonding. A MicroTec Süss ELAN CB6L wafer bonder was used for the bonding experiments. The bonding process starts with the cleaning of the SOI substrate and III-V dies. The SOI cleaning is performed by dipping the substrate into a Standard Clean 1 (SC-1) solution heated to 70°C, for 15 min. After this, the DVS-BCB:mesitylene solution is spin-coated onto the SOI substrate. The SOI substrate is then baked for 10 min at 150°C, to let mesitylene evaporate, after which the substrate is slowly cooled down to room temperature. Finally, the SOI is mounted on a carrier wafer made of Pyrex glass. Meanwhile, prior to bonding, two sacrificial layers on the III-V die are removed by selective wet etching, which also removes particles and contaminants from the III-V die surface. The III-V die is then rinsed with DI water, dried and mounted on the SOI die. Since in the presented method the dies are contacted at room temperature, individual dies can easily be pick-and-placed onto the silicon target wafer. They can be aligned manually with an accuracy of 500µm without any extra tools or can be placed more accurately using a flip-chip machine. After that, the SOI substrate on its carrier wafer is mounted on the transport fixture and is loaded into the processing chamber of the wafer bonding tool. The chamber is pumped-down and heated to 150°C with a ramp of 15 °C/min for 10 min, while applying pressure on the III-V/SOI stack. The actual bonding pressure (the applied force per area of the III-V die) is kept in the range of 200 to 400 kPa. After keeping the pressure on the dies for 10 min at 150 °C, the temperature is increased up to 280 °C, with a ramp of 1.5 °C/min. Upon reaching 280 °C, the dies are kept at this temperature for 60 min in a N_2 atmosphere. After the curing, the bonded samples are cooled down (at 6-10 °C/min) and unloaded from the processing chamber. The InP substrate of the III-V die is then removed by selective wet etching, leaving a thin III-V film with the functional layers bonded to the SOI die, ready for further processing. Some examples of transferred epitaxial III-V material onto silicon waveguide circuits are shown in Figure 1 [7].

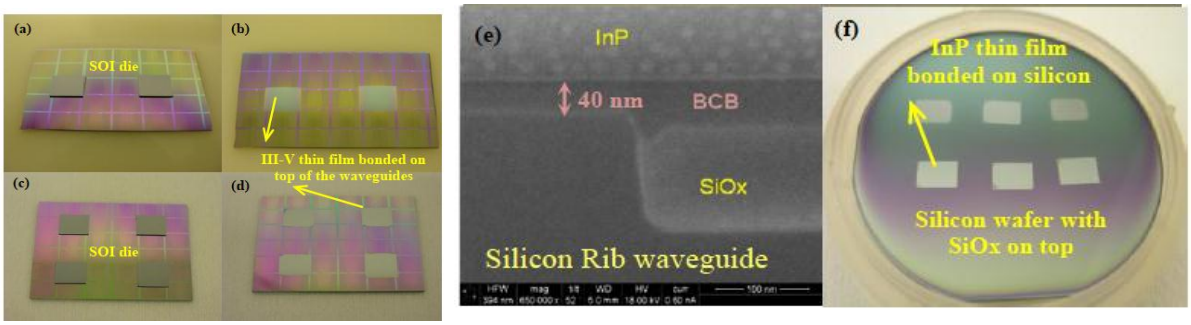

Figure 1: (a-b) two epitaxial 0.3 cm^2 III-V dies bonded on a planarized SOI die before and after the substrate removal process; (c-d) four epitaxial 0.3 cm^2 III-V dies bonded on a planarized SOI die before and after the substrate removal process; (e) SEM image of the bonding interface (f) 6 InP-membranes (with the individual die area of 0.2 cm^2)

3. III-V ON SILICON SINGLE WAVELENGTH LASERS

Several types of single wavelength lasers have been realized in recent years. Distributed feedback lasers and distributed Bragg reflector lasers [5-6, 8-9], with the grating implemented in the silicon waveguide layer were the first to be demonstrated. These devices are based on a hybrid mode layout where a large fraction of the optical field is confined in the silicon device layer and only the evanescent tail feels the multi-quantum well gain region. Both devices based on molecular and adhesive bonding technology were realized this way. Another approach to realizing III-V on silicon single wavelength lasers is to confine the optical mode completely in the III-V device layer, such that maximum modal gain can be achieved. Since the optical feedback structures are still implemented in the silicon device layer, a mode converter structure is required to couple the light efficiently between the III-V laser mesa and the silicon device layer. This structure is shown in Figure 2(a). The III-V/silicon taper structure consists of two sections: first, the III-V mesa is tapered from 3 µm to 900 nm over a length of 45 µm after which the III-V mesa is gradually tapered from 900 nm to 500 nm over a length of 150 µm. The silicon waveguide underneath tapers from 300 nm to 1 µm over 150 µm. This taper is

implemented in a 400nm thick silicon device layer (etched 180 nm), which is then in its turn efficiently coupled to the 220 nm device layer using a short adiabatic taper structure. The DVS-BCB bonding layer thickness, determining the separation between the silicon waveguide layer and the III-V layer is 110 nm in this implementation. The III-V layer stack consists of a p-InGaAs contact layer, a p-InP cladding layer (1.5 μm thick), six InGaAsP quantum wells (6 nm) surrounded by two InGaAsP separate confinement heterostructure layers (100 nm thick, bandgap wavelength 1.17 μm) and a 200 nm thick n-type InP layer. These structures were also used in our previous reports [10-11].

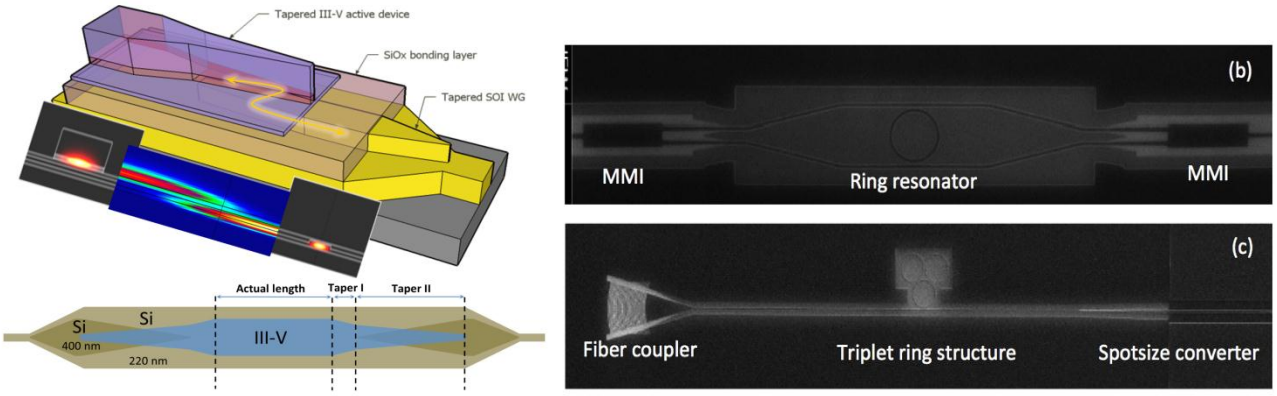

Figure 2: (a) layout of the III-V-to-silicon spotsize converter; (b), and (c) Scanning electron microscope pictures of the used wavelength selective feedback structures in silicon.

In order to realize single wavelength laser structures, two different wavelength selective feedback structures are used in this work. One structure is based on the use of an MMI-ring resonator configuration to realize a comb-like reflection spectrum. A second implementation is based on the use of a triplet ring resonator configuration to achieve the same goal. Figure 2(b) and Figure 2(c) shows a scanning electron microscope picture of these wavelength selective feedback structures.

4. DEVICE FABRICATION

A key component in the proposed III-V-on-silicon device structure is the III-V semiconductor spot-size converter. While taper tip widths of 500nm are trivial for silicon photonic integrated circuits fabricated using deep UV lithography, this is far less the case for the III-V taper tip that is realized used i-line contact lithography. In this work these high aspect ratio taper tips are realized using wet chemical etching. The general fabrication flow of our heterogeneous III-V on silicon integration process was discussed in detail before [10]. First the silicon waveguides are fabricated, in this case starting from an SOI wafer with a 400nm thick silicon waveguide layer. All patterns were defined using 193 nm deep UV lithography. A 180nm deep etch step defines the 400nm ridge waveguides and the 220nm device layer, which is used for the passive silicon circuitry. Then a 70nm deep etch step defines the DBR-mirrors and the grating couplers. In a last step the 220nm strip waveguide are etched. Next, a SiO2 cladding layer is deposited and the wafer is planarized using chemical mechanical polishing (CMP) and a controlled wet etch down close to the top of the 400nm thick silicon waveguide layer.

The III-V epitaxial layer structure was grown on an InP substrate using MOCVD. It was bonded upside down onto the silicon waveguide layer using the process described in [7], resulting in a 110nm thick intermediate DVS-BCB and SiOx layer. Next the InP substrate was removed by wet chemical etching down to an InGaAs etch stop layer (Figure 3a). This leaves us with a wafer containing the silicon waveguides and the III-V active layer in which the amplifier mesas can be defined using standard wafer scale processes, lithographically aligned to the underlying SOI waveguide circuit. A Ti/Pt/Au stripe, acting as a p-side contact and also as a hard mask for the mesa etching was defined with a lift-off process using 320 nm UV contact lithography (Figure 3b). Selective wet etching was used to etch through the InGaAs layer, the InP p-doped layer and the MQW (Figure 3c-e). By carefully selecting the orientation of the amplifier mesa with respect to the crystal orientation prior to bonding, a negative sidewall slope can be achieved in the anisotropic etching of InP. GeAu/Ni was used for the n-contacts (Figure 3f). The active waveguide is encapsulated with DVS-BCB (Figure 3g) and extra Ti/Au contacts layers were added for the contact pads (Figure 3h). Figure 1h shows a cross-section taken at the end

of the taper structure, showing the adiabatic taper at its narrowest point. Using the fabrication process outlined above a width of 500nm, required for low loss coupling, is reliably obtained even though it relies on standard contact mask lithography.

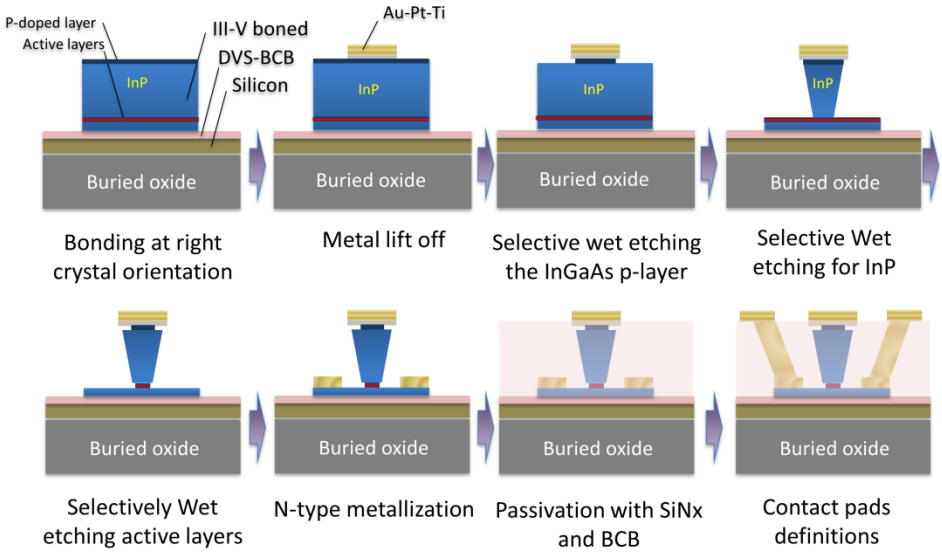

Figure 3: III-V on silicon laser process flow.

5. DEVICE CHARACTERISATION

The devices realized in this way were tested in continuous wave at 20°C. Both the L-I-V curves and optical spectra were recorded. Figure 4 and 5 shows the measurement results for both a triplet ring resonator configuration device and an MMI-ring resonator configuration device respectively. The ring resonator used in case (a) had a radius of 5 µm resulting in a free spectral range of 18 nm, while the ring resonator structure in case (b) had a radius of 3 µm resulting in a free spectral range of 30 nm. The III-V thin film optical amplifier is implemented as a 3µm wide mesa etched through to the n-type InP contact layer. In this particular device implementation the amplifier section was 500µm long. 35 mA threshold current and mW-level optical output power coupled to the silicon device layer is obtained. The spectral characteristics show clear single mode operation with a side mode suppression ratio of more than 40dB. This clearly illustrates the potential of these single wavelength laser sources for use in integrated optical transmitters on a silicon photonics platform.

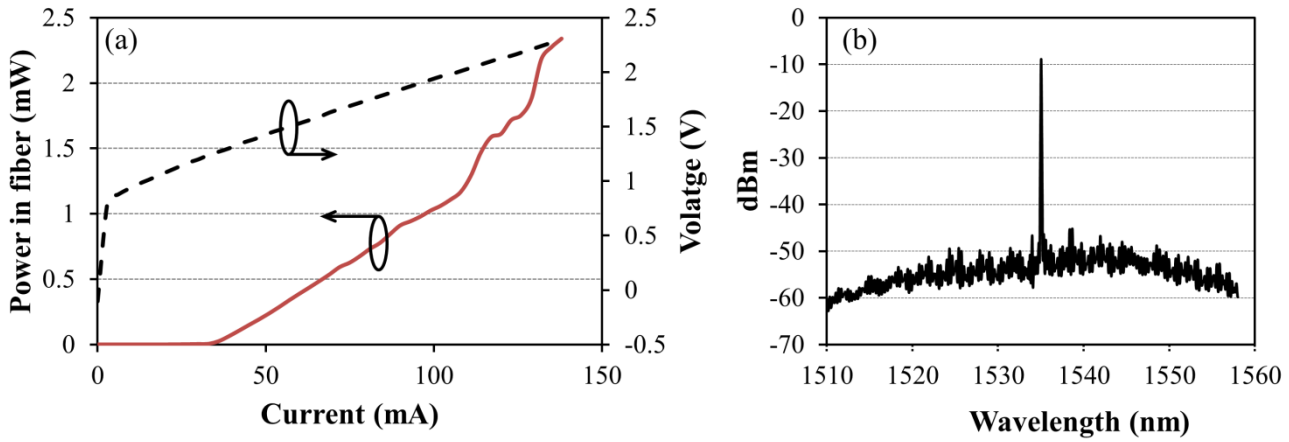

Figure 4: L-I-V curves of the realized triplet-ring resonator single wavelength laser (a) and the corresponding output spectrum (b)

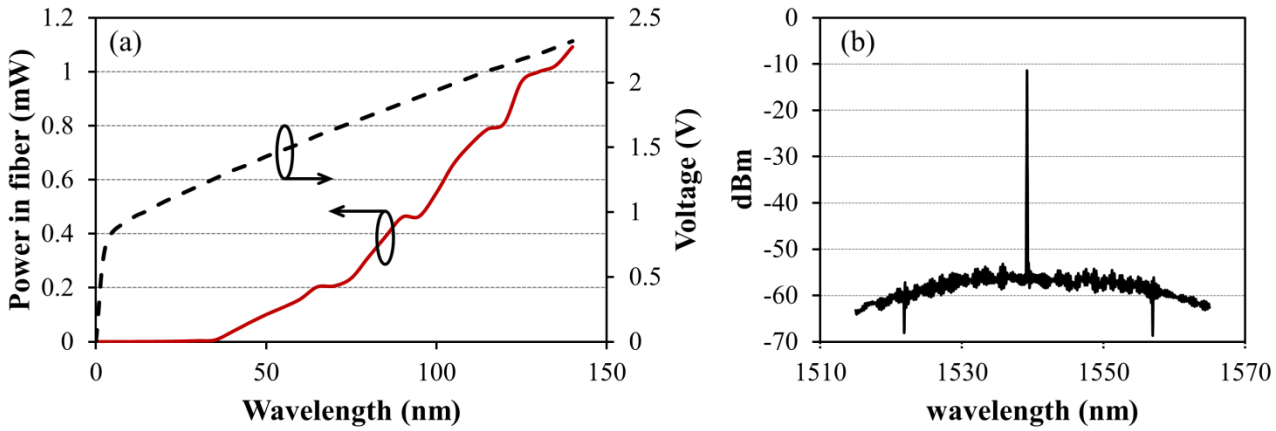

Figure 5: L-I-V curves of the MMI-ring resonator single wavelength laser (a) and the corresponding output spectrum (b)

6. CONCLUSIONS

In this paper we demonstrate two novel types of hybrid III-V/silicon single wavelength lasers. mW level optical output power and more that 40dB side mode suppression ratio are obtained. This shows the potential of these laser sources for a range of different applications, including optical transceivers and photonic integrated circuits for sensing applications.

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