View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Ghent University Academic Bibliography

Integrated Subblocks for RF Ranging Applications

Guy Torfs

Supervisor(s): Jan Vandewege, Johan Bauwelinck

I. Introduction

Scaled chip technologies made it possible to integrate high speed applications in portable devices. A large subset of these devices are situated into the area of sensor networks, which would benefit from location information. Location aware devices such as [1] require a bandwidth of at least 250MHz to perform an accurate time-of-arrival ranging. The ultra-wide band pulse based radio sends a signal with a fast risetime which makes it possible to detect the arrival of the signal within a range of 3ns, giving a resolution of less than 1m. To increase the integration and thus reduce the cost and the power consumption, specific building blocks should be developed. A low power baseband filter and flash analog-to-digital converter (ADC) required for ranging are developed and discussed here, this with the accent on ranging applications.

II. Baseband Filter

The RF ranging signal situated around 2.45GHz is received and downconverted. The huge bandwidth of the ranging signal makes it necessary to have a wide baseband path (125MHz). The main challenge, for accurate reception, is the presence of strong UMTS transmitters close to the signal of interest. To remove the interference a very linear high order filter is necessary. This is implemented as in [2], but with some extra linearity improvements. This resulted in a very low power solution with a figure of merit being 3dB higher than the state-of-the-art.

III. Low-Power 4-bit ADC

To digitize the ranging signal a low resolution ADC is sufficient, but due to the broadband nature of the signal a high sampling speed is needed. A flash ADC is the most promising approach in such situations. A common problem in flash ADCs is kickback noise, charge that is pushed back to the input which gives a memory effect to the different comparators. To reduce this, a novel technique was proposed [3]. This kind of comparator is implemented and tested in a 4-bit ADC and resulted in an improved figure of merit compared to devices with a similar speed and technology node.

IV. Conclusions

Two state-of-the-art building blocks were developed and described. A low power baseband filter with improved linearity outpasses the best figure of merit reported by 3dB. Next to this filter, a high speed low power ADC is proposed which outperforms devices with similar speed in a comparable technology node. Ongoing research targets the integration of the full receiver chain.

References

[1] X. Yin, et al, *Embedded ranging in ISM band*, IET Electronics Letters, Vol. 44, Nr. 17, August 2008, pp. 1043-1045.

[2] S. D'Amico, et al, *A 4.1-mW 10-MHz Fourth-Order Source-Follower-Based Continuous-Time Filter with 79-dB DR*, IEEE JSSC, Vol. 41, Nr. 12, December 2006, pp. 2713-2719.

[3] G. Torfs, et al, *A low-power reduced kick-back comparator with improved calibration for high-speed flash ADCs*, IEICE Transactions on Electronics., Vol. E92-C, Nr. 10, October 2009, pp. 1328-1330.

G. Torfs is with the Department of Information Technology, Ghent University Belgium. E-mail: Guy.Torfs@intec.UGent.be